

## Status and outlook for etched multilayer EUV mask

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# Outline

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**[1] Introduction**

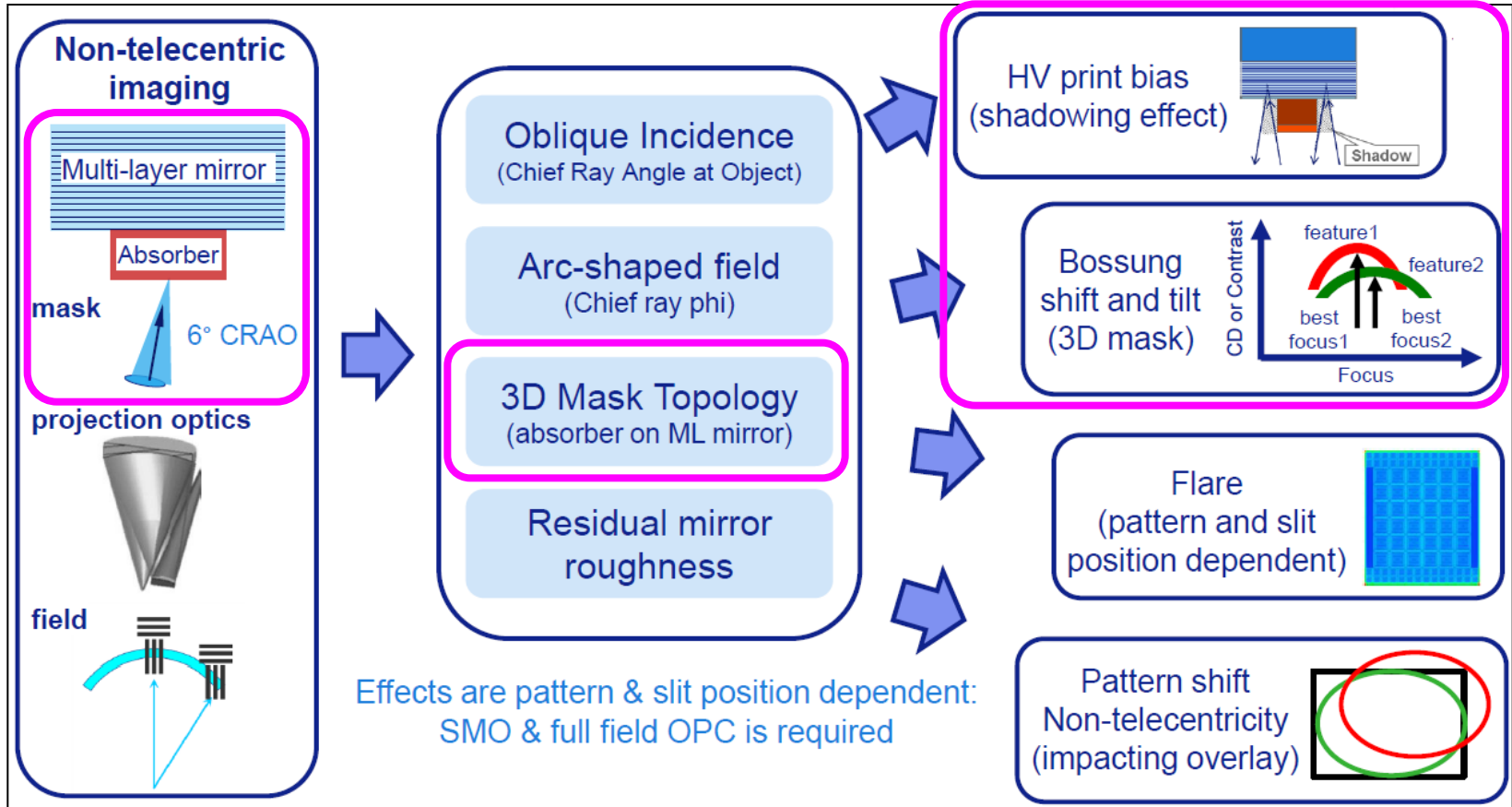
**[2] Current Process Issue and Solutions**

**[3] Evaluation Results**

**[4] Summary**

# Challenges for 0.33NA EUVL Caused by 3D Mask Topology

Martin van den Brink (ASML), BACUS2014

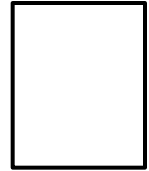


**As target pattern shrinks, the hurdles induced by mask 3D topology go higher in 0.33NA EUVL system.**

# Challenges for High-NA EUVL and Solution

EUVL Symposium 2013

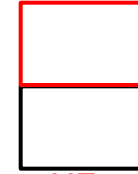
Resolution



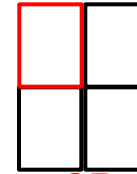
X Mag. = 9/12inch Mask  
(6 or 8)

FF(26x33)

- Infrastructure for large mask



HF  
(16.5x26)



QF  
(13x16.5)

X Mag. = 6inch Mask  
(5 or 8)

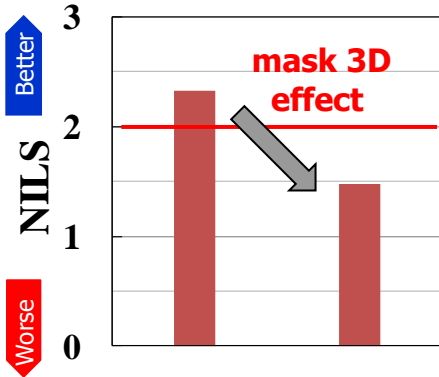
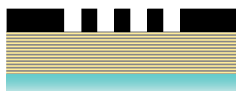
- Low exposure throughput  
- Stitching technology

High-NA EUVL trade off

Full-field

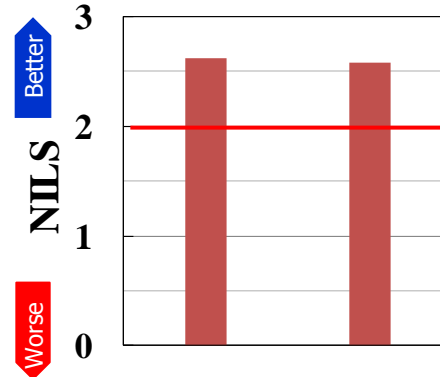
6inch mask

Ta based absorber



lower mask 3D effect

Etched Multilayer

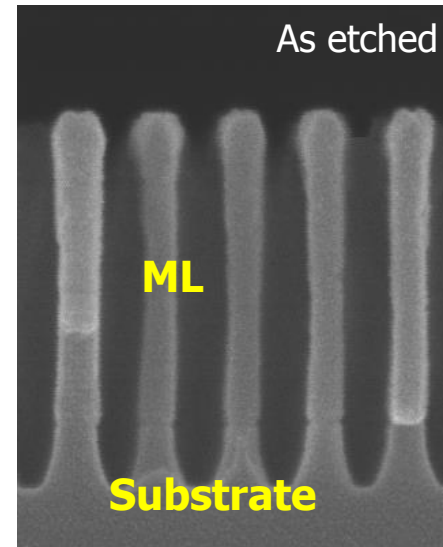
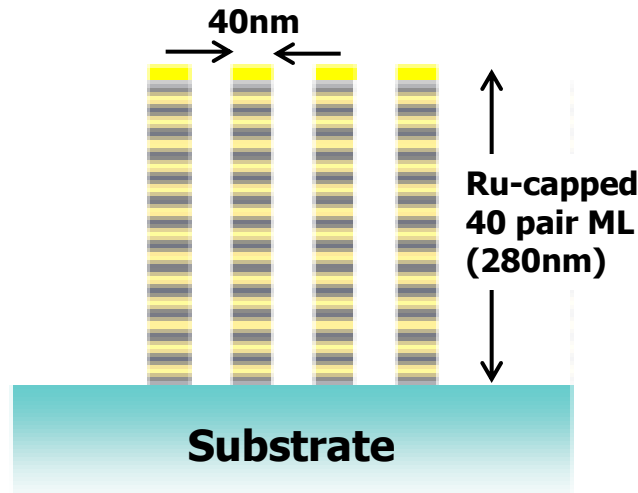


NA=0.5,  
CRA=8deg  
hp10nm

Etched multilayer mask can solve high-NA EUVL trade off (full-field, 6inch mask, high wafer resolution).

# Challenges for Etched Multilayer Mask

Illustration and X-SEM image of **etched ML mask pattern of hp 40nm** (corresponds to hp10nm on wafer)



EUVL symposium 2013

- Mask CD/ profile control
- ML pattern collapse durability against mask cleaning
- Defect inspection
- Repair of ML pattern intrusion defect
- .....

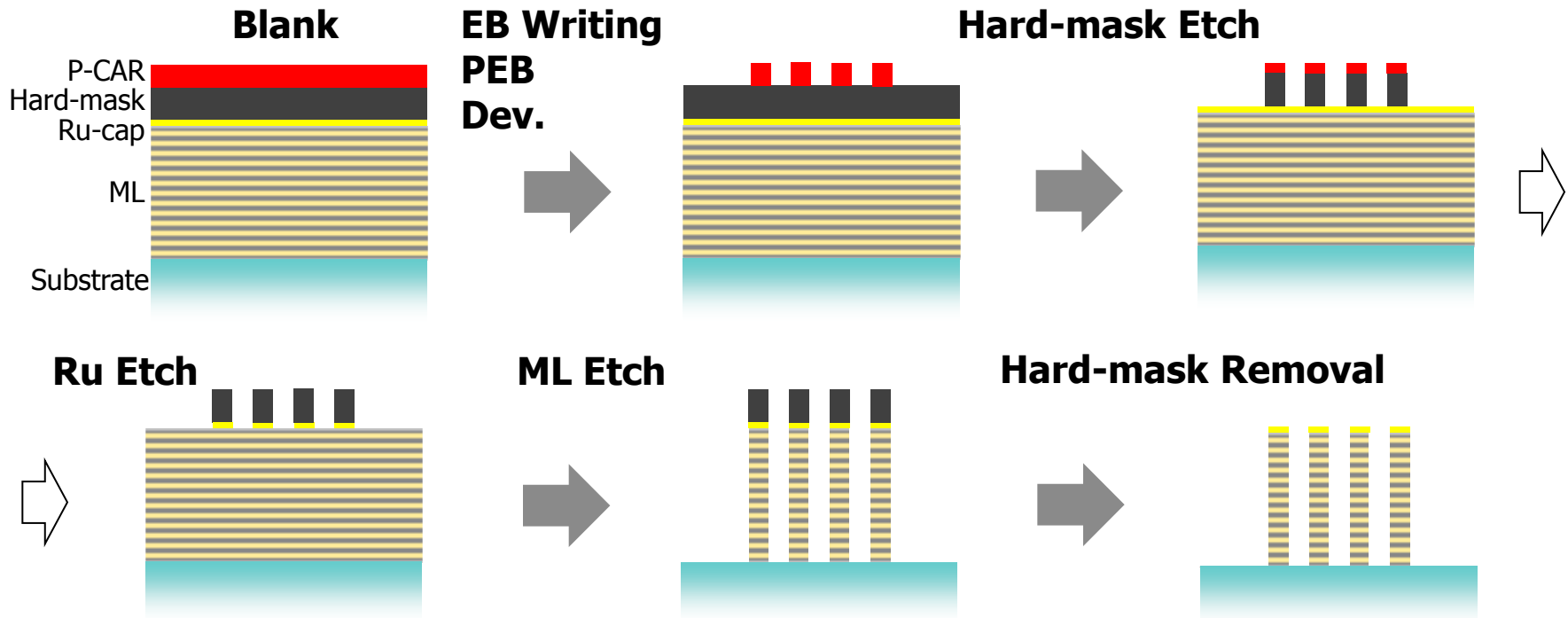
# Motivation

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Motivation is to check the feasibility of etched ML mask patterning **for 0.33NA and for high-NA** from the viewpoint of listed below;

- **Etched ML pattern collapse durability** against mask cleaning
- **Etched ML pattern CD performance** comparing to the requirement of ITRS 2013

# Process Flow of Etched ML Mask



- In order to fabricate fine ML pattern, hard-mask process is selected.
- All the dry etching processes are carried out by ARES™ (Advanced Reticle Etch System).

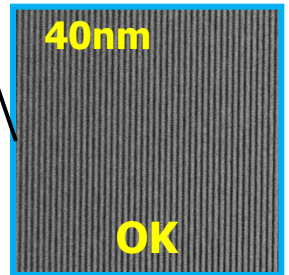
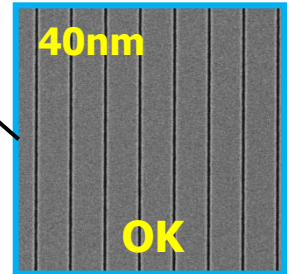


ASH/BAURA

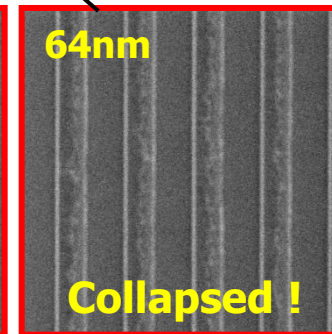
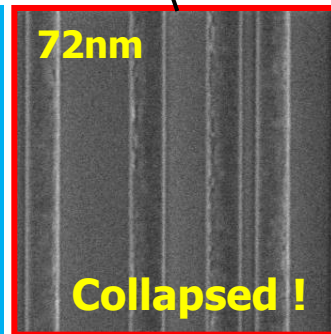
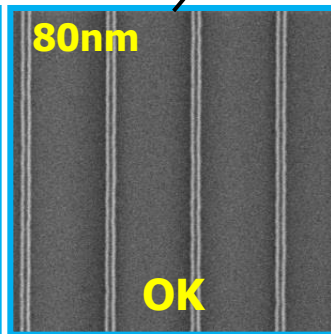
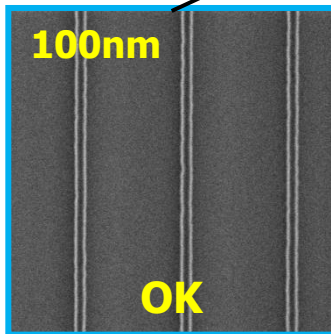
# Cleaning Durability of Etched ML Pattern

**Durable Feature Size after Cleaning** 0.33NA Target @2015 High-NA Target

	Designed Width [nm]									
	160	120	100	80	72	64	56	48	44	40
Iso. Trench										
Dense Trench										
Iso. Line										



**Top down SEM images after mask cleaning**



...OK  
 ...NOT OK

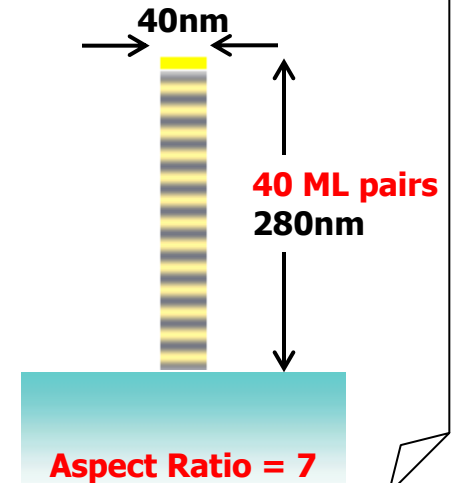
**Isolated/dense 40nm trench pattern is obtained, however, isolated 72nm line is collapsed due to low cleaning durability.**



# Root Cause of Pattern Collapse and Solution

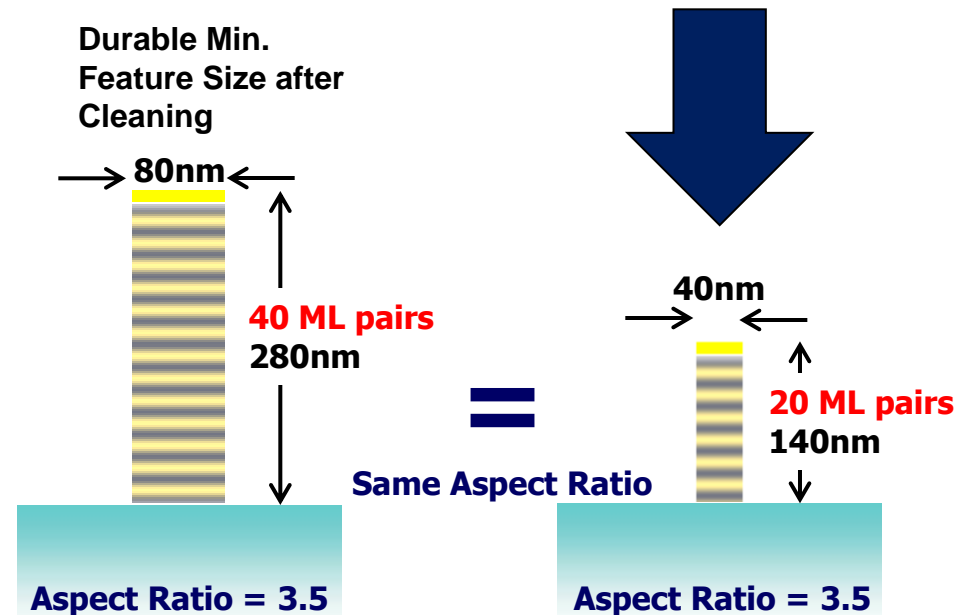
## Root Cause of ML Pattern Collapse:

- Large bending force **caused by high aspect ratio** of ML pattern during mask cleaning



## Solution:

- **Reducing 40 ML pairs to 20 ML pairs** which correspond to the same aspect ratio of durable mask topology

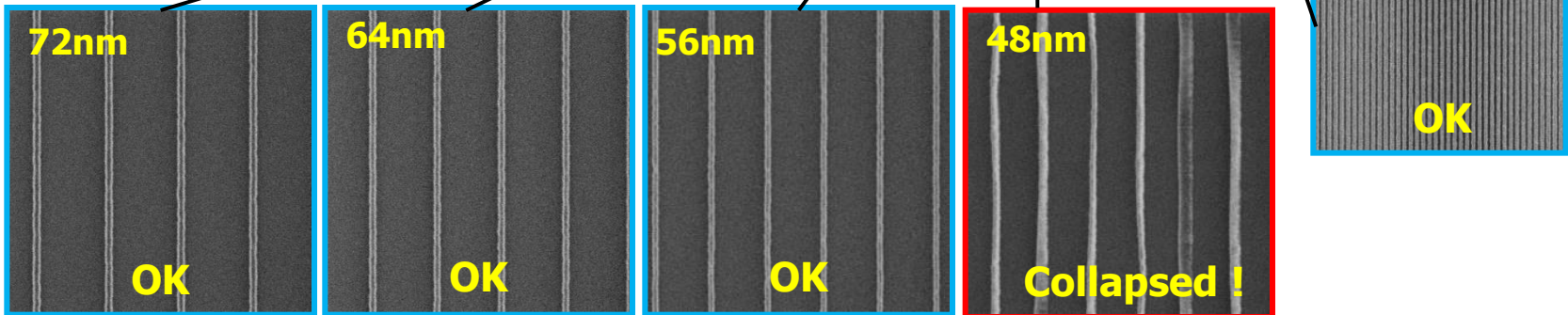


# Cleaning Durability of Etched 20ML Pattern

**Durable Feature Size after Cleaning**      0.33NA Target @2015      High-NA Target

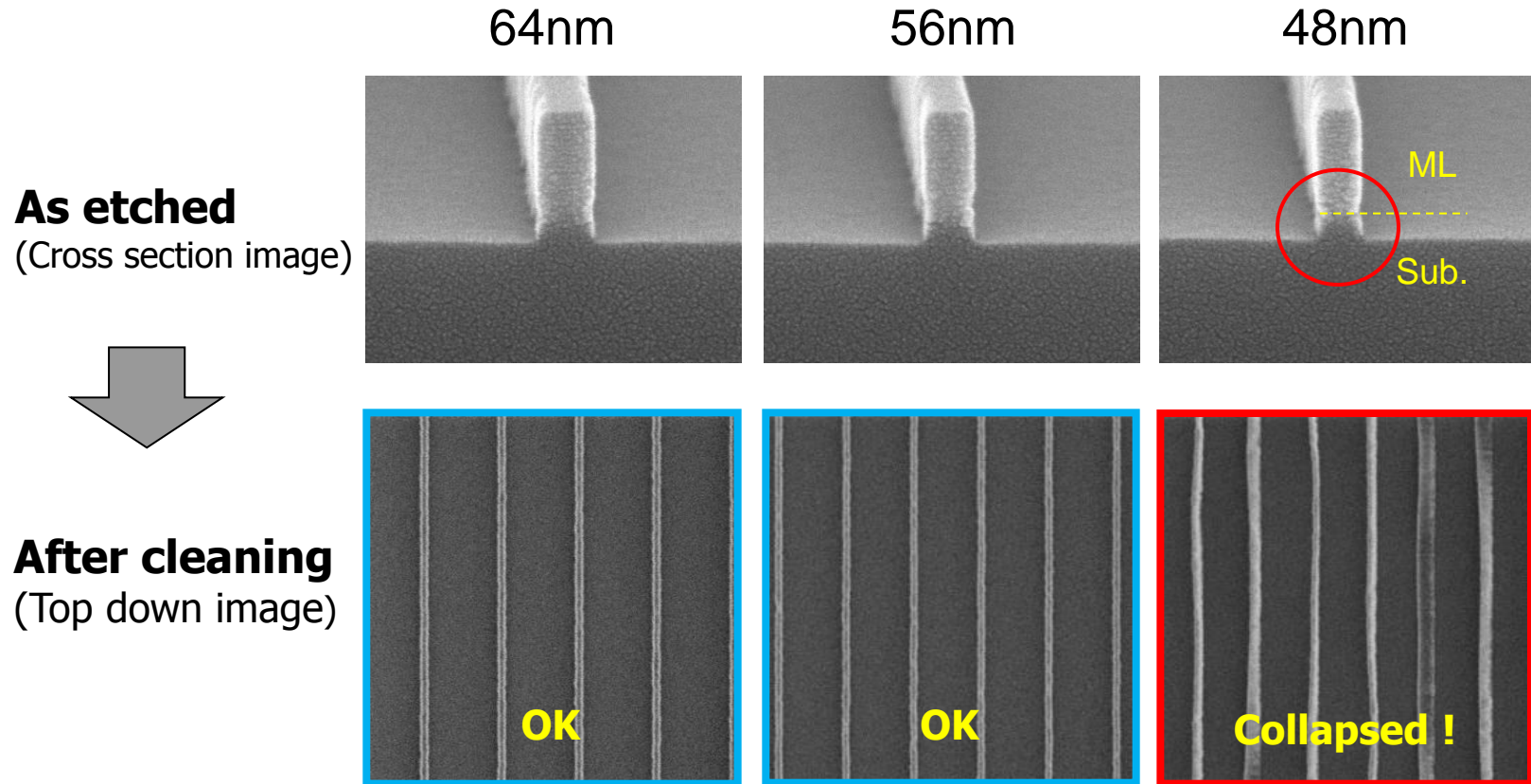
	Designed Width [nm]									
	160	120	100	80	72	64	56	48	44	40
Iso. Trench	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
Dense Trench	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
Iso. Line	OK	OK	OK	OK	OK	OK	OK	NOT OK	NOT OK	NOT OK

**Top down SEM images after mask cleaning**



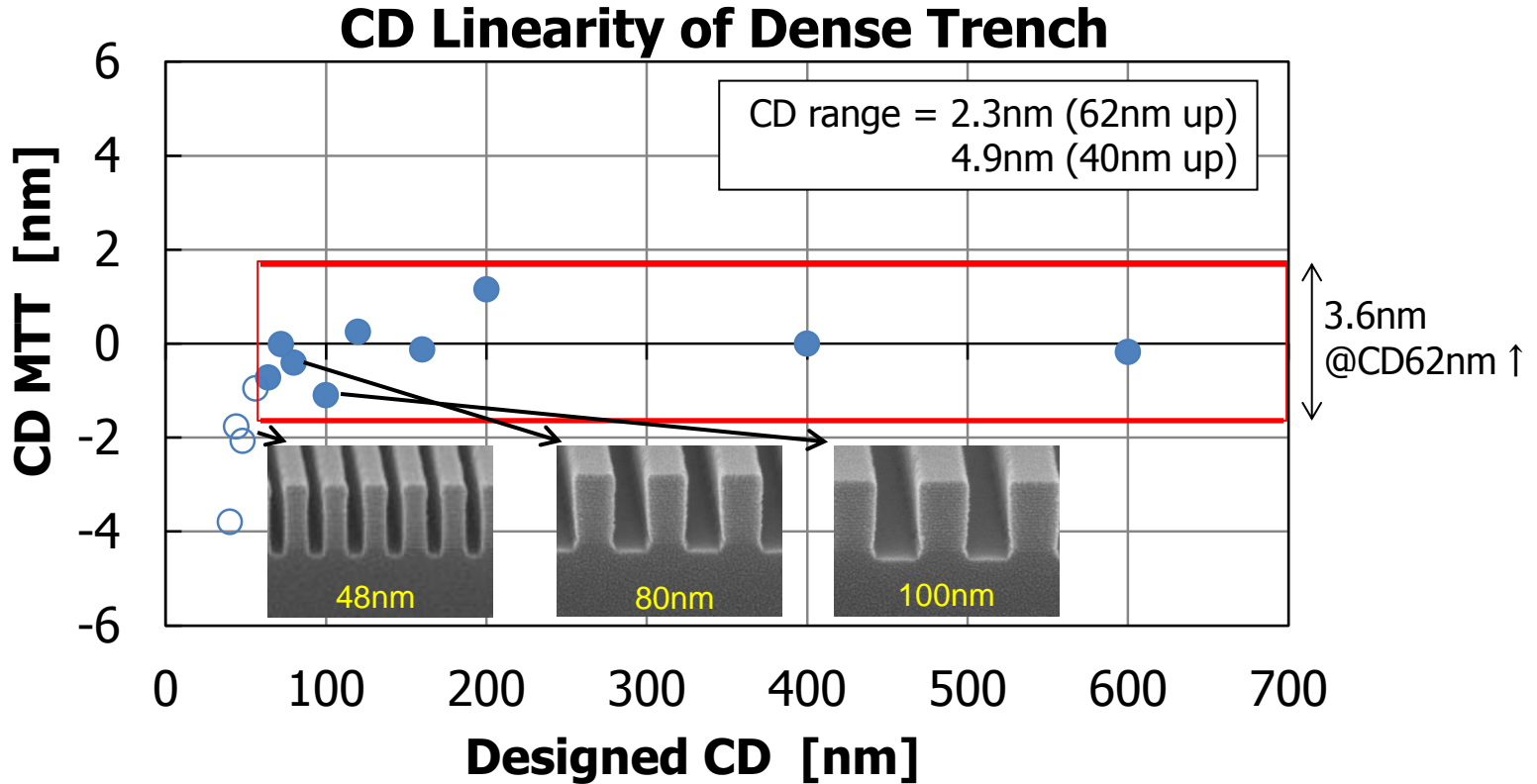
**Durable minimum size is improved to 56nm at isolated line.  
0.33NA CD target @2015 is achieved by simply reducing ML pairs.**

# Isolated Pattern Profile of Etched 20ML Mask



**Root cause that durable feature size of isolated pattern does not reach to 40nm will be worse pattern profile, such as notched shape.**

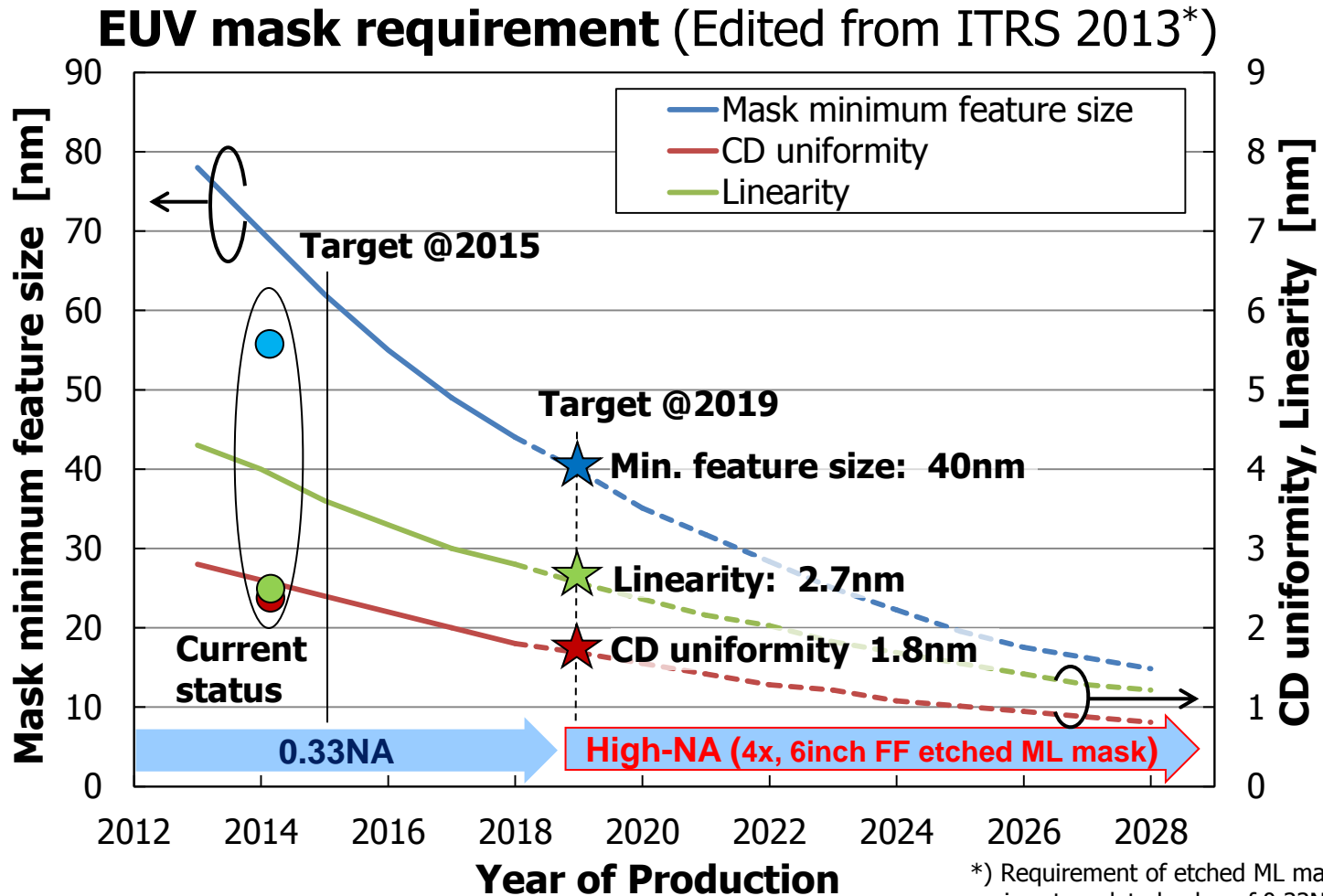
# CD Uniformity and Linearity of Etched 20ML Mask



	Target @2015(0.33NA)	Current Capability
CD Uniformity	$\leq 2.4$ nm	2.4 nm (120mm $\square$ ) 😊
CD Linearity	$\leq 3.6$ nm(CD 62nm up)	2.3 nm 😊

**Current etched ML mask CD performance catches up EUV mask requirement @2015.**

# Current Status and Outlook

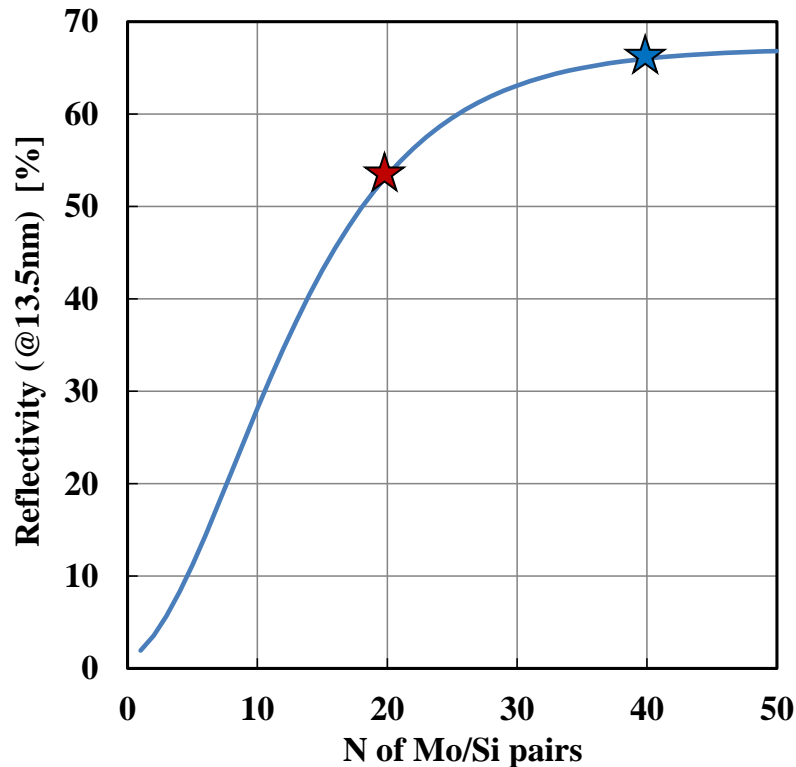


**Current etched ML mask CD performance catches up EUV mask requirement of 0.33NA @2015.**

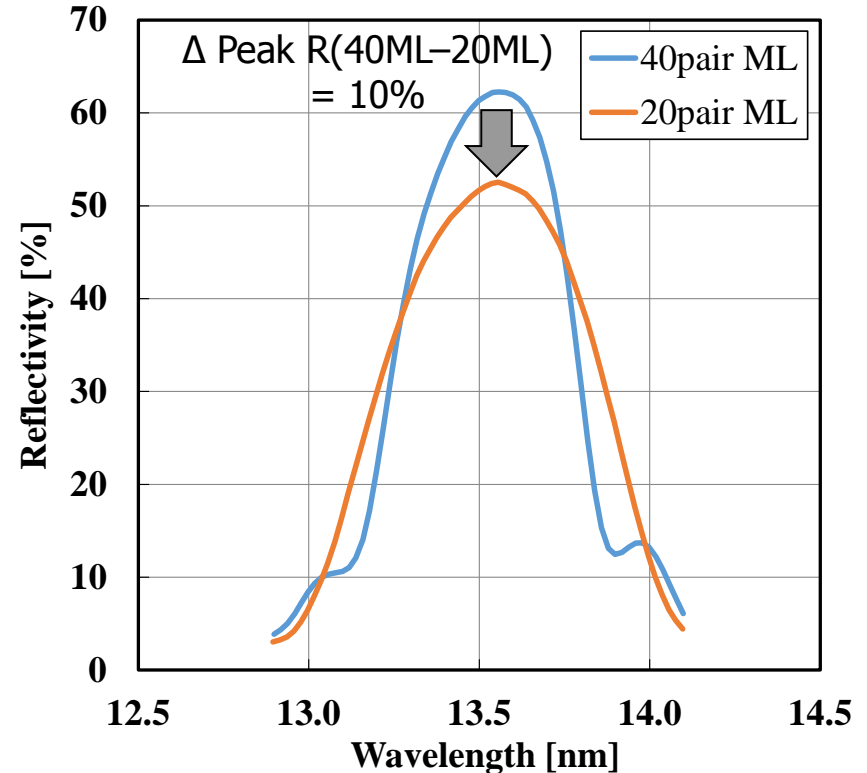
**Continuous improvement is required in order to apply etched ML mask to high-NA EUVL production.**

# EUV Reflectivity

**Simulated reflectivity as a function of number of ML pairs \***



**Measured reflectivity of Ru capped ML**



\*) ML intermixing model: N. Davydova et al., Proc. SPIE, 816624 (2011)

**EUV peak reflectivity loss is only 10% (abs.) by reducing the number of Mo/Si multilayer pairs from 40 to 20.**

**Lithographic performance needs to be evaluated from the viewpoint of EUV source power.**

# Summary

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- ✓ In order to improve durability against ML pattern collapse, thinner (20pairs) ML is evaluated. Dense ML trench, isolated ML trench of 40nm (10nm on wafer) and isolated ML line of 56nm (14nm on wafer) is achieved still after mask cleaning process.
- ✓ Current etched ML mask CD performance catches up EUV mask requirement of 0.33NA @2015.
- ✓ Continuous improvement of etched ML mask CD performance is required for high-NA.
- ✓ EUV peak reflectivity loss is only 10% by reducing 40ML pairs to 20ML pairs. Lithographic performance needs to be evaluated from the viewpoint of EUV source power.

**Etched ML mask is ready for 0.33NA experiments.**

# Acknowledgement

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The authors would like to thank Rikiya Taniguchi and Kazuki Hagihara of Toshiba for the discussion of mask metrology tools and their measurements.