Accelerating the next technology revolution

EUV Mask Challenges, Status, and Closing the Remaining Technology Gaps

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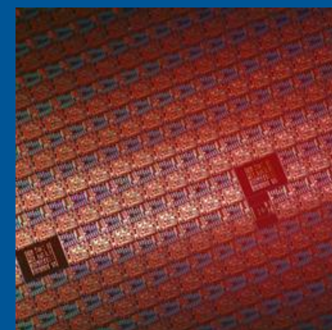

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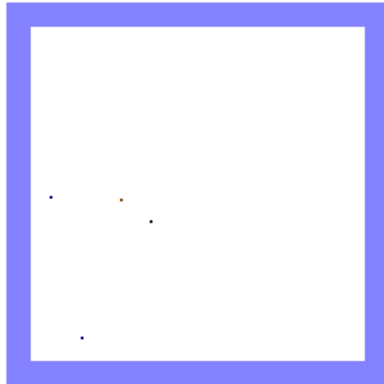
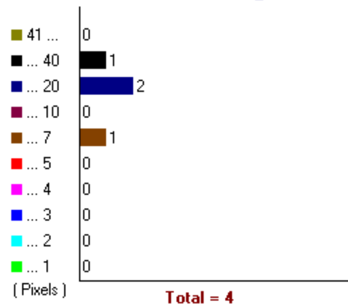
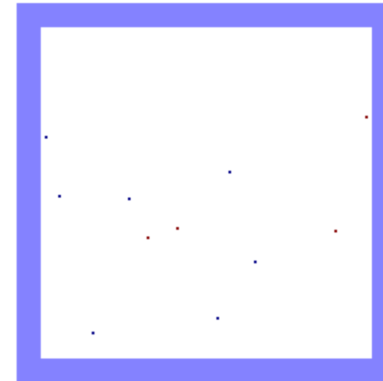
SEMATECH Champion Data

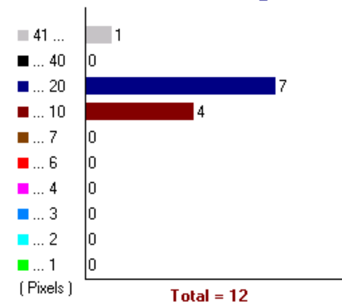
M1350





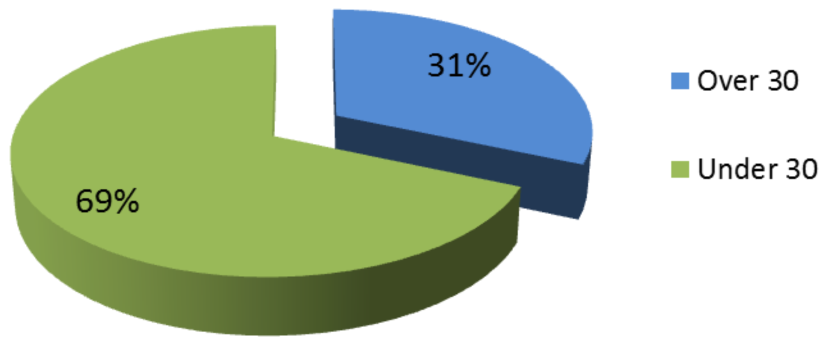
M7360 Dense Scan

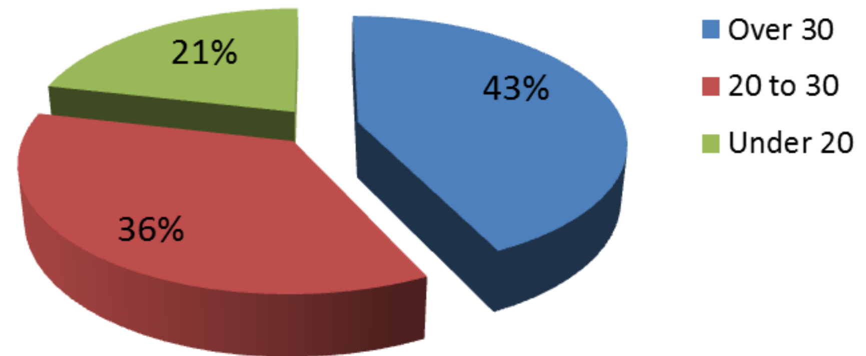




- Achieved 12 defects @ 45 nm or 8 defects @ 50 nm from M7360 inspection
  - 10 pits (from substrate), 1 handling defect, **1 defect from deposition**
- 65% reduction in defects from last year champion data (23 defects @50nm)

Yield analysis with M1350 (>70nm) and M7360 (>45 nm) [SiO_2 equiv.]





- Quality blanks: ~70% of yield below 30 defects >70nm from M1350
- 60% of Quality blanks have less than 30 defects >45 nm from M7360
- 20% of Quality blanks have less than 20 >45 nm from M7360

Mask Blank Defect Density Trend

Mask Blank Defect Density Trend (@73nm SiO2 equiv.)

Defect Density / Process Run

100.000
10.000
1.000
0.100
0.010
0.001

10/06/03
02/17/05
07/02/06
11/14/07
03/28/09
08/10/10
12/23/11

Date of Process Run

Defect requirements of device manufactures have changed

2015 Memory
2015 Logic
Memory HVM

Logic HVM

- 2015
  - Overall defect counts should meet requirements
  - Large size “Killer” defects still present
- HVM
  - Significant improvement needed to meet logic specifications
- Recent gains where made with the substrate
  - Reduction of cleaning induced defects
  - Substrate quality improvement at suppliers
- Process yields are not good

Substrate challenges

- Approximately 60%-65% of total mask blank defects originate from substrate defects
- Meeting simultaneously: substrate finish, figure (flatness), roughness and defect specifications is a significant challenge
  - Substrates are amorphous in nature, making it difficult to control CMP
- Reaching figure and finish specifications requires several iterations between global and local polish
  - This creates defects such as scratches or embedded particles
- The surface physical and chemical properties are modified by the polish steps and do interact with the cleaning processes
  - Tight management and control between final polish and cleans to ensure cleaning does not introduce additional defects

Substrate Defects

- Defect signature is different between suppliers
- Majority of substrate defects are not detection during inspection
  - Majority only become visible after ML deposition through decoration
  - Decoration through ML deposition is of limited value
    - Adds to cycle time and reduces learning cycles
    - Adds complexity to data analysis
- Will require substrate inspection capability
  - Current technology not able to detect sub-35nm pits (SiO2 equiv.) or shallow scratches
  - Plans for actinic inspection tools for mask blanks will not address this gap

EUV Substrate Gaps

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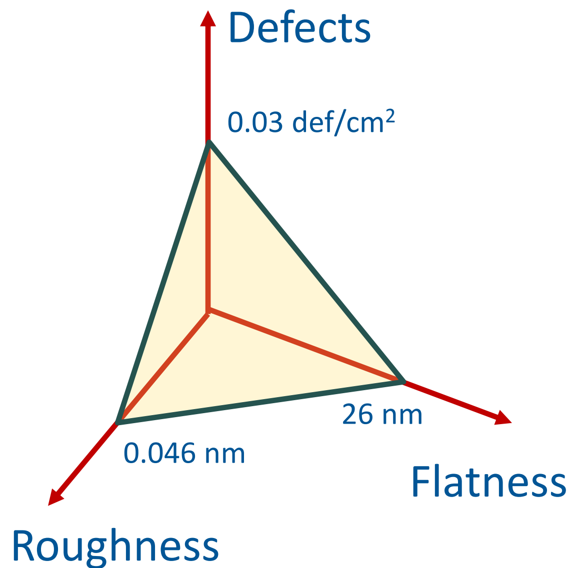
- Defect levels, roughness and flatness specifications must be met for successful EUVL implementation



EUVL Substrate Requirements @22 nm HP node	Specification	Source	Current Status
Defect size	30 nm	ITRS 2011 Update	**0 defects @ 40 nm+**
Defect density	0.03 def/cm2	SEMI standards, 2009 update	**0 defects @ 40 nm+**
Roughness	0.046 nm	P. Naulleau, LBNL	~0.05 nm
Flatness	26 nm PV	ITRS 2011 Update	**80-100 nm typical**
Local Slope	1.8 microradians	ITRS 2011 Update	No issues

Mask Blank ML Deposition Challenges

- Approximately 20%-25% of total mask blank defects are deposition related
- Mask blank defectivity requirements have not yet been demonstrated
  - Large “killer” defects are a significant problem
    - Prohibits implementation of defect mitigation schemes
    - Comes from deposition tool and process
    - Detected on each mask blank SEMATECH has measured
  - Defect counts are close to meeting memory and pilot line logic requirements
    - Requres ~4X improvement to meet logic HVM specifications
- Deposition process yield
  - Quality deposition region is only 10%, at best, of overall process run
  - Target surfacing and burn-in critical

Tool and Process Limitations

- Limitations of deposition chamber and process
  - Overspray of ion source
  - Substrate Handling
  - Process yield, significant number of deposition cycles required to reach quality deposition region
  - Small process window for reflectance uniformity
  - Shield surfaces
  - Proximity of substrate to shields
- New Deposition Tool is Required
  - Cleaner, less divergent ion source
  - Chamber with a larger volume
  - New substrate location
    - May require flexibility to move substrate to multiple positions
  - Cleaner handling of substrates and mask blanks
    - May require dual pod solution

Optimized Ion Beam Profile For Defect Reduction

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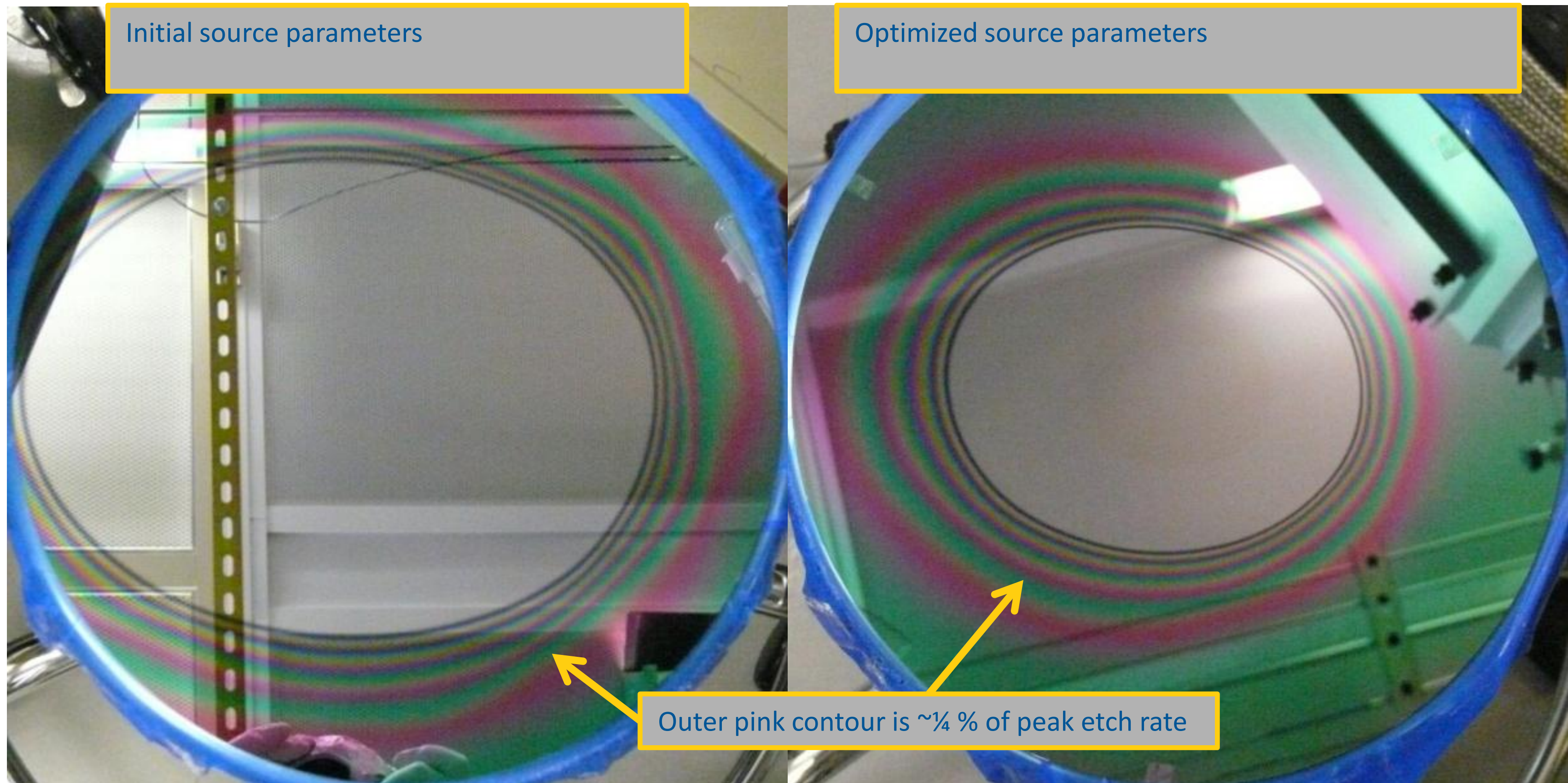


- Higher operating voltages/currents can give narrower focus on target
- New parameters give < ¼ % of peak etch at edge of target
  - Does not completely eliminate sputtering of shields

EUV Mask Blank Gaps

- Defect levels, roughness, and reflectivity

EUVL Mask Blank Requirements @22 nm HP node	Specification	Source	Current Status
Defect size	18 nm	ITRS 2011 Update	**12 defects @ 45 nm+**
Defect density	0.002 defects/cm2	Device Manufactures	**0.043 defects/cm2**
Roughness (rms)	0.05 nm	Defect Metrology	~0.14 nm
Reflectivity	65%	ITRS 2011 Update	63%-64%

Mask Blank Roadmap

2011				2012				2013				2014				2015			
Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4

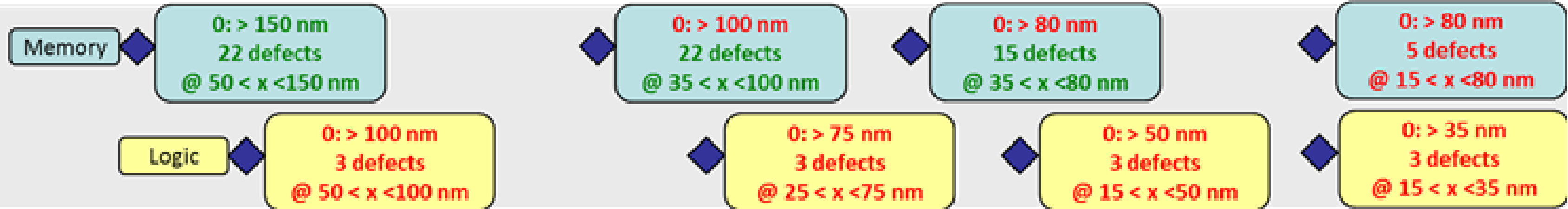
Pilot start

HVM ramp

HVM start

Blank defects

Industry Need



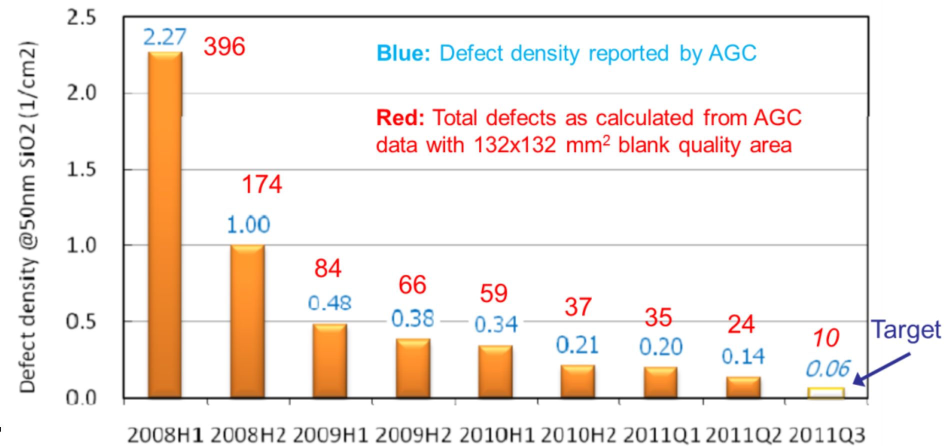
Tool Capability

High Level Requirements for Actinic Blank Inspection

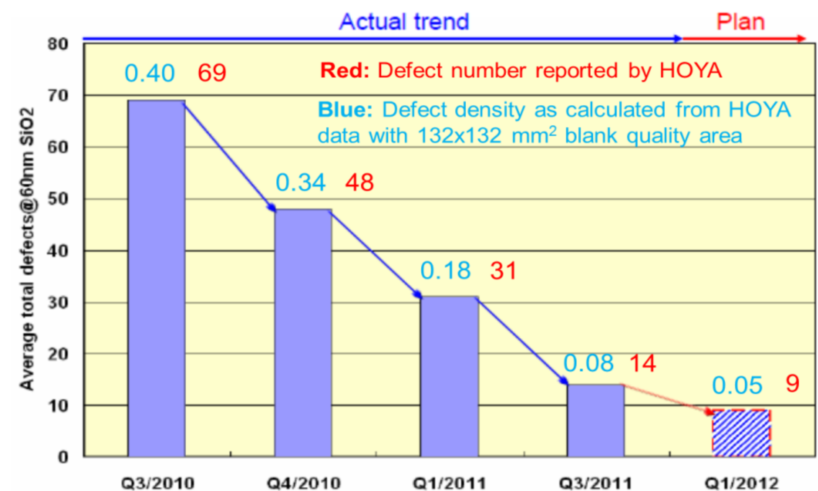
- Inspection requirements:
  - Substrate pits/bumps (phase defects) must be detected
  - Particles, even just under the capping or top multilayers (amplitude defects) must also be detected
- Classification and review requirements:
  - Review should accurately localize the defects so mitigation by pattern shifting can be used.
  - Defects should be classified, and near the sensitivity limit, reviewed to determine printability

Defect Trends of Suppliers

- Defect trends of mask blank suppliers are improving
- However, delivered mask blanks will have some defects
- Defect printing mitigation methods will be needed



AGC: from 2011 EUV Symposium



HOYA: from 2011 SPIE Adv Litho

Mask Layout Pattern Shift

- Position design layout so that all mask blank defects remain covered by the absorber
- Remaining questions:
  - Probability of eliminating all blank defects using pattern shift
  - Potential impact on field size
  - Allowed defect count and size distribution
- Successful pattern shift requires:
  - Excellent coordinate accuracy
  - Low-defect fiducial process
  - Infrastructure for sorting blanks and matching to mask patterning
  - All printable defects need to be detectable

Current EUV Mask Technical Gaps

- Challenges with defects continue:
  - Substrate Defects
    - Defects become visible after deposition
  - Multi-Layer Deposition
    - Killer defects from ML deposition still an issue
    - Low process yield
  - Defect free EUV masks
    - Mitigation of mask blank defects will be required
  - Metrology
    - What inspection capability existing is running out of steam
    - Inspection tools required to meet HVM requirement are not available
- Infrastructure
  - New generation of ML deposition tool is needed
  - Metrology and inspection tool development required

Closing the Gaps

- Mask blank suppliers maintaining their current roadmaps
- Consortia and Mask Blank Suppliers continue to work on EUV development
  - Substrate polishing and cleaning
  - ML Deposition tool and process optimization
- Consortia and Tool Suppliers are addressing tool gaps
  - Inspection tools
    - Mask Blank (substrate?)
    - Pattern Mask
  - Deposition
    - Next generation IBD tool
- Pre-production exposure tools
  - Increasing mask manufacturing cycles of learning
  - Driving focus on process yield across all areas of mask manufacturing
    - Lack of metrology tools demands wafer print for process and defect verification which is slowing learning
- Increased focus by industry on addressing HVM needs

Thank You

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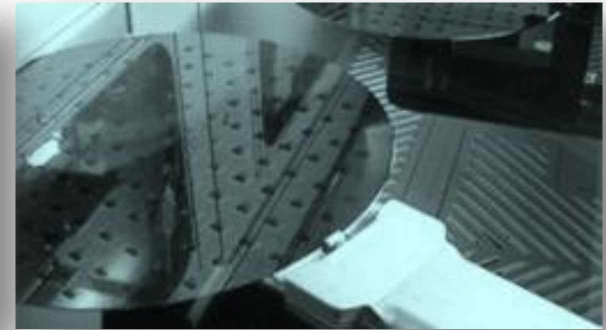
Research

Development



Manufacturing