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EUV Mask Defect Reduction : Status and Challenges

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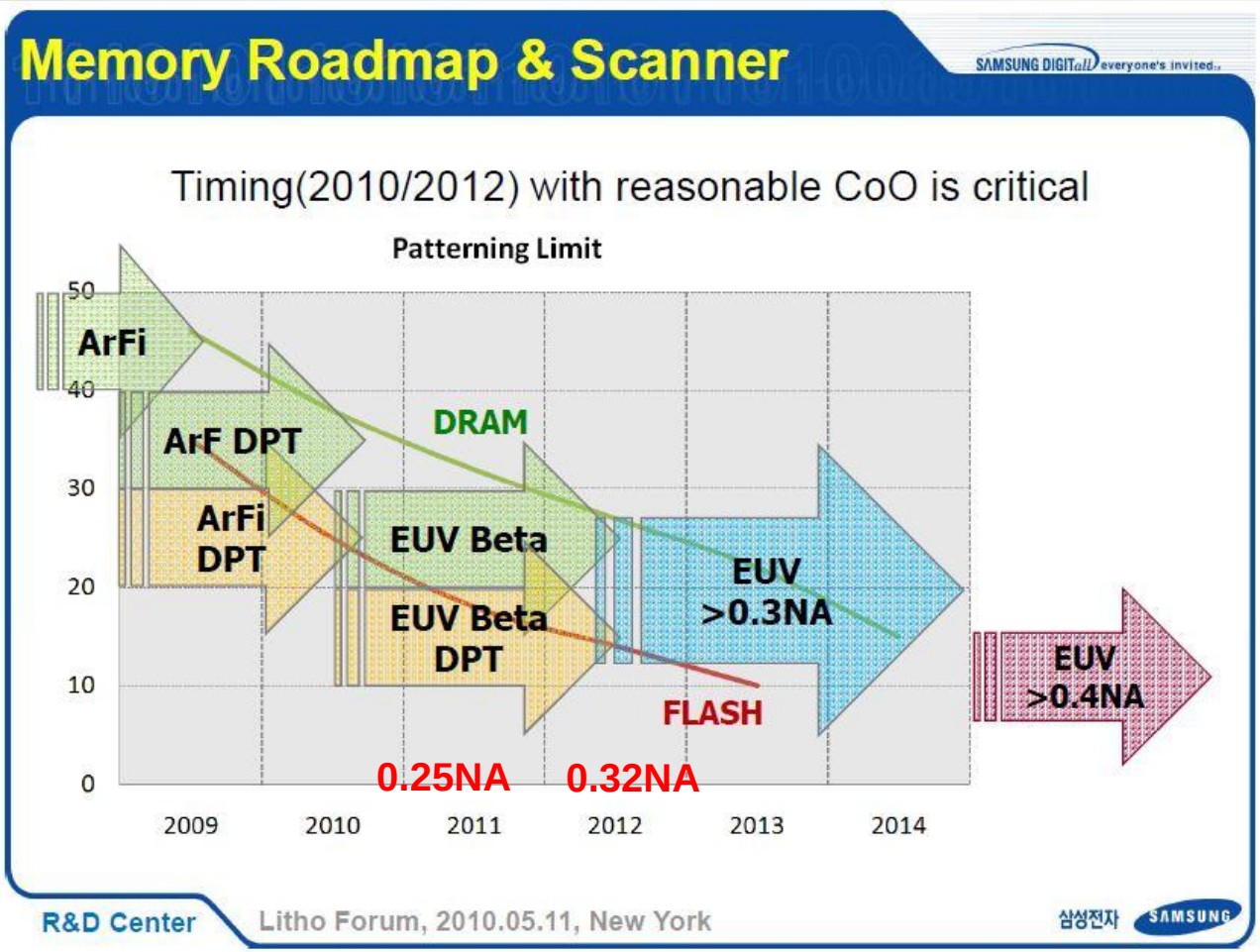
SAMSUNG DIGITall
everyone's invited™

Outline

- Background
  - Device Roadmap, EUV mask defect type
- Current Status of EUV mask defect and Technical Challenges
  - Defect Characteristics
  - Defect Density and Defect Pareto Analysis
  - Blank, Resist, Etching, Cleaning, Repair, Inspection, Defect Verification
  - Mask Defect Disposition, Mask Qualification
- Prospect of EUV Mask Defect Reduction
- Summary

EUVL Roadmap for Memory



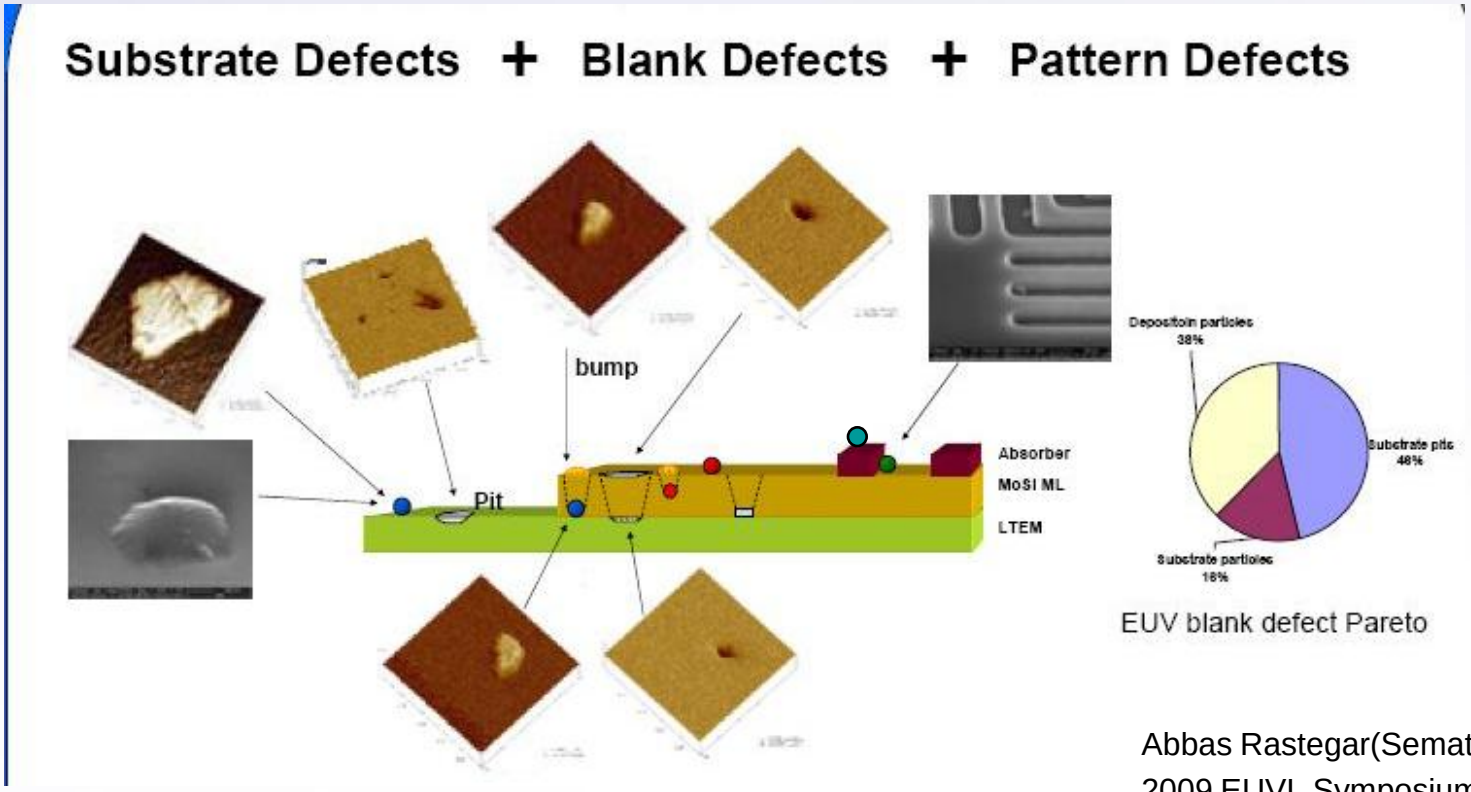
30nm HP DRAM

- 2010 for Device development
- 2012 for HVM

- Mask Defect Readiness (2011) for HVM

Jungho Yeo (Samsung), 2010 Litho Forum

EUV Mask Defects



Abbas Rastegar(Sematech), 2009 EUVL Symposium

- **Complicated**
- **Difficult to trace**

Getting worse !

EUV Focus Areas 2005-2009

2005 / 32hp	2006 / 32hp	2007 / 22hp	2008 / 22hp	2009 / 22hp
1. Resist resolution, sensitivity & LER met simultaneously	1. Reliable high power source & collector module	1. Reliable high power source & collector module	1. Long-term source operation with 100 W at IF and 5MJ/day	1. Mask yield & defect inspection/review infrastructure
2. Collector lifetime	2. Resist resolution, sensitivity & LER met simultaneously	2. Resist resolution, sensitivity & LER met simultaneously	2. Defect [illegible] infrastructure	2. Long-term reliable source operation with 200 W at IF
3. Availability of defect free mask	3. Availability [illegible]	[illegible]ity of defect free mask	3. Resist resolution, sensitivity & LER met simultaneously	3. Resist resolution, sensitivity & LER met simultaneously
4. Source power	4. Reticle protection during storage, handling and use	4. Reticle protection during storage, handling and use	• Reticle protection during storage, handling and use	• EUVL manufacturing integration
▪ Reticle protection during storage, handling and use	5. Projection and illuminator optics quality & lifetime	5. Projection and illuminator optics quality & lifetime	• Projection / illuminator optics and mask lifetime	
▪ Projection and illuminator optics quality & lifetime				

Steering Committees of 4th-8th International EUVL symposia, 2005-2009.

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EUV Mask Defect Questions

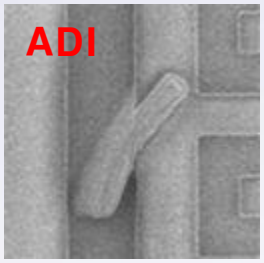
- **Many ?**
  - **What do defects on EUV mask look like?**
  - **How serious is it ?**
  - **Defect density @ blank, @maskmaking**
  - **Portion of blank defects from entire mask defects**
  - **Is it repairable ?**
  - **Is it inspectable ?**
  - **Is it acceptable for device development, HVM ?**
  - **Target for development and HVM**
  - **…….**
  - **……..**

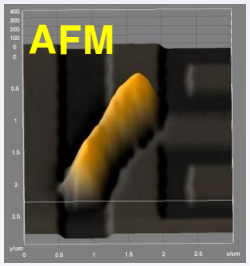
- **For last couple of months, we analyzed defect pareto from blank to mask process based on initial development stage.**

Defect Images

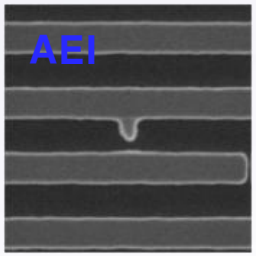
- process step -

Blank

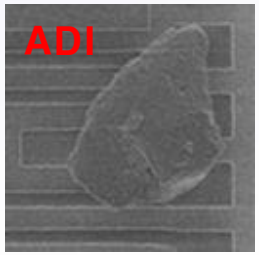


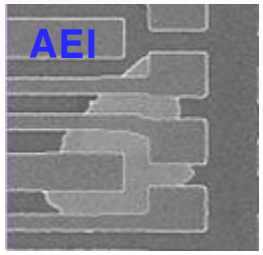


Resist

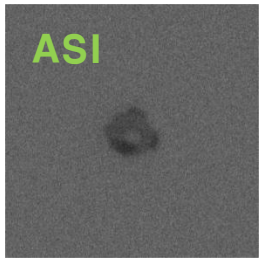


Etch





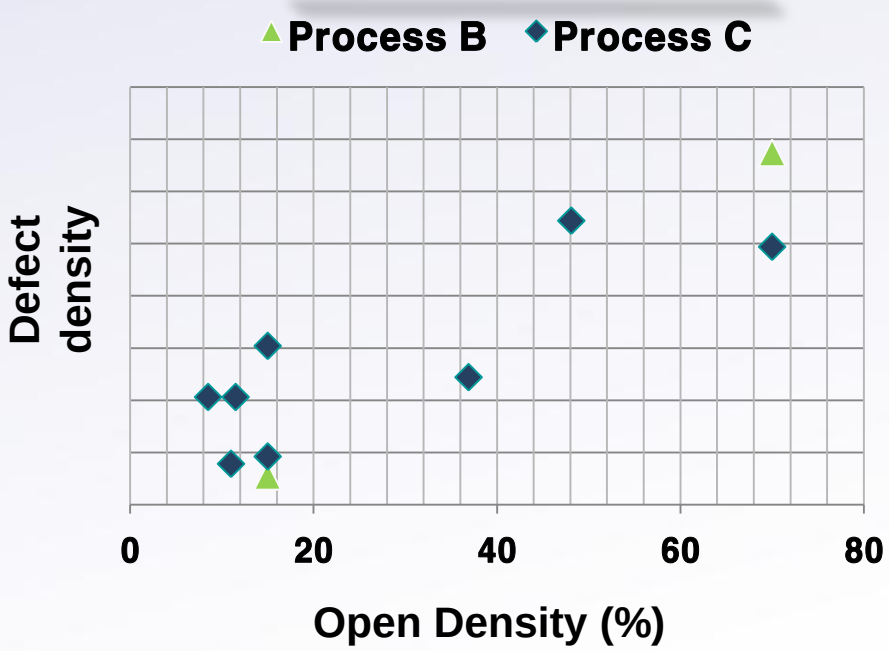
Cleaning



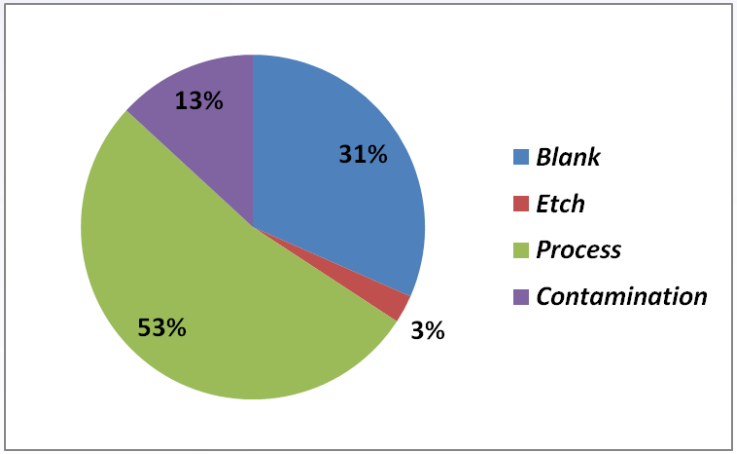
- Defect Images show various defect sources from blank to mask patterning.

Defect Density & Defect Pareto Analysis

Defect Density



Defect Pareto



- 30nm HP
- Blank inspection @M1350
- Mask inspection @19X tool
- Defect Density : 0.39 defects/cm^2

- Defect density depends on open density.
- Achieved 0.39 defect density including blank & pattern with pattern mask inspection.
- Continuous improvement is still in progress.

Technical Challenges of EUV Mask Process for Defect Reduction

Blank

- Substrate (pit, bump)
- ML, Absorber (particle)
- Resist (particle)
- Late learning cycle due to the lack of inspection and printability

Resist

- New resist
- New surface

Etch

- New material
- New gas
- New process
- long term stability

Cleaning

- PRE, adders
- Surface damage
- Carbon contam.
- Backside contam.
- lack of inspection

Inspection

- Lack of wavelength
- Sensitivity
- Tool timing for HVM

Repair

- New material
- Capping damage
- lack of selectivity
- Undercut
- Depth control

Defect Verification

- Lack of wavelength
- TAT
- Verification rule

EUV Mask Blank

- Technical challenges -

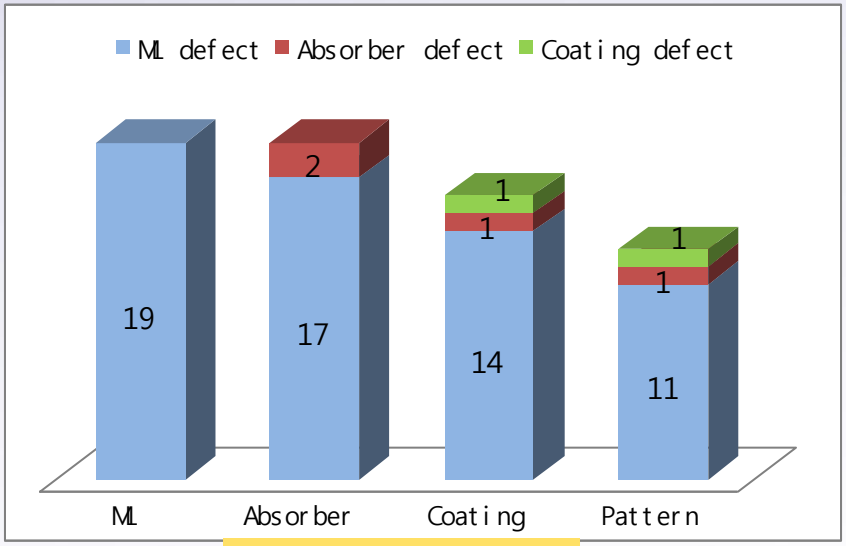
- Responsibility : Provide defect free blank mask to mask makers
- Status : Still behind schedule in terms of technology and timing for HVM

- Multilayer Defect Specification for DRAM

	2009	2010	2011	2012
Defect Density (ea/plate @25nm)	800	160	40	10
Converted # (ea/plate @70nm)	40	8	2	0.5

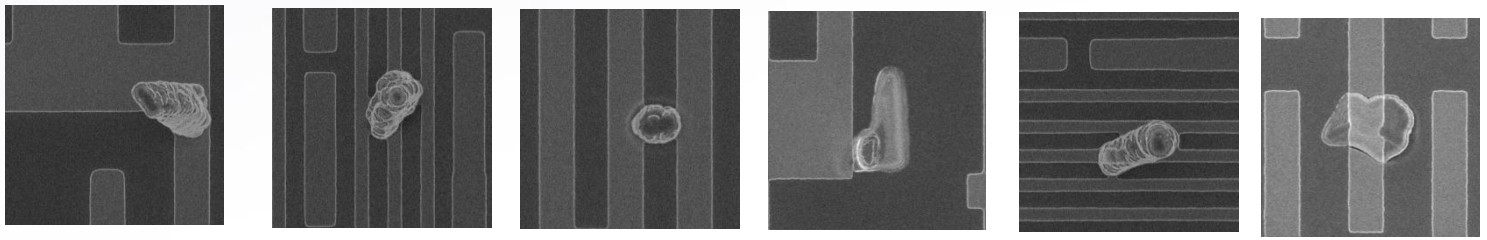
- Considerations
  - Need continuous improvement of EUV mask blank (blank suppliers)
  - Defect avoidance using navigation of defect location (mask makers, blank suppliers)
  - Relaxation of defect specification based on printability (mask makers, blank suppliers)
  - New tool development for blank inspection (blank suppliers, industry-funding)
  - Defect tracing from blank defect to wafer printing (blank suppliers, mask makers)

Examples :
EUV Mask Blank Defect Analysis



- Design node : 30nm HP
- Mask pattern area : 100cm^2
- ML inspection : M1350
- Absorber inspection : M1350
- Coating inspection : M2351
- Pattern inspection : 193nm

ML defects (Mask SEM)



- ML defect shows complex topography on mask and will be difficult to be repaired.
- ~40% of ML defects were transferred on pattern defect.
- Absorber, Coating process also should be well taken care of.

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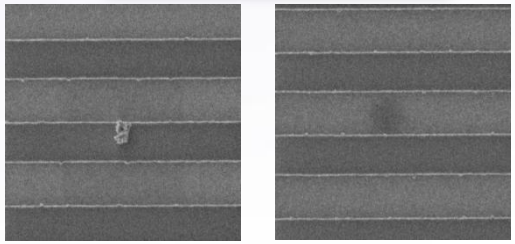
Resist Process

- Technical challenges -

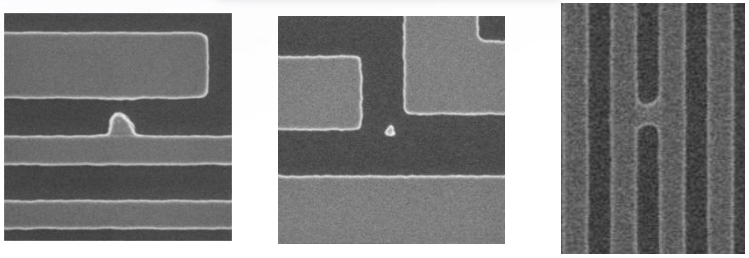
- Considerations
  - New resist but it will be minor change
  - New surface characteristics (Ta-based)
  - New coating process due to different surface characteristics
  - Repairable defect or not
  - Defect versus film loss & CDU impact

Resist defect images

After develop



After etching



- Similar to optical mask defect

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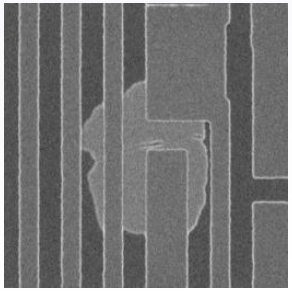
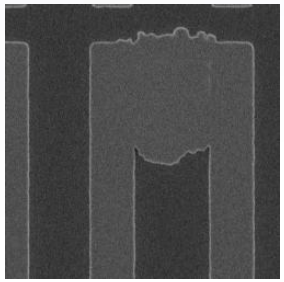
Etching Defect

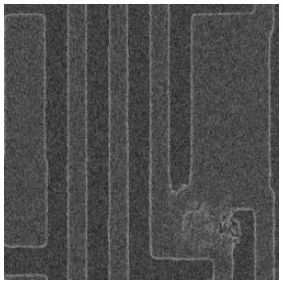
- Technical challenges -

- Considerations
  - New etch processes (single or combo)
  - New gas, material reaction
  - Long term stability (need more statistics)
  - No more benefit of overetch
  - Need to protect thin capping layer
  - Repairable defect or not

Defect from Etching







- For EUV mask etch, defect type and defect density are also similar to optical mask but will need more statistical data due to new gas & material reaction.
- Large defect from etch will be critical because of repair difficulty.

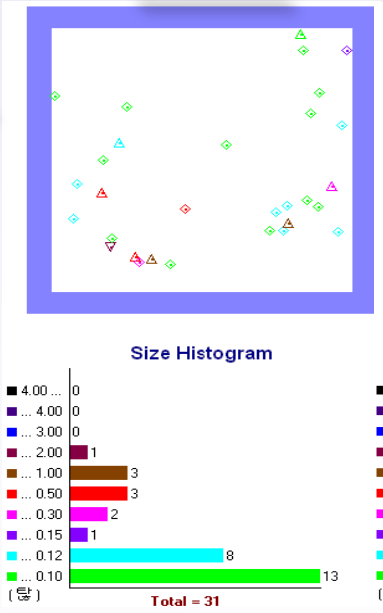
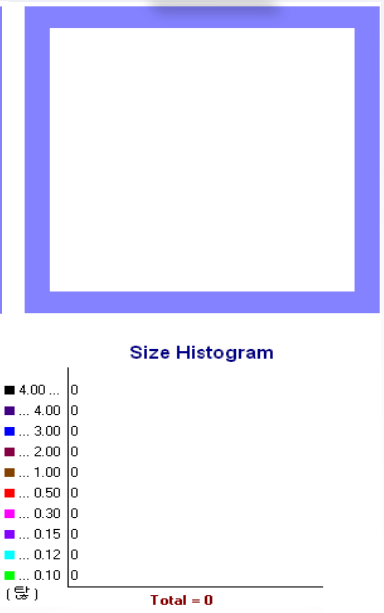
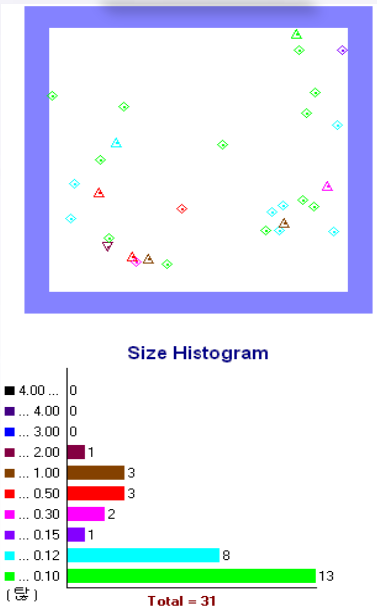
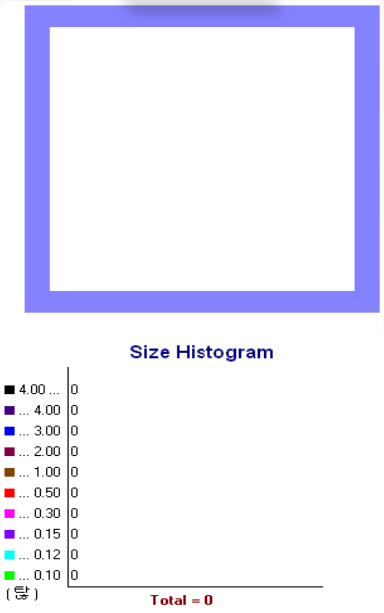
Mask Cleaning
- Technical challenges -

- Considerations
  - Higher PRE, zero Adders
  - Pattern damage free process is required down to ~75nm(4X).
  - Thin capping layer should be well protected after multiple cleaning.
  - Resist strip capability needs no cross-contamination of backside of mask.
  - Mask life time should be evaluated over the time.
  - Carbon contamination should be removed without any loss of EUV reflectivity.

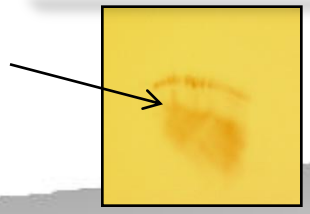
- Current status
  - Shows good PRE, possible for zero adder
  - Manageable pattern damage @75nm for EUV node
  - Good durability of Ru capping (~2.5nm)
  - Successful removal of carbon contamination

PRE & Carbon contamination

Best PRE on Ru surface shows 100% of native particle and zero adders

	initial	final	removed	adder
M2351				

Carbon contamination was removed

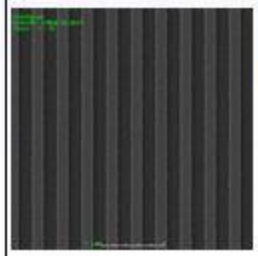
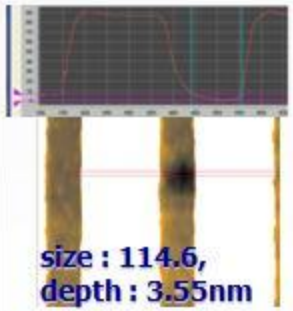
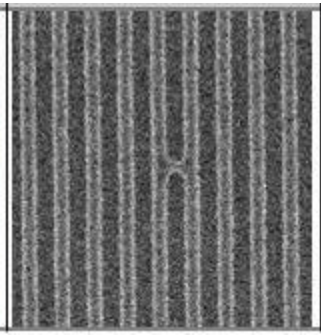
Before cleaning	After cleaning
	

Carbon Contamination

Inspection
- Technical challenges -

- Goal : BI + PI + WI → 100% capture rate of mask defect

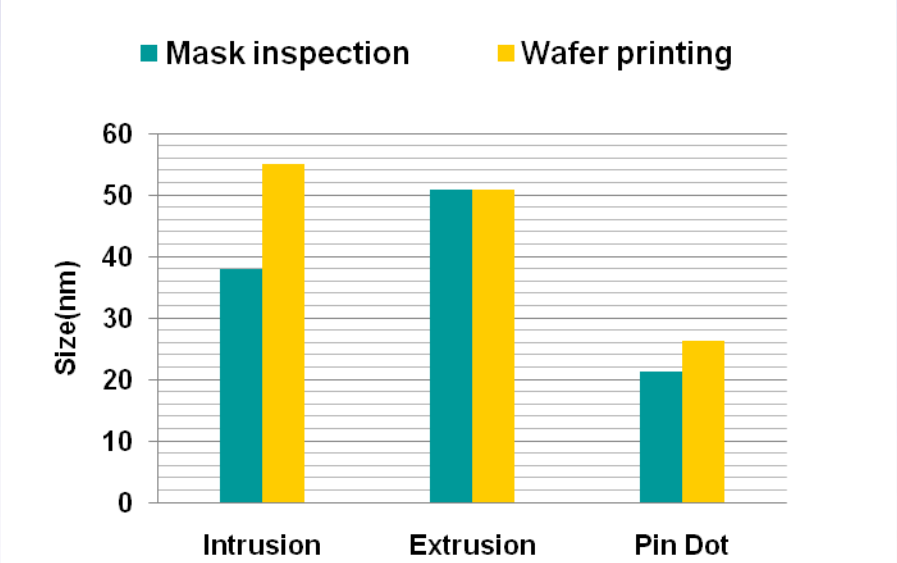
- Blank Inspection (BI)
  - Need more capability for phase defect & smaller amplitude defect
  - Timing is critical for device development & HVM

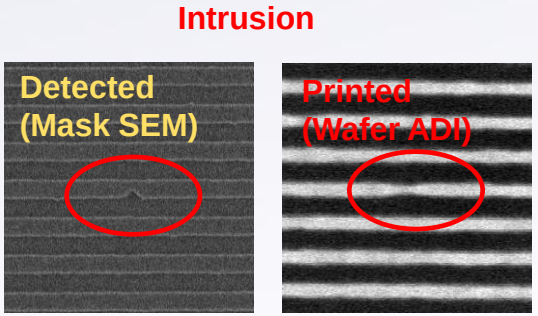
	Blank inspection	Mask inspection	SEM (mask)	AFM (mask)	SEM (wafer)	Wafer inspection
Shallow blank defect	Not detected	Not detected				Detected

See Sungmin Huh's "Printability and Inspectability of Programmed and Real Defects on the Masks in EUV Lithography" *in Mask 2 Session Oct 20(Wed), 2010*

Inspection

- Technical challenges -





- 30nm HP
- 193nm mask inspection
- TaBO/TaBN/Ru/ML

- Pattern inspection (PI)
  - Mask inspection tool detects most of printing defects on wafer for PDM.
  - Need more optimization for more various defect types & sizes for native pattern defect
  - Extendibility of 193nm and need of new e-beam inspection also should be reviewed between 22nm and 16nm HP.
  - Beyond 16nm HP, actinic inspection will be promising solution.

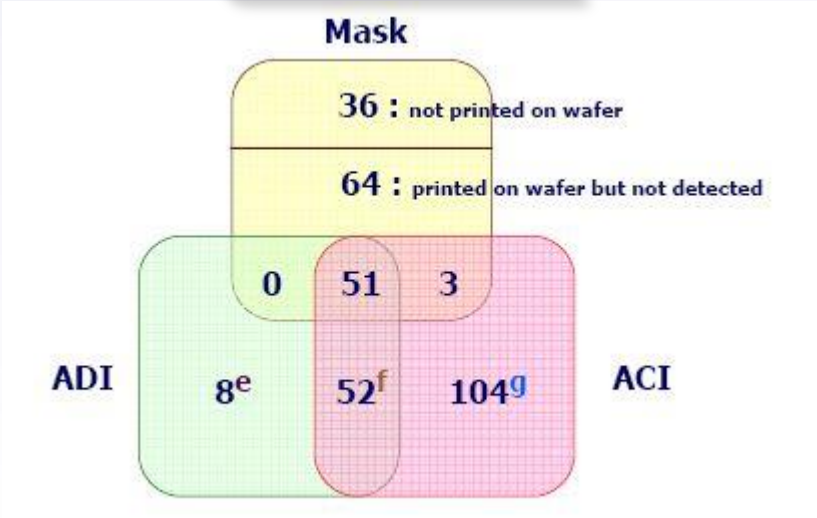
Inspection
- Technical challenges -

- Wafer inspection (WI)

ACI inspection > ADI inspection
SiN stack wafer > Oxide stack wafer

KY Cho(Samsung), 2009 EUVL Symposium

HP 50nm L/S

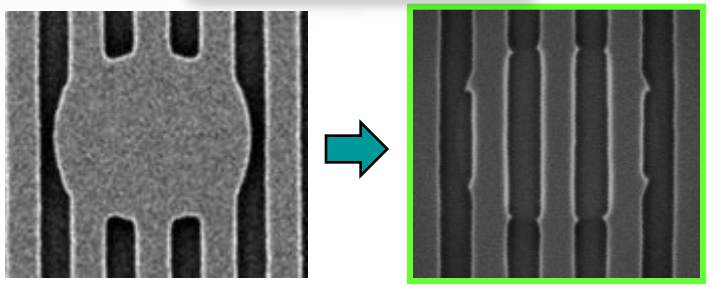


- Tools for mask defect disposition, repair verification & mask qualification
- Technology gaps for complex pattern & certain type of mask defect
  - E-beam technology need to be evaluated to close the gap
- Review SEM vs CD SEM for mask qualification

Defect Repair
- Technical challenges -

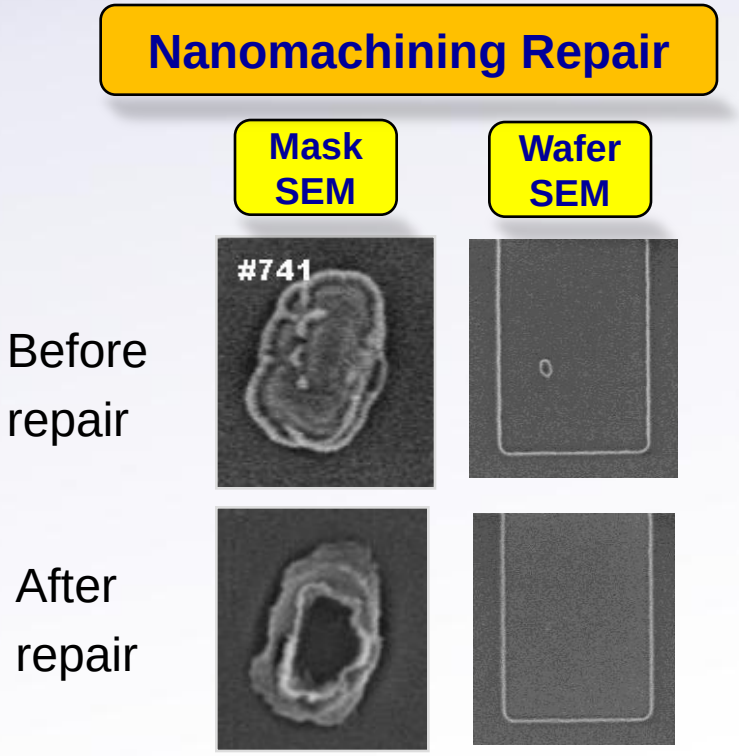
- Considerations
  - New materials (Ta-based, Ru)
  - New gas chemistry needed (currently XeF2, H2O)
  - Undercut, Ru damage, spontaneous reaction of non-repaired area
  - New criteria (protection of thin capping layer)
  - Precursor, passivation, gas flow → need more controllability
  - Blank defect repairability (absorber defect due to ML defect)
  - Extendibility of new materials for HVM
  - Depth controllability of nanomachining

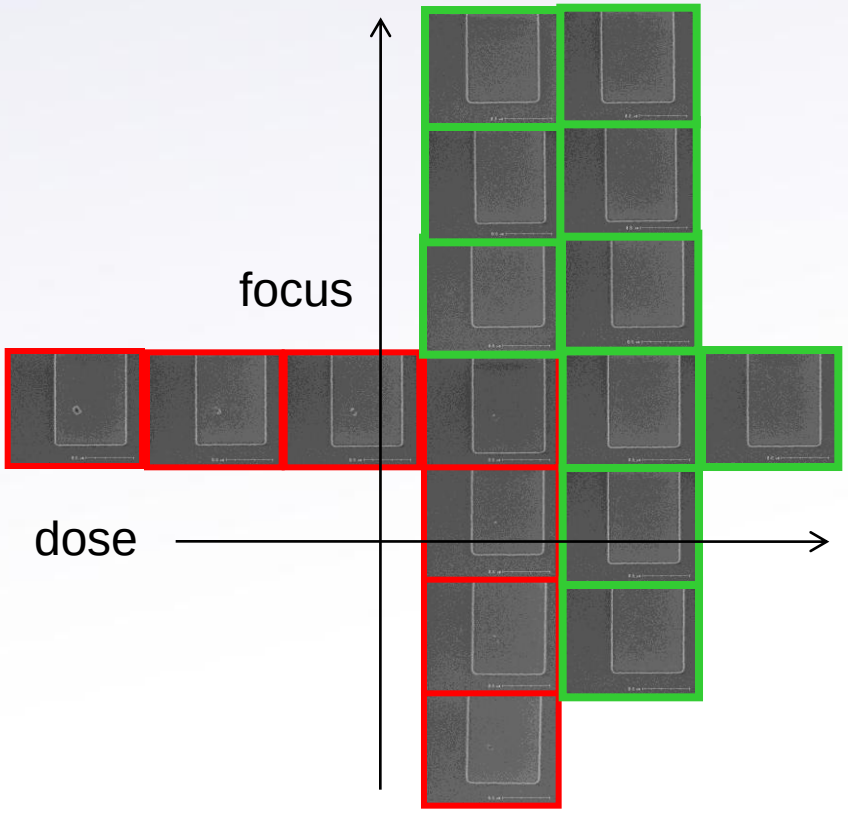
E-beam Repair



- 30nm HP
- Large absorber defect repair for programmed defect (TaBO/TaBN/Ru/ML)
- Repair tool : MG45
- Need more study with sloped defect

ML-induced defect repair on Absorber





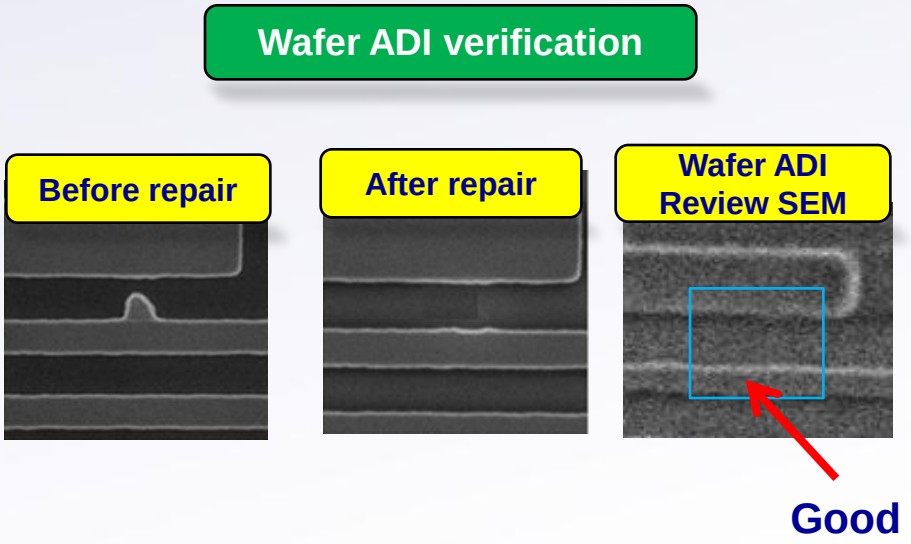
- Feasibility test with nanomachining repair of ML defect was done.
- Non-printable within 100nm of DOF
- Need more study how to handle ML-induced absorber defect

Mask Defect Repair Verification

- Technical challenges -

- EUV AIMS
  - Timing for HVM
  - Extendibility of NA
- First verification with SEM/AFM after repair
  - Development stage
  - Depends on defect type thus will not be satisfactory
- Alternatives before EUV AIMS introduction
  - Wafer printing is only the option
- Considerations of Wafer Printing Verification (wafer inspection)
  - Inspection capability of repeating mask defect (defect type, pattern type)
  - Inspection step (ADI, ACI)
  - Dose/focus check rule
  - Feedback TAT from wafer printing to mask maker

Wafer ADI & ACI for repair verification



- Simple extrusion defect repair(30nm HP) is verified at ADI step.
- Need to decide defect verification step considering pattern type, defect type and inspection capability
- Local CD error from repair process might not be differentiate from LER on wafer

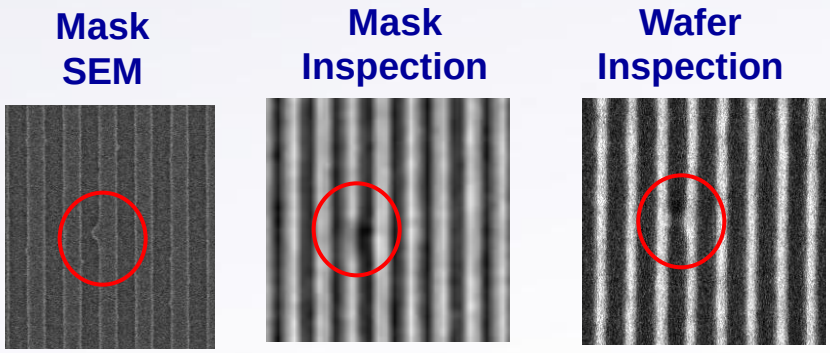
Mask Qualification

- Key focus : phase defect, mask inspection, defect repair, wafer inspection

	Mask Inspection	Mask Repair	Wafer Inspection (ADI)	Wafer Inspection (ACI)	Mask Qual.	What do we need?
Ideal (optical)	Detected !	Repaired	No detection (no defect)	No detection (no defect)	Good Mask	Mask inspectability Mask repairability
Based on printability	Detected !	No repair (non-printable)	No detection (non-printable)	No detection (non-printable)	Good Mask (?)	Printability Library (defect skip rule)
Worst case (pattern defect)	No detection	No repair	Detected !	Detected !	NG Mask	Mask inspectability Wafer inspectability
		Repaired	No detection (no defect)	No detection (no defect)	Good Mask	Mask repairability Wafer inspectability
Worst case (phase defect)	No detection	No repair	Detected !	Detected !	NG Mask	Blank capability Phase defect repairability(?)
Worst case (large ML bump)	Detected !	No repair	No detection (lack of inspectability)	No detection (lack of inspectability)	??	Wafer inspectability

Wafer inspection / printing & Mask Qualification

HP 30nm



- For real defect, chance of mismatch of mask inspection and wafer inspection / printing
  - Mask Qual. Issue
- Wafer printing might not be final tool for mask qualification.
  - Need more improvement of mask inspection to screen defects
- Need more study to fix mask qualification rule

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Prospect of EUV mask defect reduction @ 30nm HP

	Severity	Areas to focus on
Blank	High	ML defect reduction (suppliers) Determining of realistic defect spec. (mask makers)
Resist	Mid-Low	Study of new surface interaction
Etching	Mid-Low	Need more statistics, more lots, long term stability
Cleaning	Mid-Low	Durability, more smaller particle
Blank Inspection	High	Need phase defect inspectability
Pattern Inspection	Mid-Low	Optimization of 193 nm inspection New tool need to be developed in time for HVM
Wafer Inspection	High-Mid	Need more matching test with mask inspection
Repair	Mid-Low	Technology of high selectivity exists. Need more feasibility of ML defect repair.
Defect Verification	High	new tool need to be developed in time for HVM
Defect Disposition	High-Mid	Fast TPT to judge mask defect via wafer inspection. Need wafer inspection improvement & EUV AIMS.
Mask Qualification	High-Mid	Need more study of defect printability & device performance

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- Current Status of EUV mask defect and Technical Challenges
  - Defect Characteristics
  - Defect Density and Defect Pareto Analysis
  - Blank, Resist, Etching, Cleaning, Repair, Inspection, Defect Verification
  - Mask Defect Disposition, Mask Qualification
- Prospect of EUV Mask Defect Reduction
- Summary

Summary

- We reviewed EUV mask defect issues from blank to patterning @ 30nm HP.
- Quality of EUV blank is biggest concern and needs to be continuously improved and practical requirement also should be revised to deal with slipping of blank roadmap for both development and HVM of device.
- Process defects from resist & etching need to be carefully monitored with more statistical data during mask fabrication.
- Mask cleaning shows good performance so far but still concern should be focused on mask lifetime over the time.
- Inspection is most critical step for entire mask defect reduction.
  activity, especially for blank inspection. 193nm pattern mask inspection will be likely no issue for EUV mask @30nm HP.
- Defect disposition will be time consuming due to need of printability feedback.
- Mask defect repair shows also good performance for small Programmed defect but more study should be followed with practical pattern defects which have topographical shape.
- Procedure of mask qualification will be troublesome to judge good/NG mask decision.
- Wafer inspection capability also carefully need to be reviewed to help mask defect verification and mask qualification.

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Questions ?