Systematic Quantification of Flare Mitigation Strategies

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[1]On assignment from Intel

[2]On assignment from Samsung

[3]IMEC

Outline

- Introduction
- Flare compensation design mask
- Long range and short range flare
- Interaction between flare ranges
- Rule-based flare mitigation strategy
- Full-chip flare map calculation
- Experimental validation
- Conclusions

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What is Flare?

- **Flare** is the loss of contrast due scattering of light from the bright regions of the image plane into the dark regions
- Flare is caused by mirror roughness with spatial wavelengths in the range of 1mm to 1μm
- Flare is proportional to $1/\lambda^2$
- ADT flare expected to be 16%
- The **point spread function** (**PSF**) describes the response of an imaging system to a point light source

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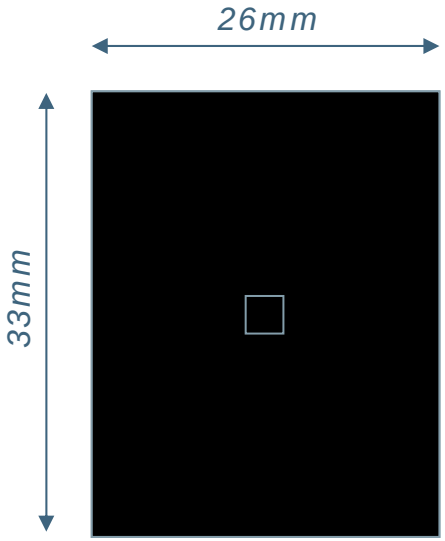
Introduction



1 mm Window	33 x 26 mm Reticle	Flare (%)
Clear	Clear	16.2
Dark	Clear	9.2
Dark	Dark	0.5

Results obtained using Solid-EUV

- **Flare has a very long range**
- **Standard local flare compensation strategies (< 1mm) will not work**
- **The development of computationally efficient and accurate flare compensation methodology is required**

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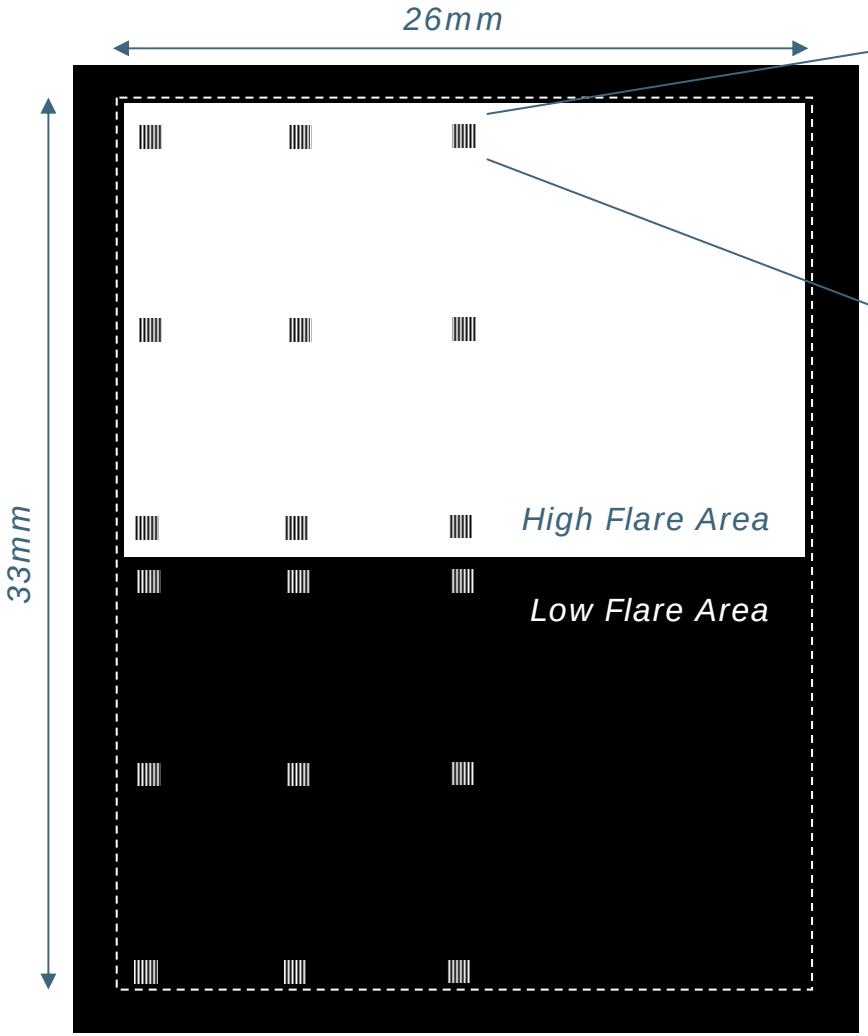
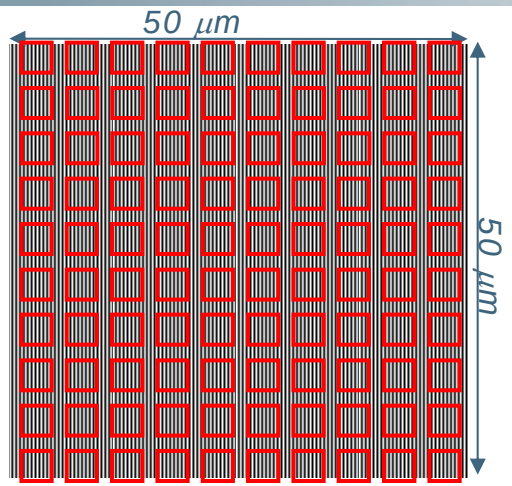
Flare Compensation Design Mask





40nm DL 1:1

- 5 μm step: 1800 Locations
- 25 μm step (162 locations)
- 1 μm step (45,000 locations)

- Mask design for simulation only
- Design chosen because it can be loaded in:
  - Rigorous Simulator (SOLID-EUV)
  - Standard EDA software

- **CDU can be used to quantify the quality of the Flare compensation strategy**

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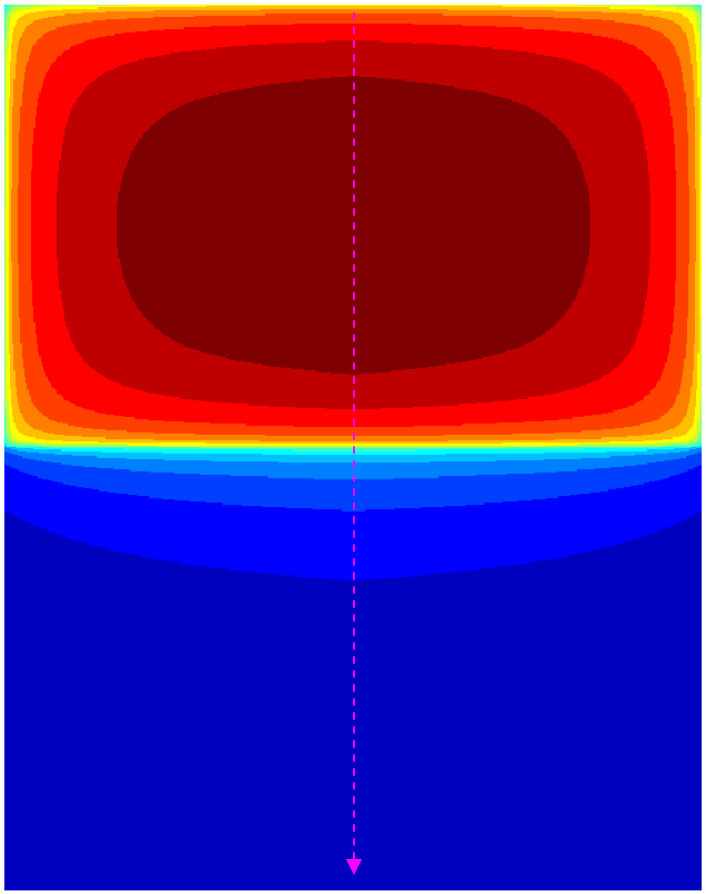
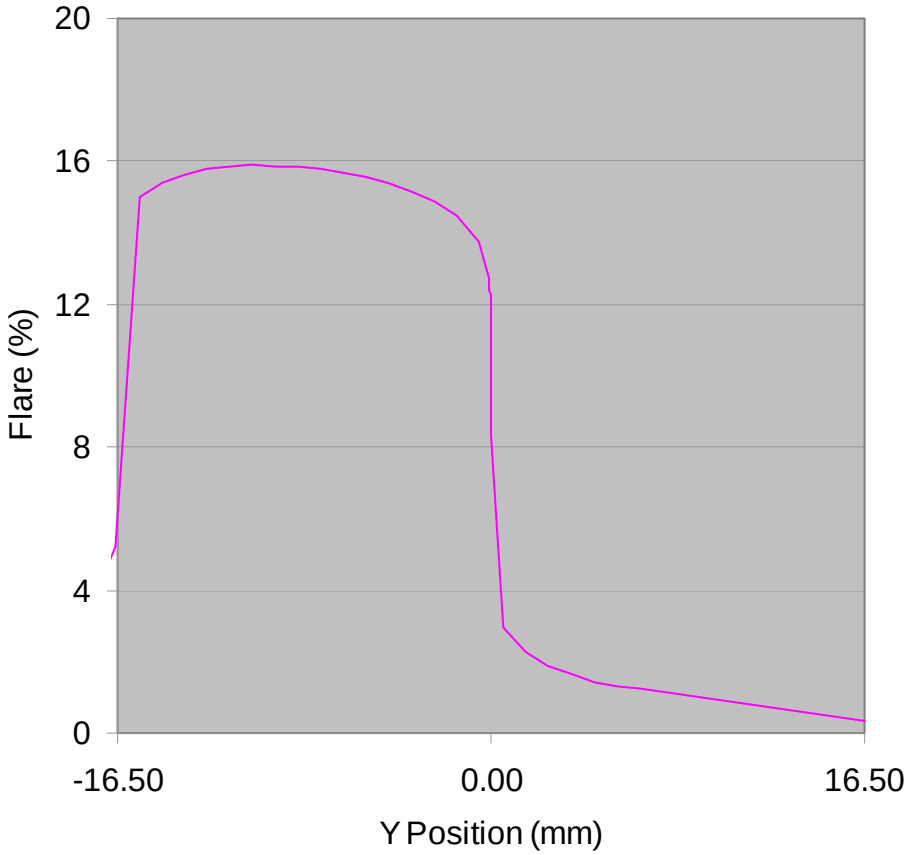
Long Range Flare





- Flare Map (50 micron sampling)
- Flare Profile

Large variation in Flare through the mask

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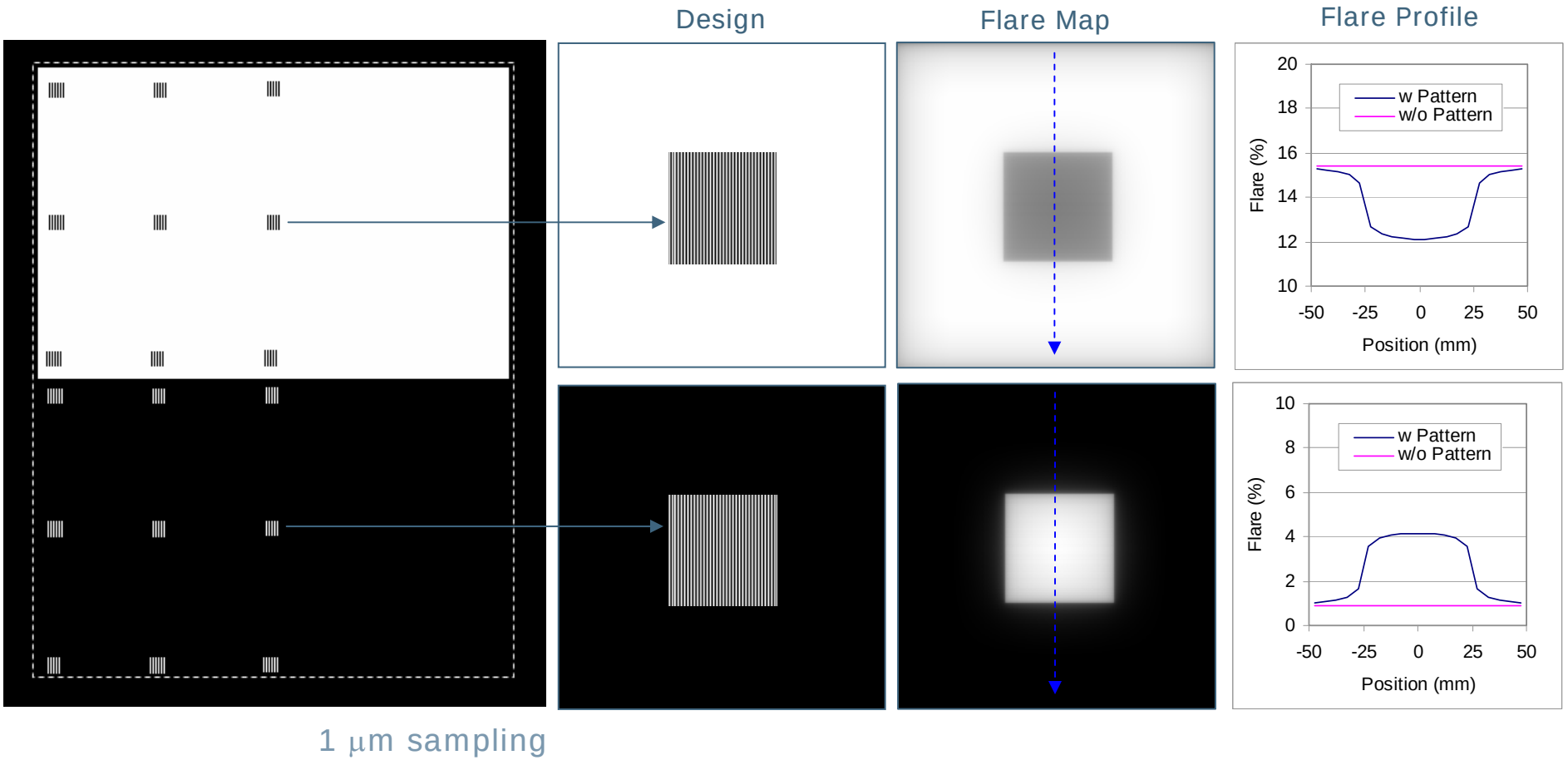
Short Range Flare



1 μm sampling

- **Local contribution is only a few percent %**
- **Flare "reversal" depending on the surrounding**

Singh et al.
Intel Corp
US Patent No. 6,625,802 B2

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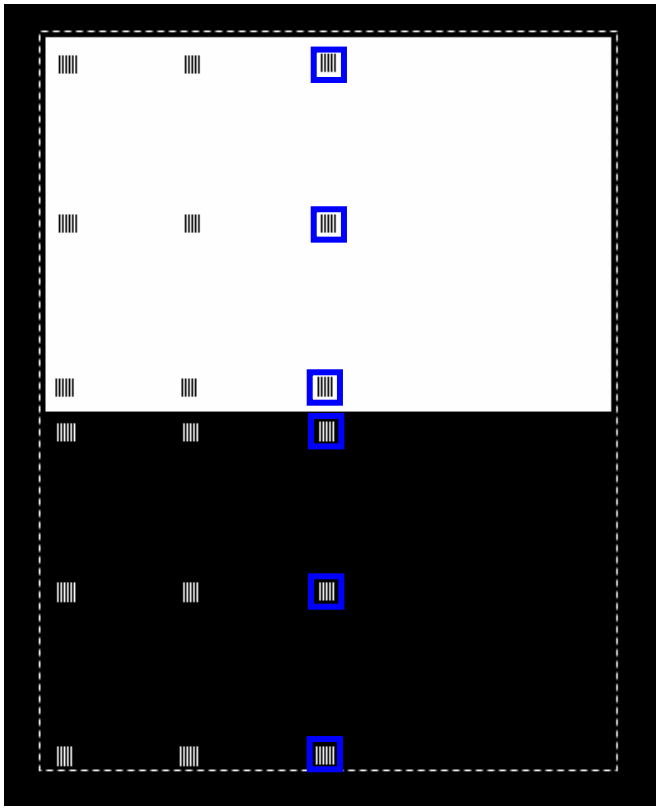
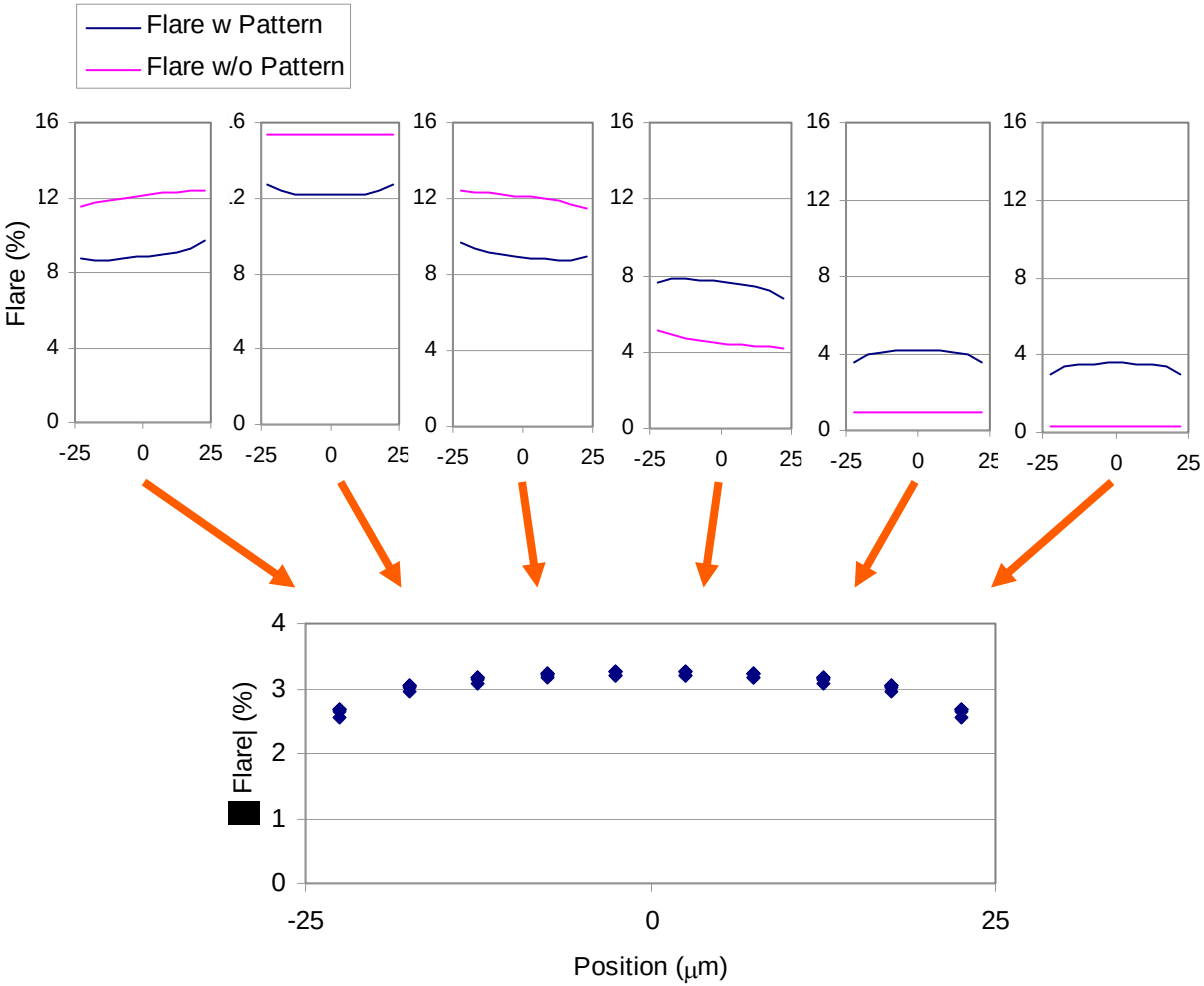
Modulation of Short Range Flare – 1D





- **Short range flare is modulated by long range flare**
- **The individual contribution of each short range pattern is identical**

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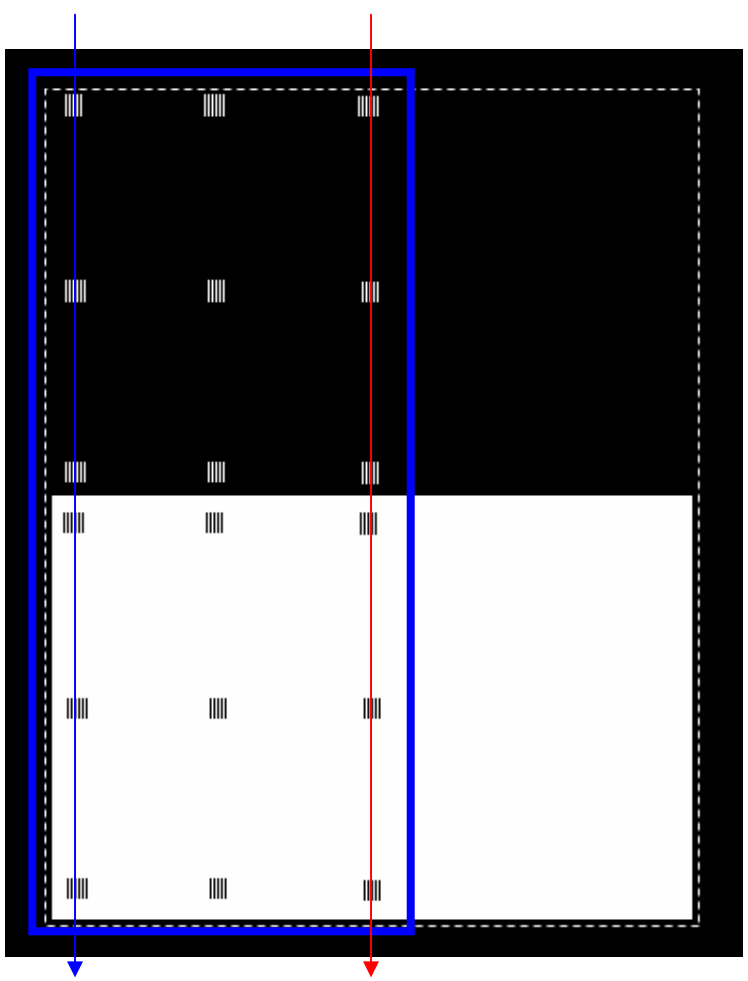
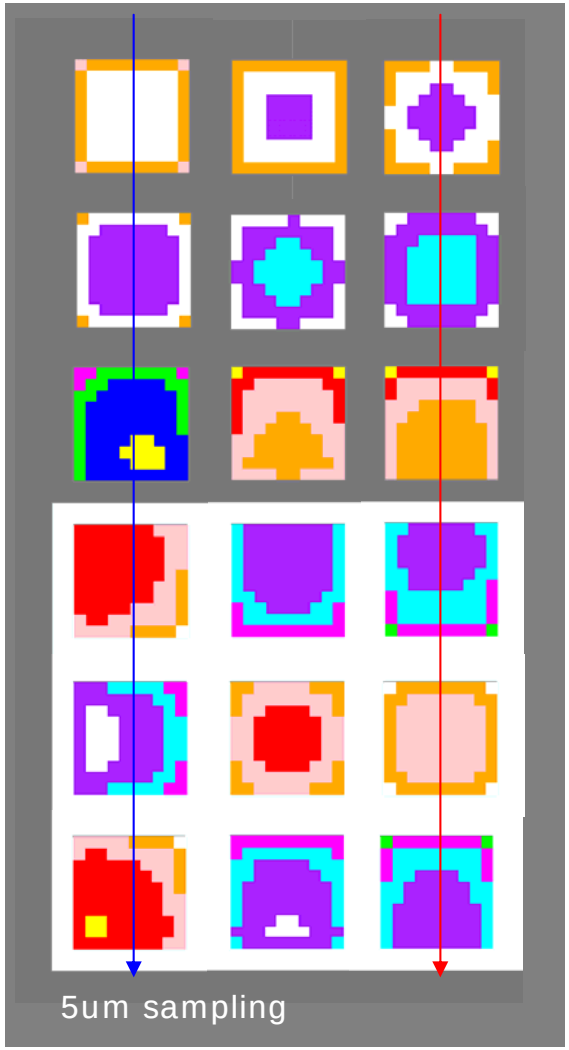
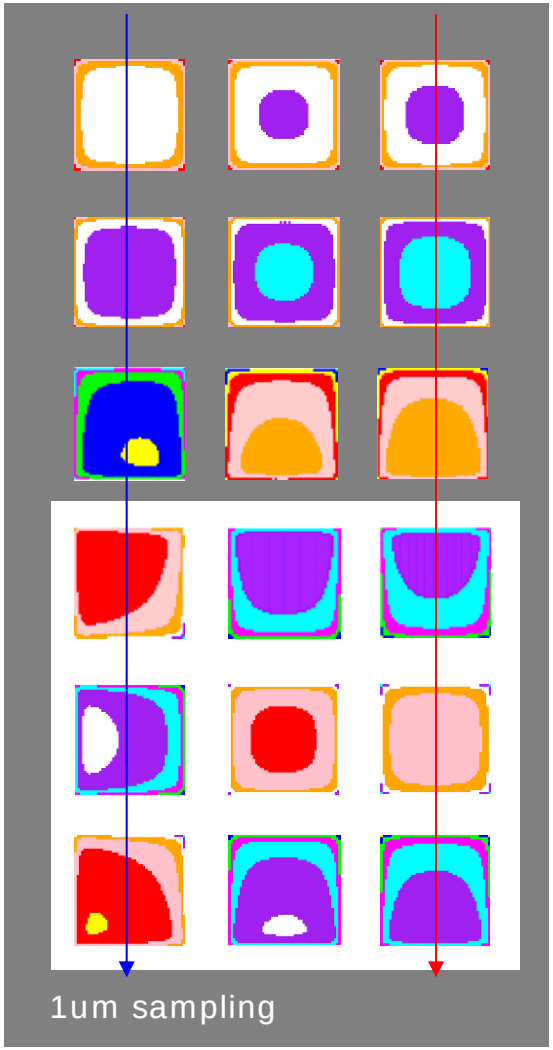
Modulation of Short Range Flare – 2D







- **Local flare maps skewed by long range flare**

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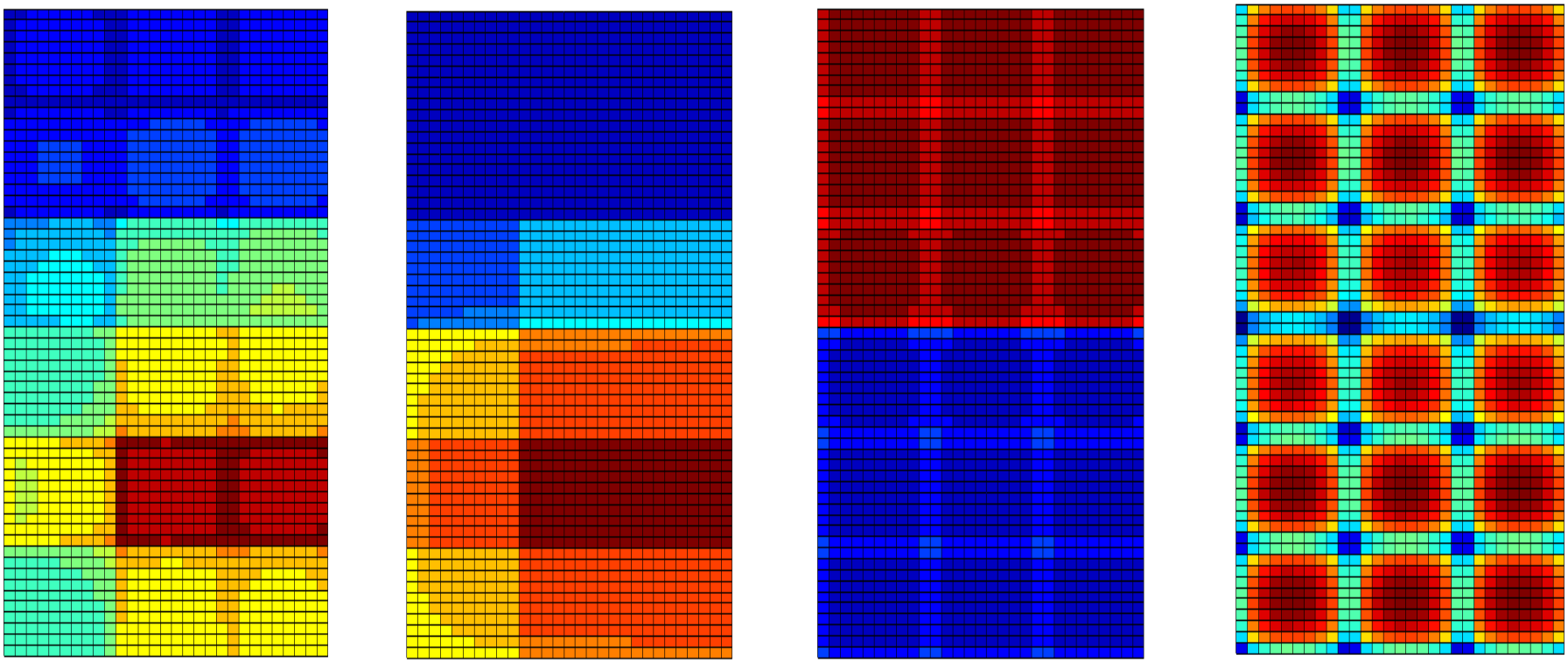
Modulation of Short Range Flare – 2D



- **The individual contribution of each short range pattern is identical in 2D**

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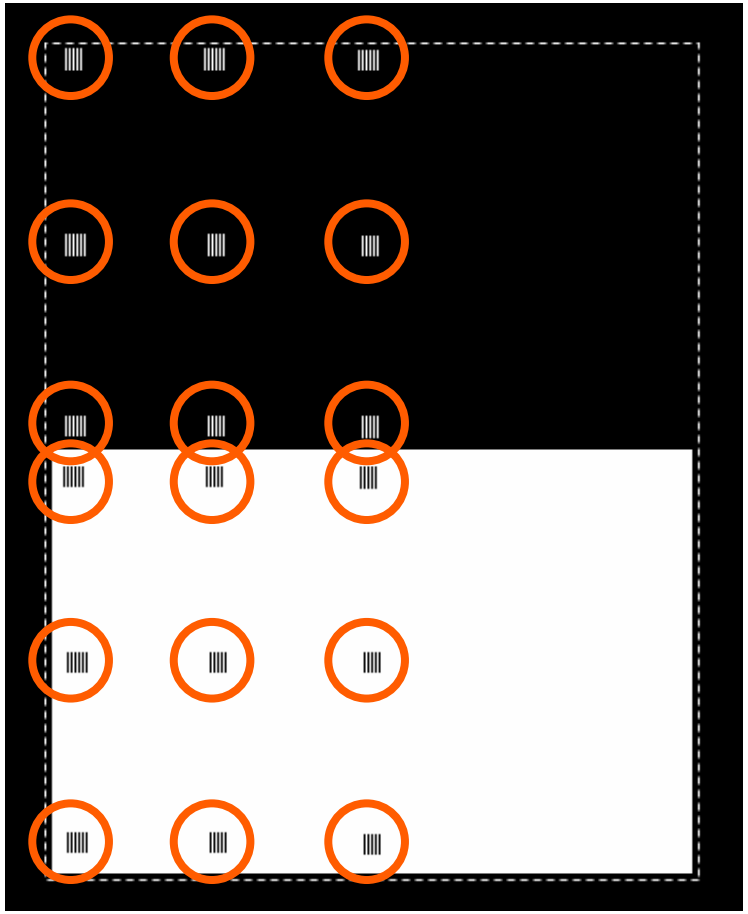
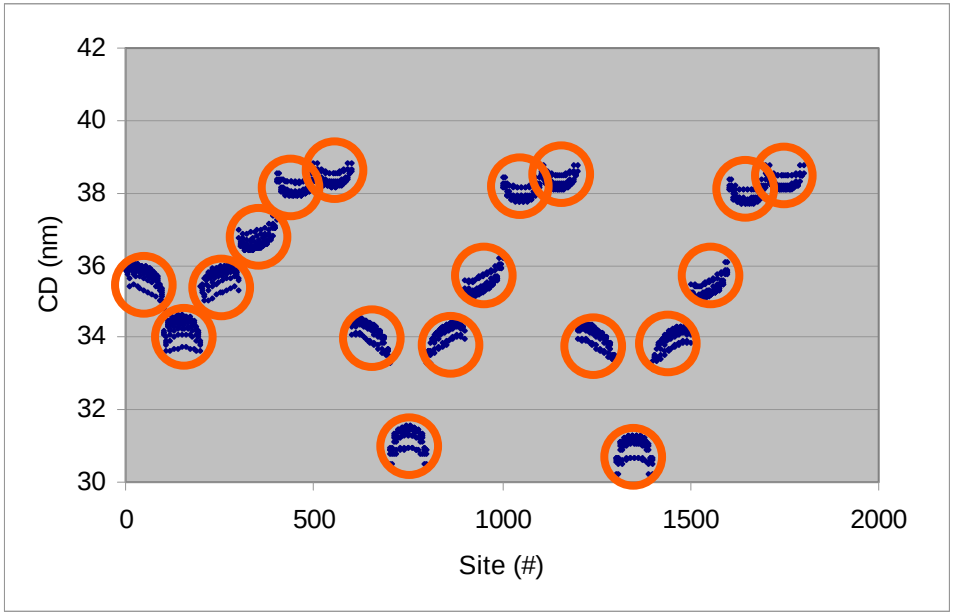
CD Variation with Flare





CD Uncorrected (5μ m resolution)

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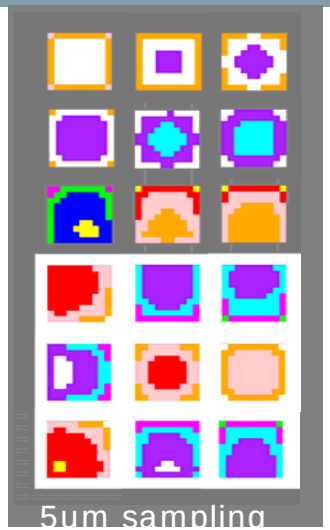
Rule-based Flare Correction

Flare Map



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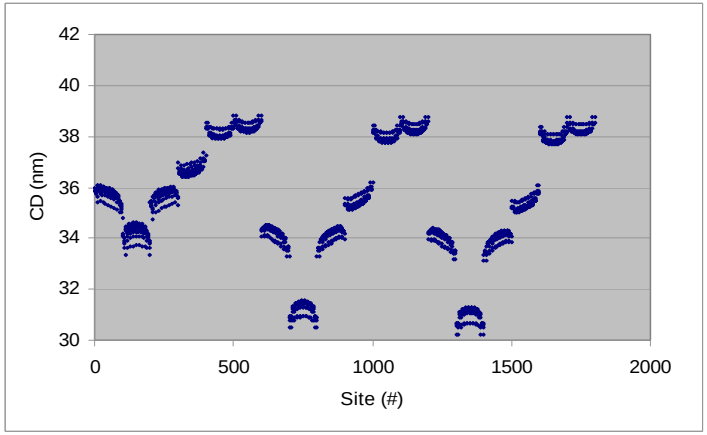

CD Uncorrected (5μ m resolution)

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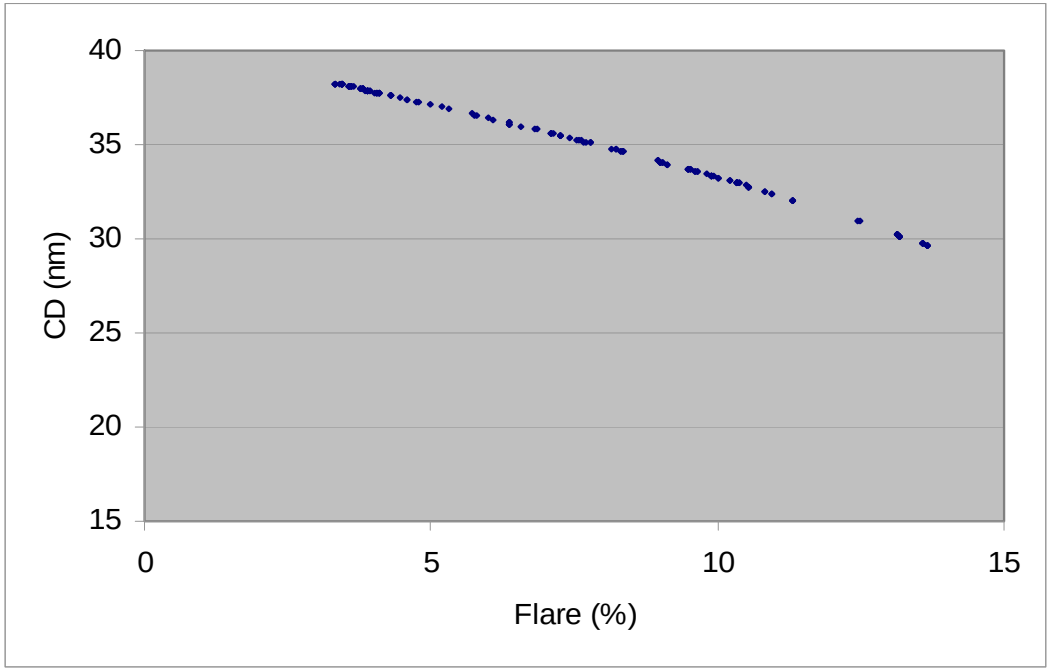

Rule

- **Rule-base correction re-sizes CD at mask level to remove flare artifacts**

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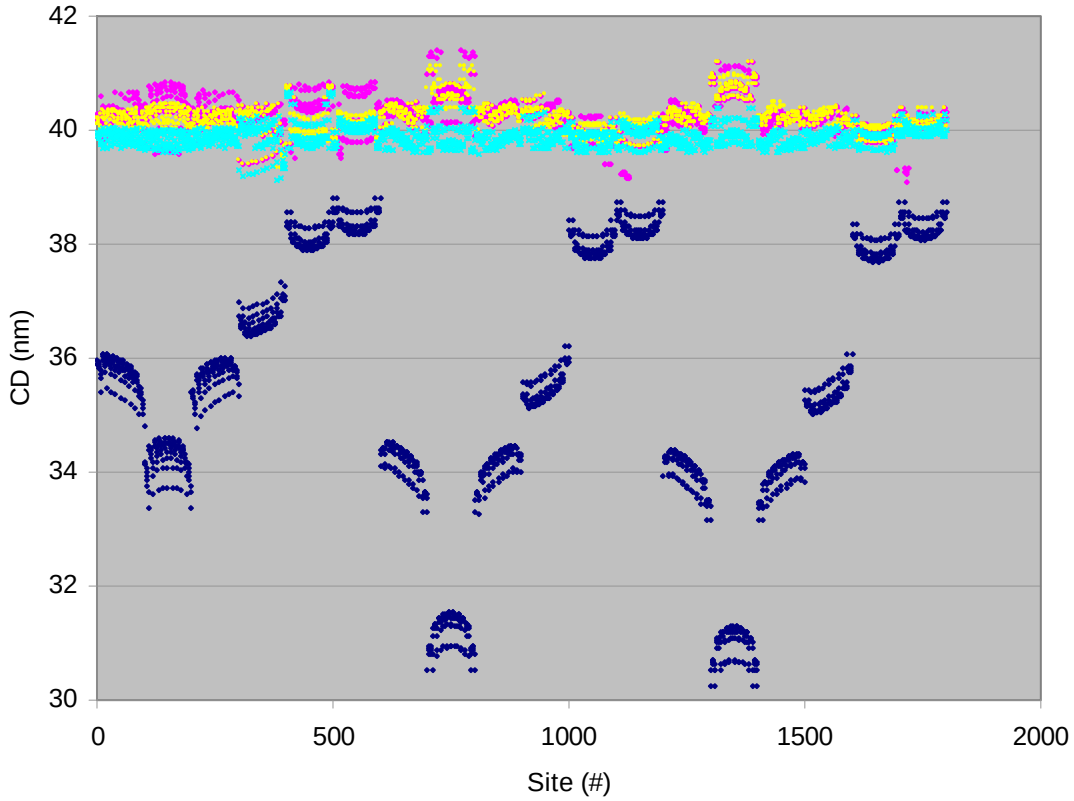
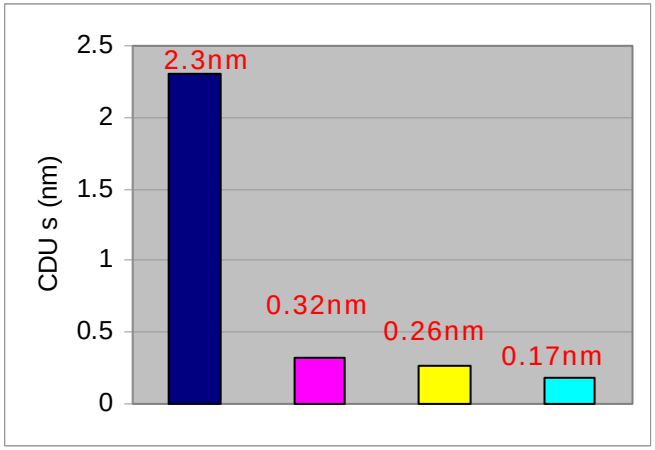
Quantifying the Quality of Rule-based Flare Correction (accounting for MEEF)



- CD Uncorrected
- CD Flare-corrected - not fractured
- CD Flare-corrected – Fractured
- CD Flare-corrected – Fractured – Iterated on Flare



- **Rule-base correction is very effective**
- **Small residual caused by MEEF and binning (estimated σ = 0.18nm)**
- **High-quality Full-Chip Flare map critical to implement rule-based**

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Simplification of Flare Map Calculation

- Why we need to simplify
  - Rigorous full chip calculations with 1μm resolution would take **261 yrs**

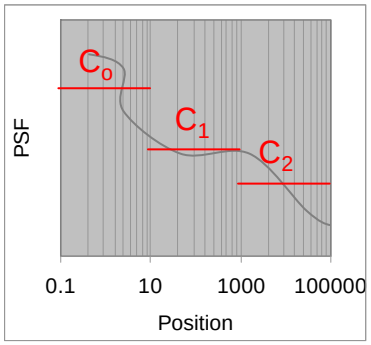
- Factorization of the convolution integral

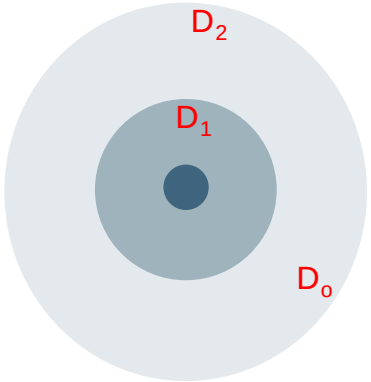
$$\int_0^{\infty} PSF \otimes D = \int_0^{R_0} PSF \otimes D + \int_{R_0}^{R_1} PSF \otimes D + \int_{R_1}^{R_2} PSF \otimes D + \ldots + \int_{Rn}^{\infty} PSF \otimes D$$

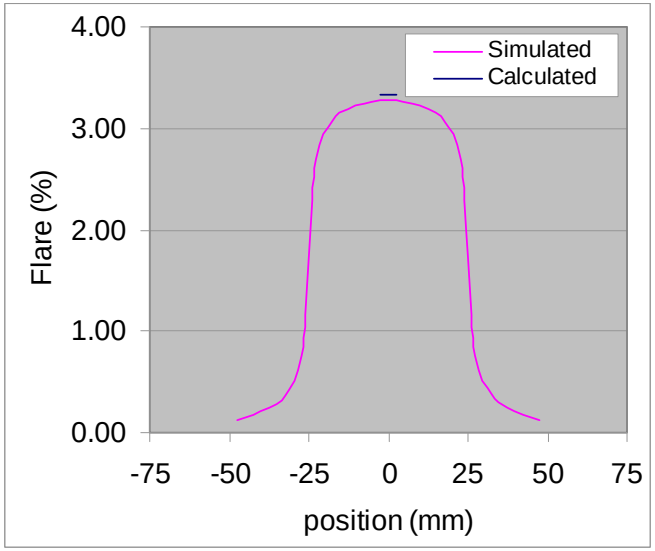
$$= C_0 \int_0^{R_0} D + C_1 \int_{R_0}^{R_1} D + C_2 \int_{R_1}^{R_2} D + \ldots + C_n \int_{Rn}^{\infty} D$$

$$= C_0 D_0 + C_1 D_1 + C_2 D_2 \ldots + C_n D_n$$

- Logarithmic sampling in space







- **Simplified model is accurate**

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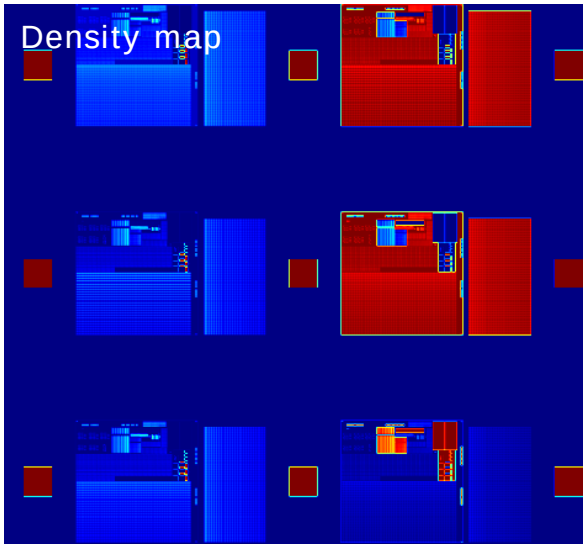
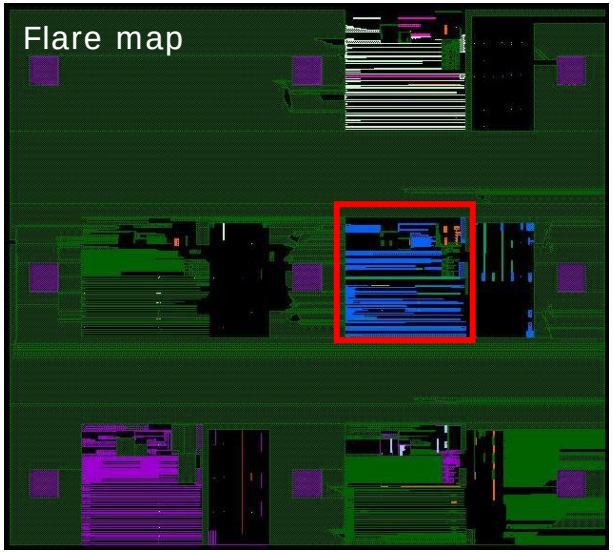
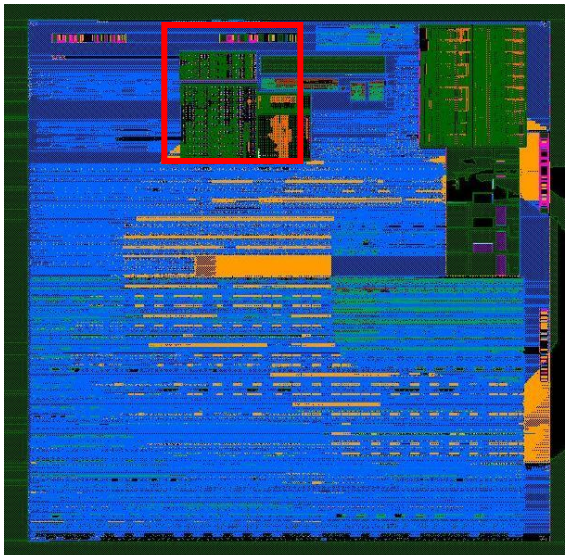
Full Chip Flare Map of TM07



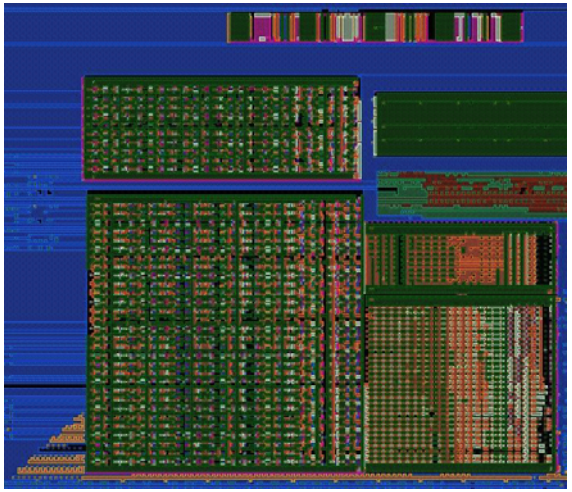
68 hrs





10.4mm x 9.34 mm
14 GB
10 μm resolution

10.4mm x 9.34 mm
4 GB
30 μm resolution



- **High resolution full chip flare map can be calculated in reasonable time with standard SW**

Courtesy Brian Ward from Synopsys

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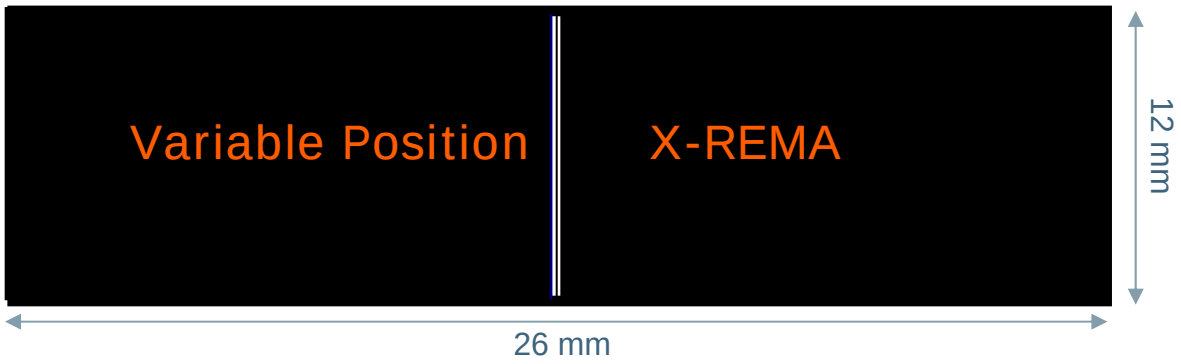
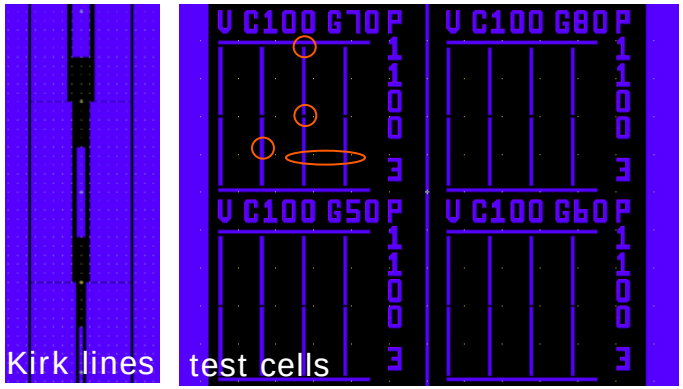
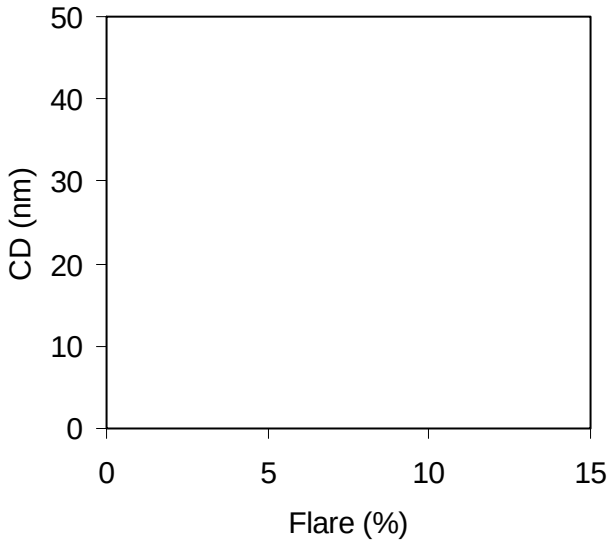
Experimental Determination of the Flare Design Rules







CD 20 – 100 nm
Gaps/Line Ends 30 – 100 nm
Pitch 1:1 – 1:10

C. Mack, Proceedings of SPIE, Vol. 5040, 2003, p 151-161.

Mask co-designed and built at Intel's mask shop, ready to use

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Conclusions

- Short and long-range flare are separable with no loss in accuracy
- Rule-based flare mitigation strategy is effective
- A full-chip high-resolution flare map is feasible
- Experimental determination of rules can be determined on the ADT with a dedicated mask

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Acknowledgments

- Brian Ward (Synopsys)
- Mieke Goethals, Rik Jonckheere (IMEC)
- Noreen Harned, John Zimmerman, Hans Meiling (ASML)

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