Development of EUV mask substrates with low thermal expansion

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Critical issues of EUV mask substrates

CTE

Requirement :＜±5ppb/K in production

⇒Low Thermal Expansion Material (LTEM) will be needed

In HOYA, Corning ULE (SiO_2-TiO_2 glass) is mainly used as EUV mask substrate

Flatness

Requirement : ＜50 nm P-V on both sides (142mm sq.)

Flatness;d

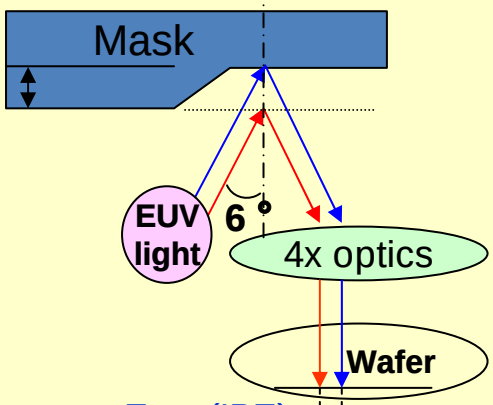


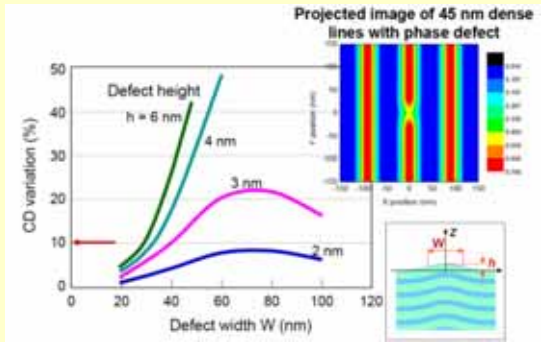
Image Placement Error(IPE)

=(d ＊tan6 °)/4 ＜4.8nm (ITRS spec. @2010)

Defects

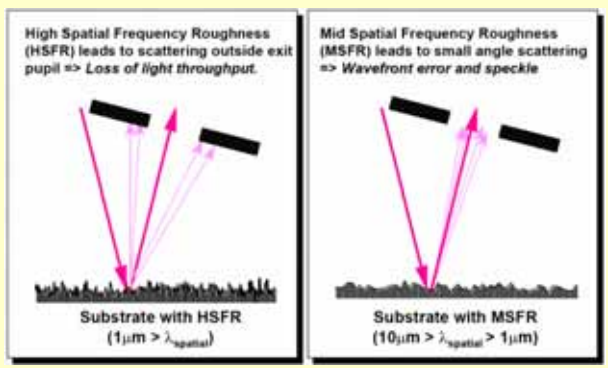
Killer defects : 70nmW x 2nmH on ML

Simulation results T. Terasawa et al. PMJ2004



Roughness(HSFR, MSFR, Local slope, etc.)

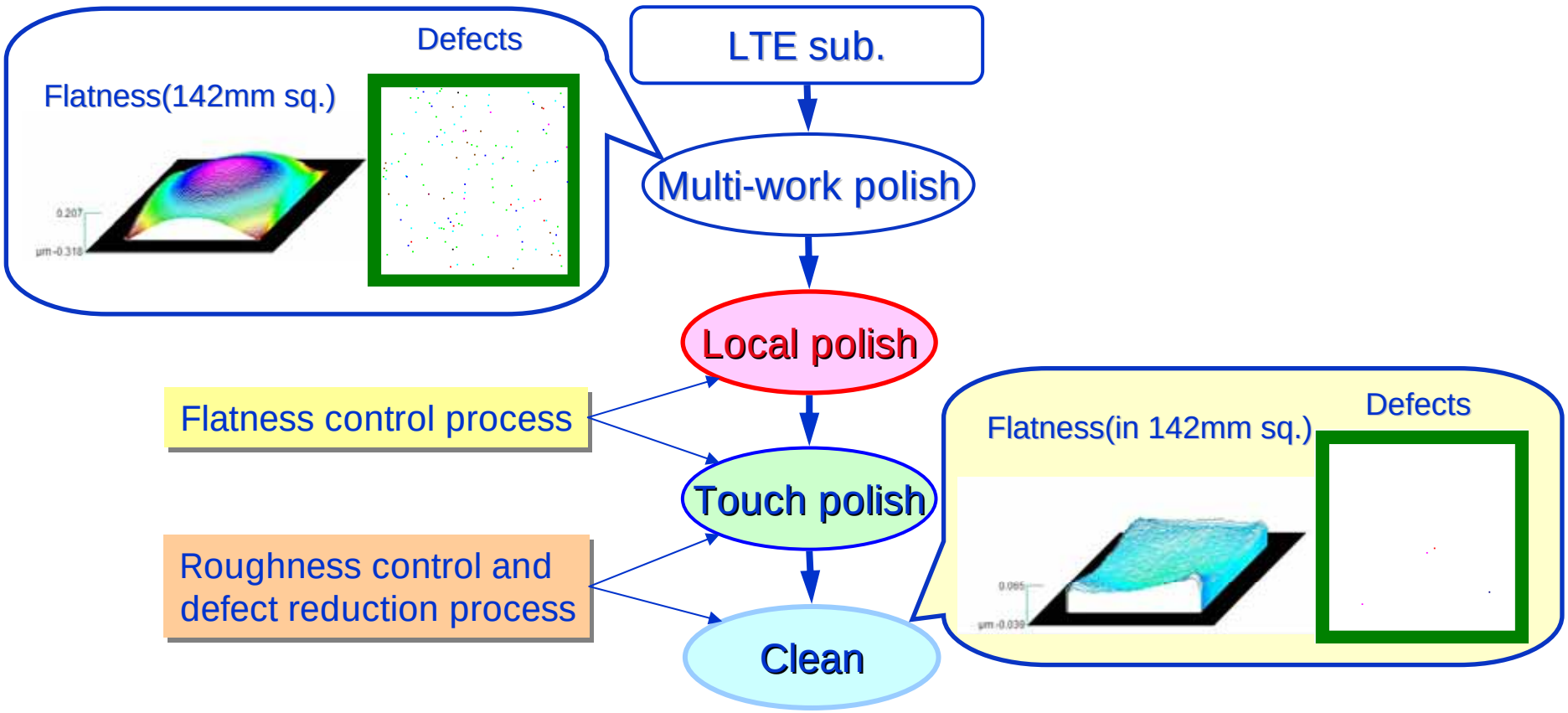
⇒Affect on EUV light reflectivity and LER



EUV mask substrates specification (SEMI P37)

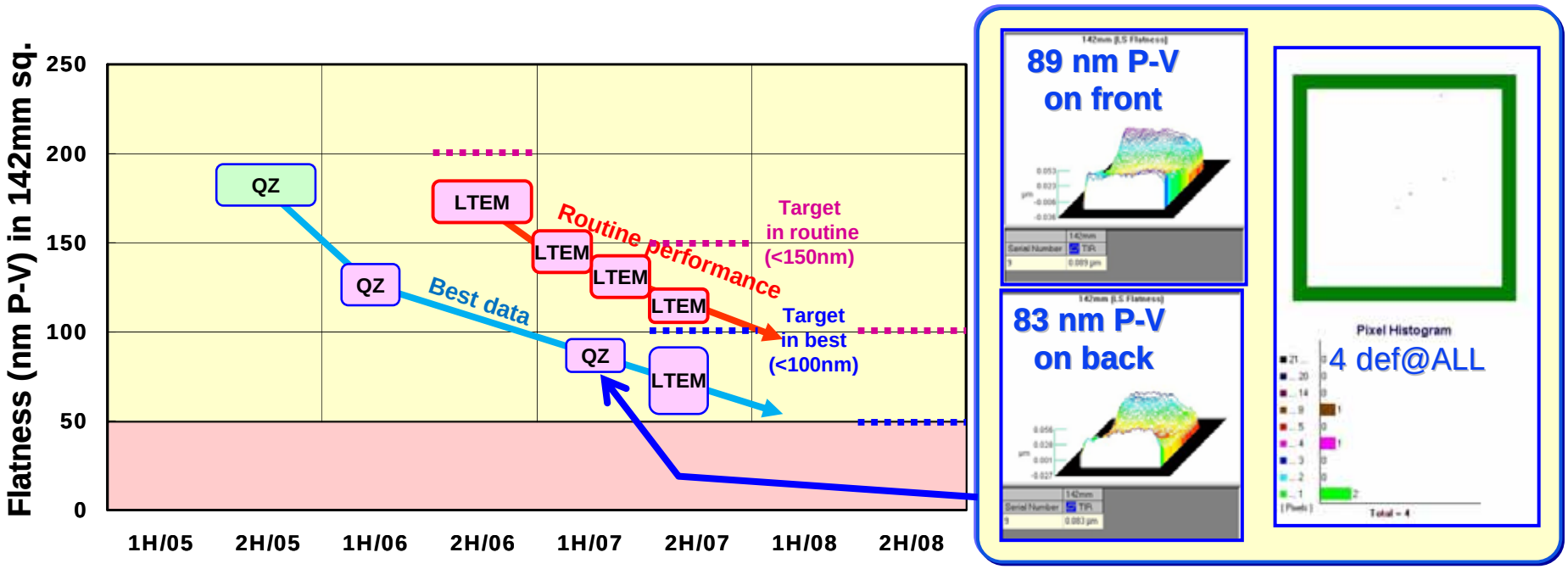
	Size or area definition	Spec.	units	Current metrology in HOYA
Coefficient of thermal expansion (CTE)		Class A:±5 Class B:±10	ppb/K	
Flatness (Both sides)	142mm sq.	Class A:<30 Class B:<50	nm P-V	Corning-Tropel Ultra Flat
Roughness① Local slope(low)	$5\mu m < \lambda_{spatial} < 1mm$	<1.5	mrad (3σ)	Zygo NewView
Roughness② Local slope(high)	$250nm < \lambda_{spatial} < 5\mu m$	<1.8	mrad (3σ)	AFM
Roughness③ HSFR	$50nm < \lambda_{spatial} < 250nm$	<0.15	nm-rms (1σ)	
Defect (Particle, Pit)	> 50nm PSL equivalent size	0	counts /cm²	Lasertec M1350

Process flow of EUV mask substrates



- Advanced processes including local polish have been developing to attain substrates with higher flatness and lower defects

Flatness improvement

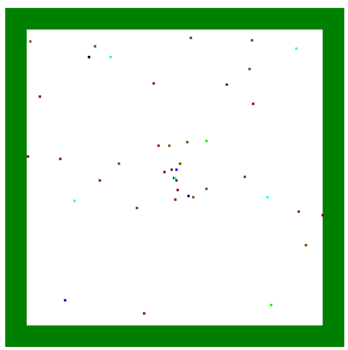


- Substrates with high flatness and low defects can be produced using local polish
- Best flatness of ~80nm and routine flatness of ~120nm were attained in 2007

Defect reduction of LTE substrates

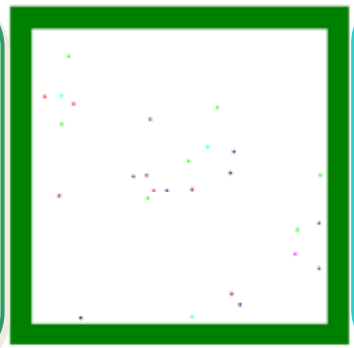
Inspection equipment: Lasertec M1350

1H/'06
0.23def/cm^2@all pixels



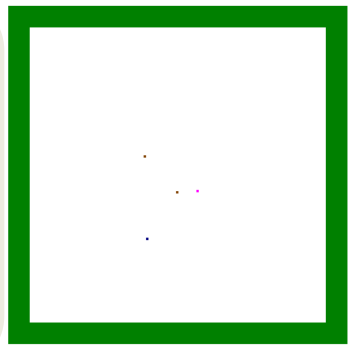
Polishing process development → to decrease pits

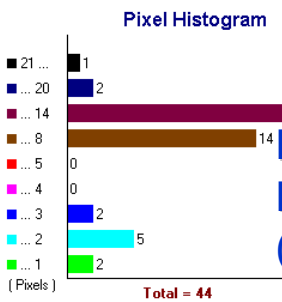
2H/'06
0.15def/cm^2



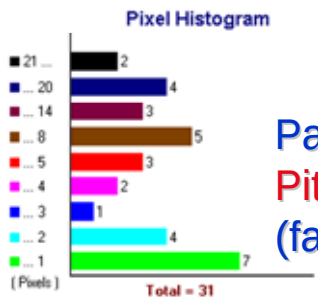
Cleaning process development → to decrease particles

1H/'07
0.02def/cm^2

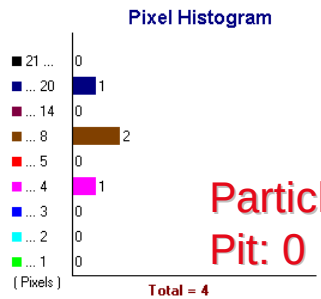




Particle: 32
Pit: 10
(false: 2)



Particle: 26
Pit: 1
(false: 4)



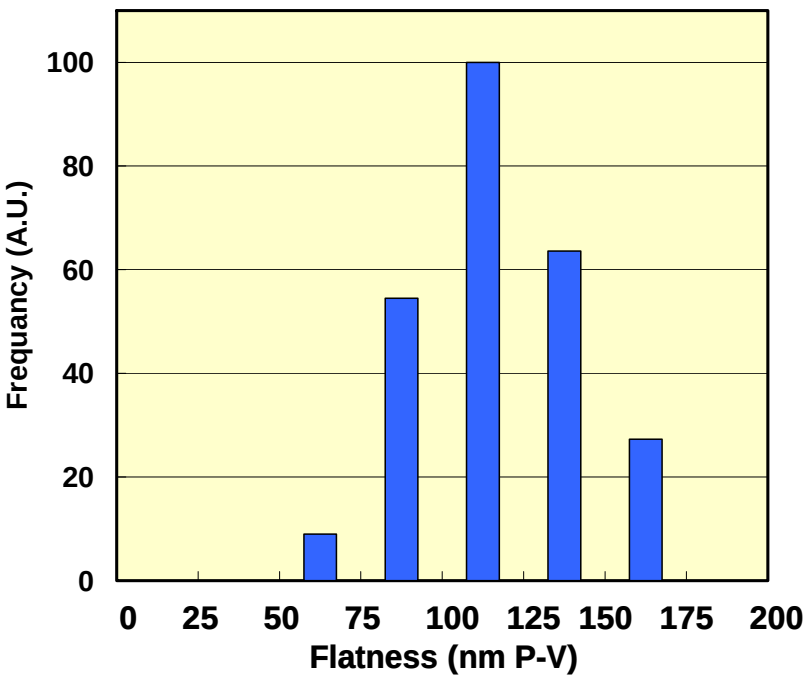
Particle: 4
Pit: 0

- Defects on LTE substrates have been decreased by improvements of polishing and cleaning processes

LTE substrates performance: Flatness and defects

Routine Target in 2007: <150 nm P-V in 142mm sq.

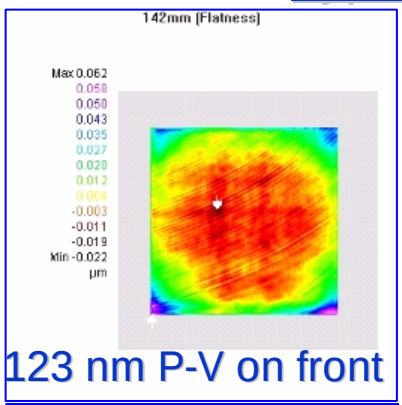
Reproducibility



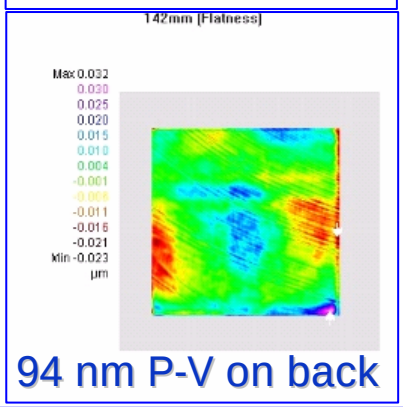
Average：117 nm P-V

23% was within 100 nm P-V

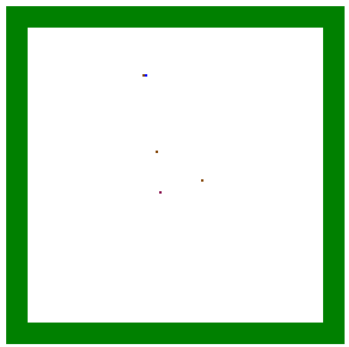
Typical ULE substrate

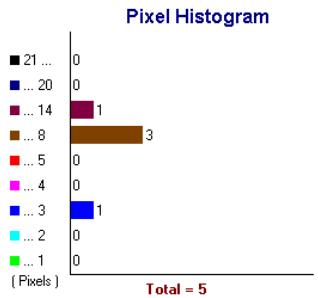


123 nm P-V on front



94 nm P-V on back



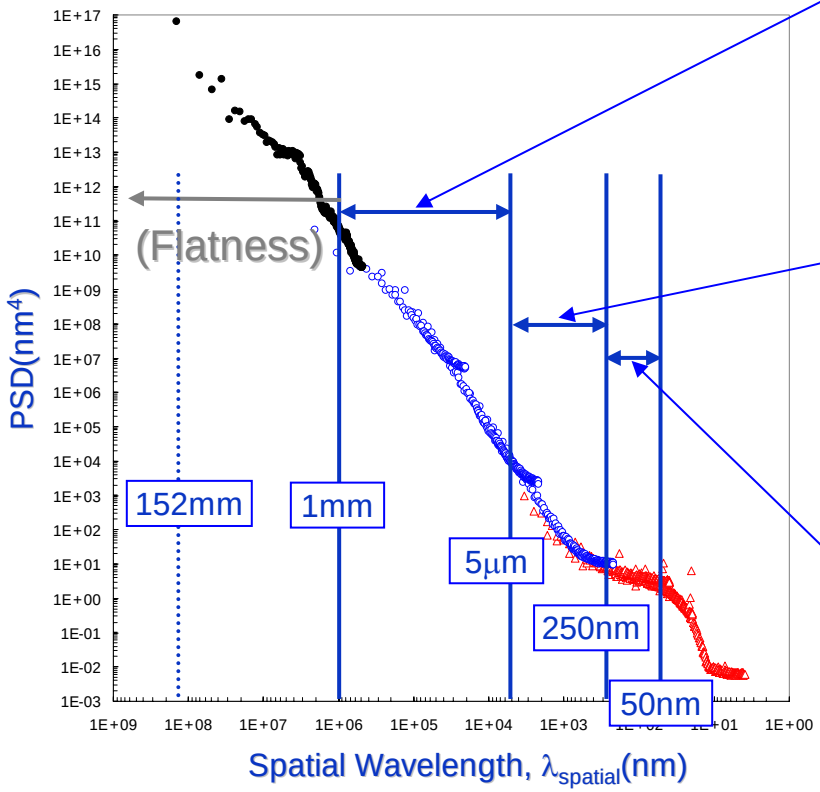


5 defects@all

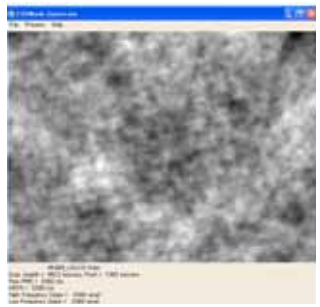
- LTE substrates with high flatness of 100 nm and low defects were achieved

LTE substrates performance: Roughness

Power spectle density curve of LTE sub.

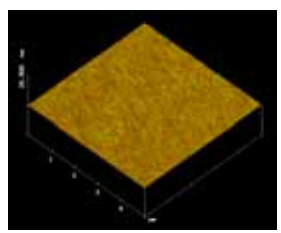


・Local Slope(low):
0.29mrad(3σ)
⇒◎



・Local Slope(high):
1.99mrad(3σ)
⇒△

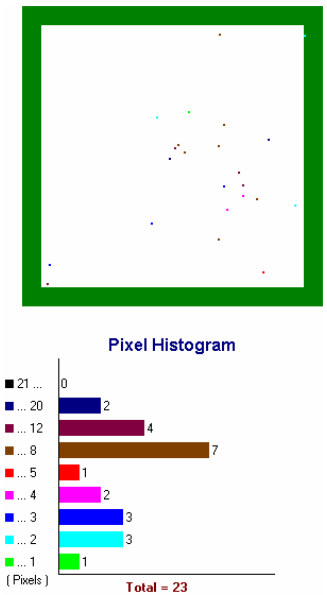
・HSFR:
0.08nm
⇒◎



- Local slope(high) should be improved

Performance of ML blanks with LTE sub.

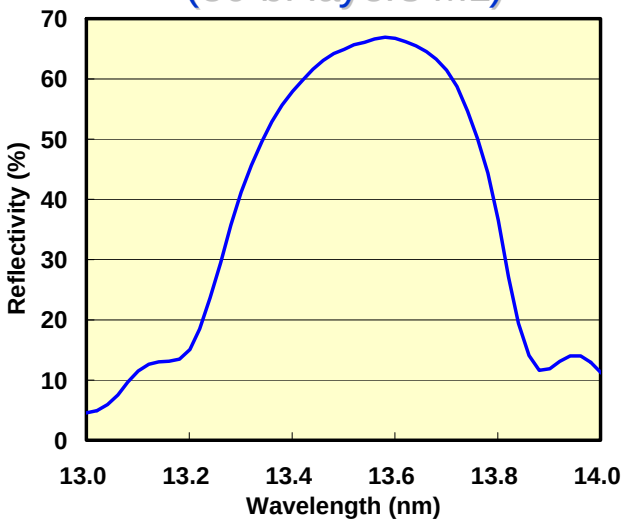
ML blank defects



23 defects

EUV reflectivity spectra

(50 bi-layers ML)



EUV reflectivity was measured by reflectometer located at Selete

	Blanks on LTEM	Target in 2007	Target in 2010
Reflectivity (Peak, %)	66.4	>64	>66
Defects on ML (counts/cm^2)	0.13 @70nm	0.40 @70nm	0.20 @40nm

- ML blanks meeting the target spec. in 2007 can be produced by using improved ULE substrates

Summary

- HOYA has been focusing on development of fabrication process for LTE substrates to attain high flatness, smooth surface and low defects, since 2006
- LTE substrates with high flatness of less than120 nm and low defects of less than 0.05 def/cm^2@60 nm can be produced by improvement of fabrication process
- We are supplying EUV blanks with LTE substrates meeting target specifications for alpha EUV exposure test

- We are now challenging further defect reduction and further flatness improvement of LTE substrates toward production target