ASML

The only cost effective extendable lithography option: EUV

Martin van den Brink
Executive Vice President Marketing and Technology

Barcelona, October 17, 2006

Content

- Lithography will remain key driver for shrink
- Need for shrink continues
- The only cost effective extendable lithography option: EUV
- EUV partnering and infrastructure
- Conclusion

The impact of lithography in 2006

Semiconductor Market
>$250B

Litho Tools, Masks, Mask Equipment, Resist Materials and RET SW
$13B

Litho Exposure Tools
$6.5B

Source: VLSI Research,

The impact of lithography in 2011

Semiconductor Market
>$350B

Litho Tools, Masks, Mask Equipment, Resist Materials and RET SW
$19B

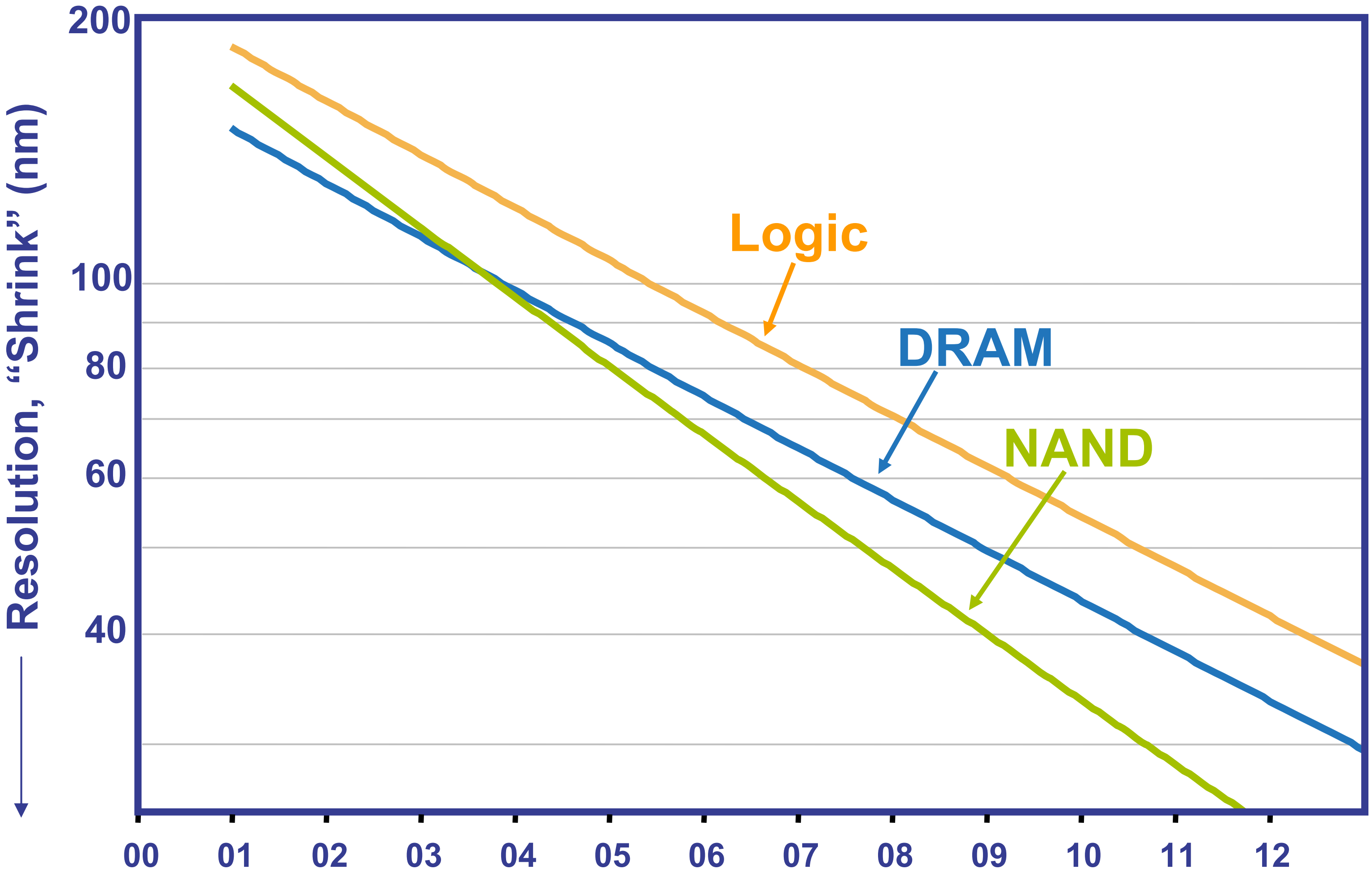
Litho Exposure Tools
$11B

Source: VLSI Research,

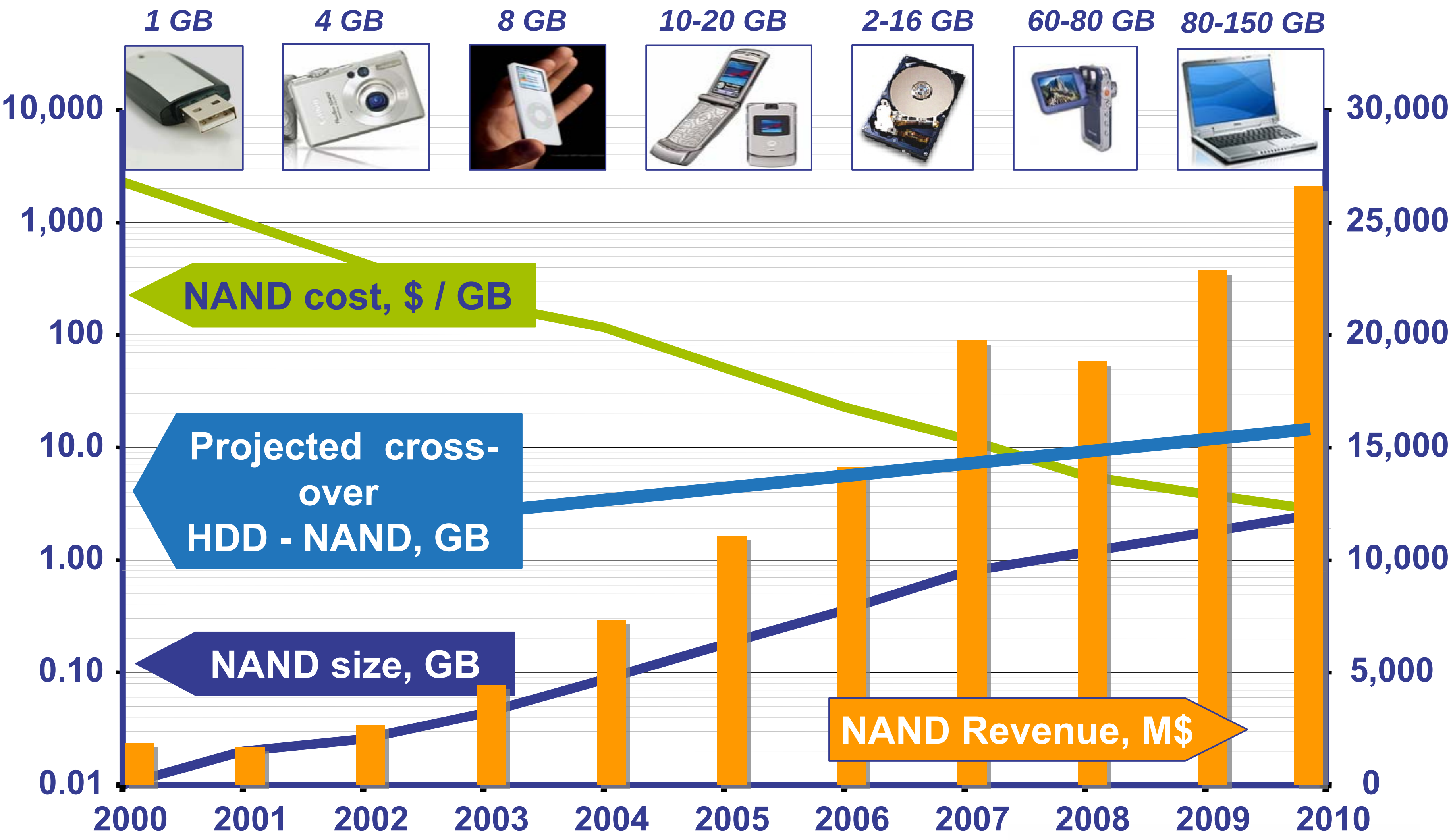
Content

- Lithography will remain key driver for shrink
- **Need for shrink continues**
- The only cost effective extendable lithography option: EUV
- EUV infrastructure
- Conclusion

Customers' appetite for shrink continues unabated



Shrink drives cost per function and market growth

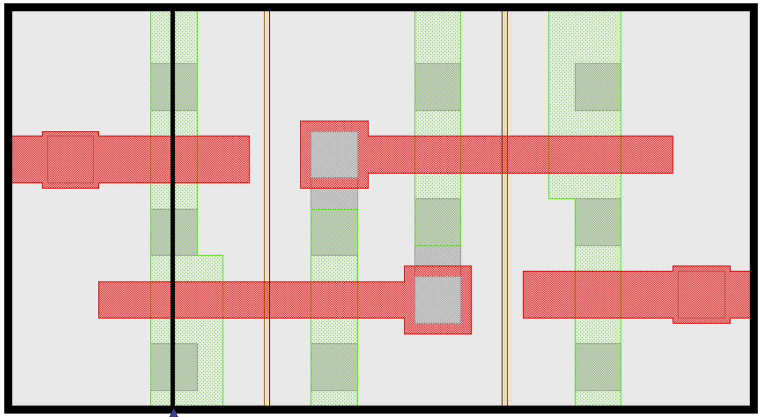


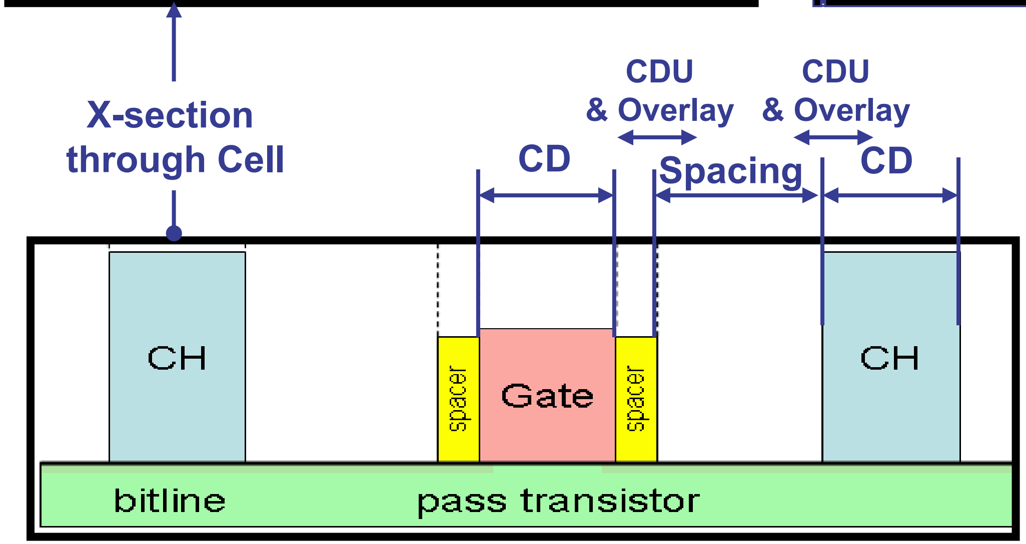
Source: Gartner Dataquest, iSuppli, ASML

Barcelona, October 2006/ Slide 7

Resolution, CD uniformity & overlay drive shrink

Layout 6 transistor SRAM Cell



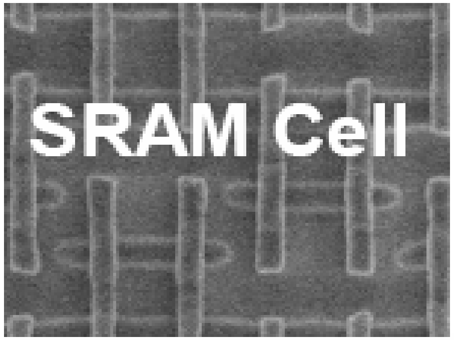


Source: IMEC, TI

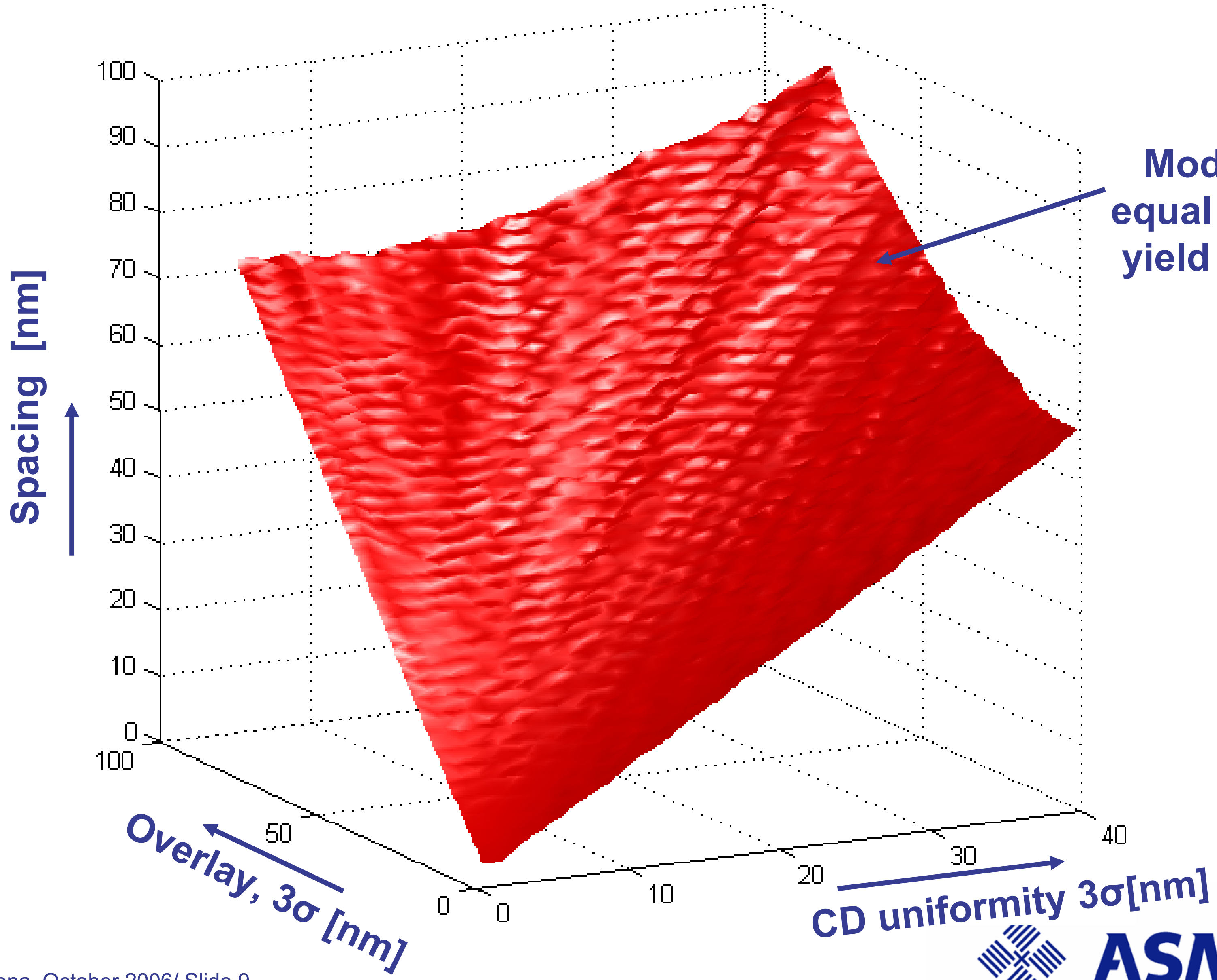
Design Rule & Cell Area [µm²]

Node	Aggressive	Typical	Relaxed
130 nm	2.00	2.50	3.00
90 nm	1.00	1.25	1.50
65 nm	0.45	0.55	0.80
45 nm	0.20	0.27	0.34
32 nm	0.10	0.13	0.19

cell area 0.24 μm^2
metal pitch 130nm
ArF immersion



Overlay and resolution (-control) key for device scaling



Modeled equal 99.9% yield plane

Roadmap scenarios

Resulting k_1 as function of resolution, wavelength and NA

	half pitch	100	65	45	32	22	16	11
	year		2005	2007	2009	2011	2013	2015
λ [nm]	NA							
248	0.80	0.32						
193	0.93		0.31					
	1.20		0.40	0.28				
	1.35			0.31	0.22	0.15		
	1.55				0.26	0.18		
13.5	0.25				0.59	0.41		
	0.35					0.57	0.41	
	0.45						0.53	0.37

k_1 = (half pitch) * NA / wavelength

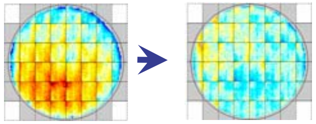
Most aggressive k_1 in production today = 0.3,
physical limit single exposure = 0.25
Practical limit double patterning = 0.2

Highest air-based NA system will support 60-65 nm

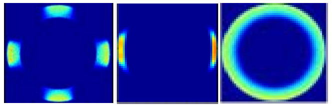
	half pitch	80	65	45	32	22	16	11
	year		2005	2007	2009	2011	2013	2015
λ [nm]	NA							
248	0.80	0.30						
193	0.93		0.31					
	1.20		0.40	0.28				
	1.35			0.31	0.22	0.15		
	1.55				0.26	0.18		
13.5	0.25				0.59	0.41		
	0.35					0.57	0.41	
	0.45						0.53	0.37

Highest air based NA supports 60-65 nm

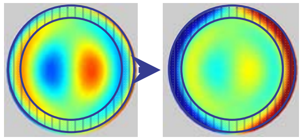
ASML mask and system enhancements extend lithography to the limit of k_1



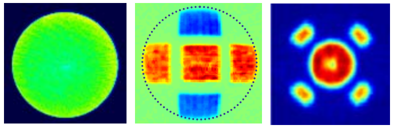
DoseMapper for optimum CD Uniformity



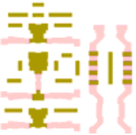
Flexible off-axis & polarized illumination



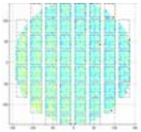
Application specific lens setup



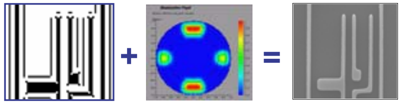
In-built wave-front, polarization and pupil metrology



Mask enhancement techniques & optimization software



Offline Dual stage wafer height mapping
Focus Dry, Expose Wet



Illumination source optimization & software

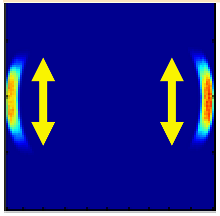
First super high NA immersion system enables 45 nm

	half pitch	100	65	45	32	22	16	11
	year		2005	2007	2009	2011	2013	2015
λ [nm]	NA							
248	0.80	0.32						
193	0.93		0.31					
	1.20		0.40	0.28				
	1.35			0.31	0.22	0.15		
	1.55				0.26	0.18		
13.5	0.25				0.59	0.41		
	0.35					0.57	0.41	
	0.45						0.53	0.37

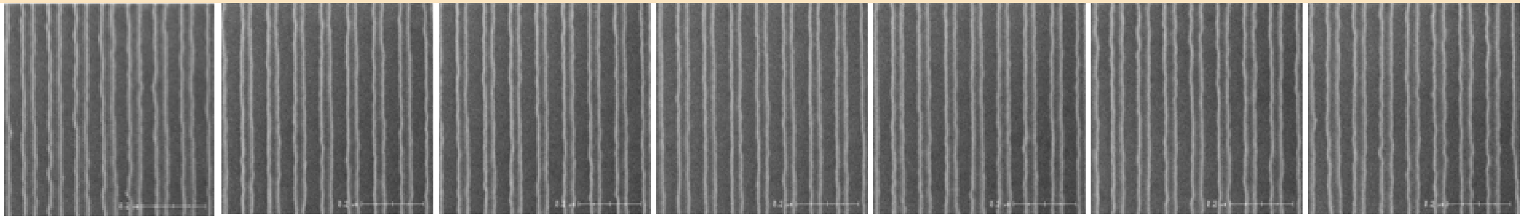
First super high NA immersion system enables 45 nm

Overview dense line XT:1700i imaging results

42nm 1.2NA, σ=0.89/0.98, Dipole X-35, Y polarization, k1 =0.261

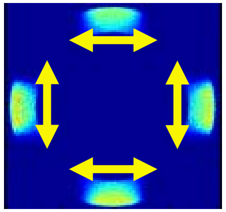


950nm DoF

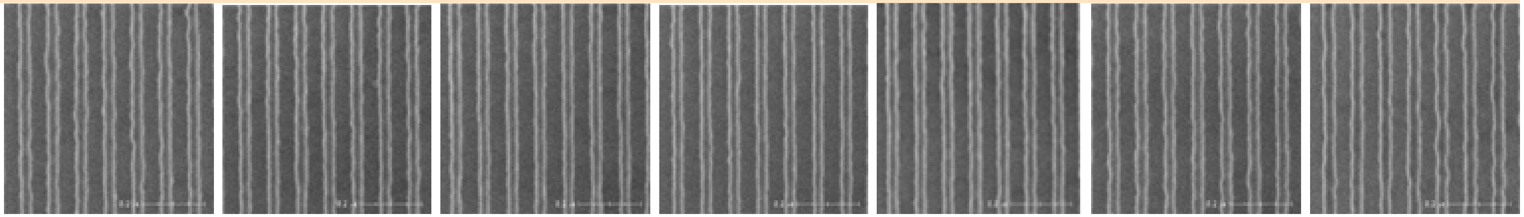


-500nm -300nm -180nm NF +180nm +300nm +450nm

45nm 1.2NA, σ=0.82/0.97, C-Quad-30, XY polarization, k1 = 0.28

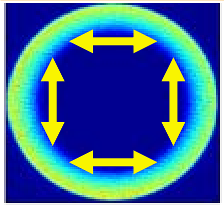


500nm DoF

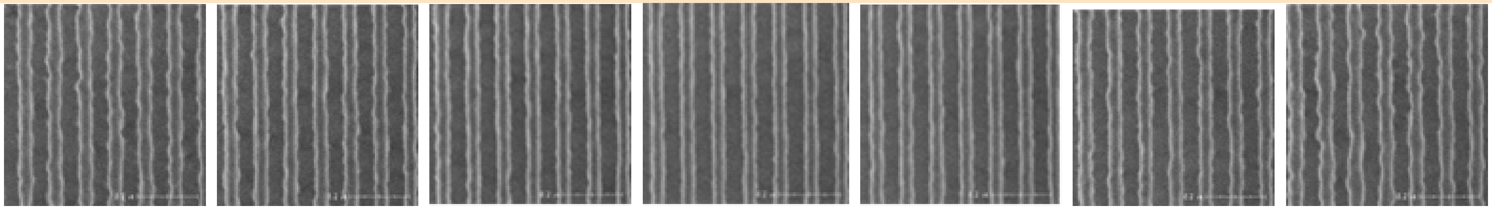


-300nm -240nm -120nm NF +60nm +120nm +210nm

50nm 1.2NA, σ=0.74/0.94, annular, XY polarization, k1 = 0.31



400nm DoF



-210nm -150nm -90nm NF +90nm +150nm +210nm

@ 550mm/s Scan speed

ASML

Roadmap scenarios, the impact of immersion

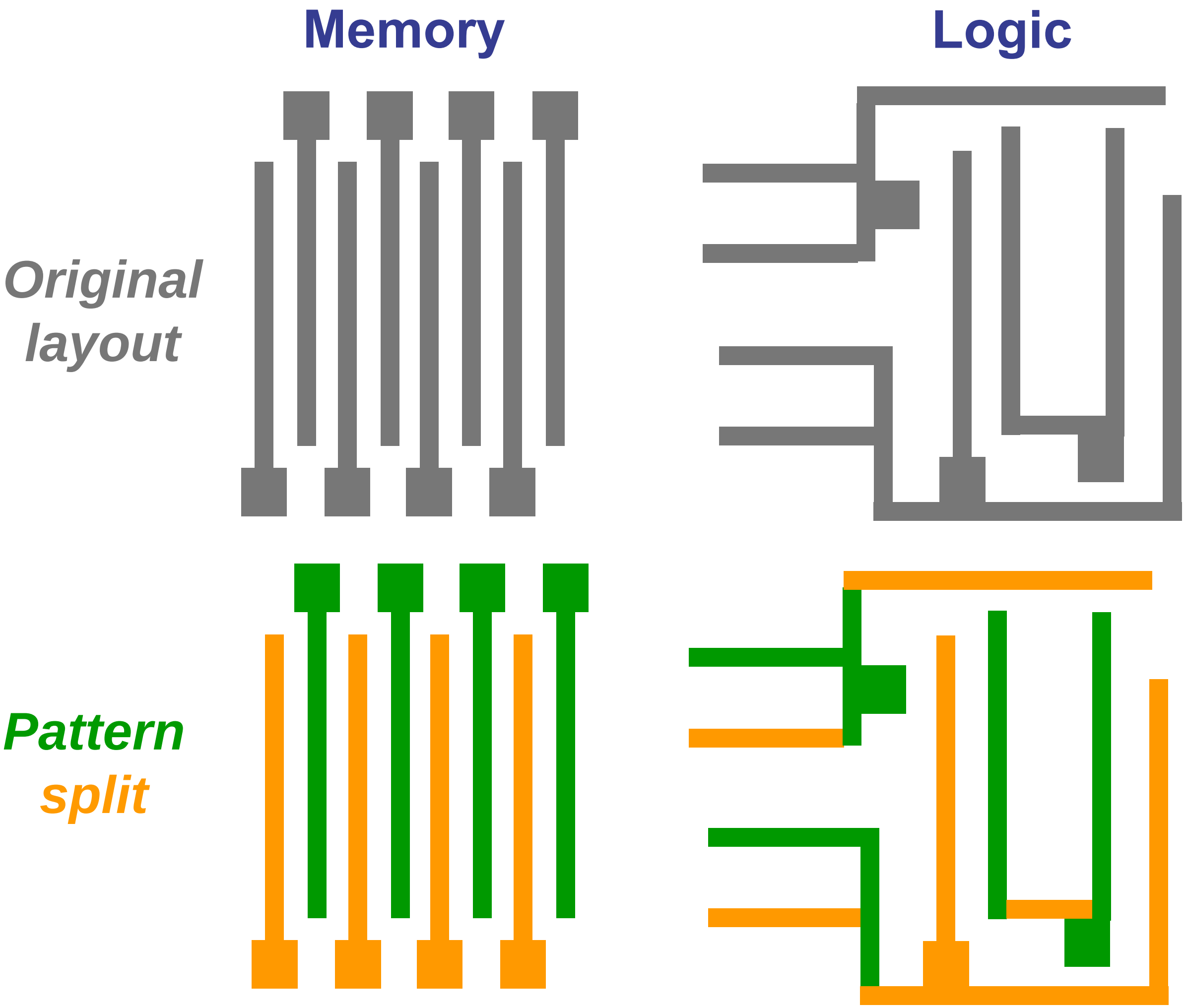
Water-based 193 not sufficient for 32-nm half pitch

DPT real option, but costly

	half pitch	100	65	45	32	22	16	11
	year		2005	2007	2009	2011	2013	2015
λ [nm]	NA							
248	0.80	0.32						
193	0.93		0.31					
	1.20		0.40	0.28				
	1.35			0.31	0.22	0.15		
	1.55				0.26	0.18		
13.5	0.25				0.59	0.41		
	0.35					0.57	0.41	
	0.45						0.53	0.37

Max NA water-based 193 nm immersion requires double patterning to get to 32 nm

New software & algorithms required to split & optimize OPC and stitching for Double Patterning



Challenges

- Correct decomposition
- OPC for decomposition
- Model-based stitching error compensation

Increasing Difficulty

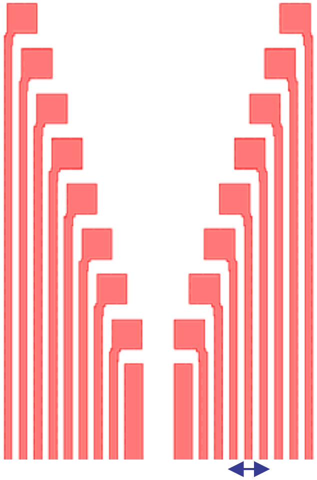
- NAND Flash
- DRAM
- Restricted Logic
- Random Logic

Double line patterning; 32-nm half pitch Flash

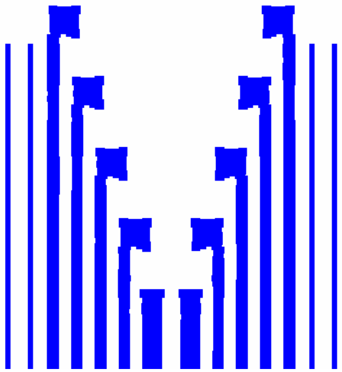
Target
Min Pitch 64nm
k1 = 0.20

SPLIT + OPC

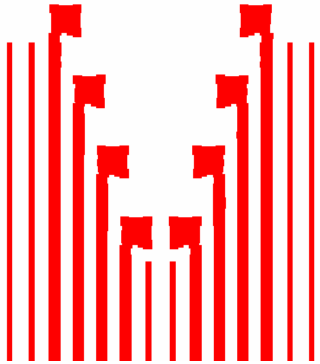
Poly patterning
Annular 0.8/0.5, X-Y polarized
XT:1700i, 193nm - 1.2NA

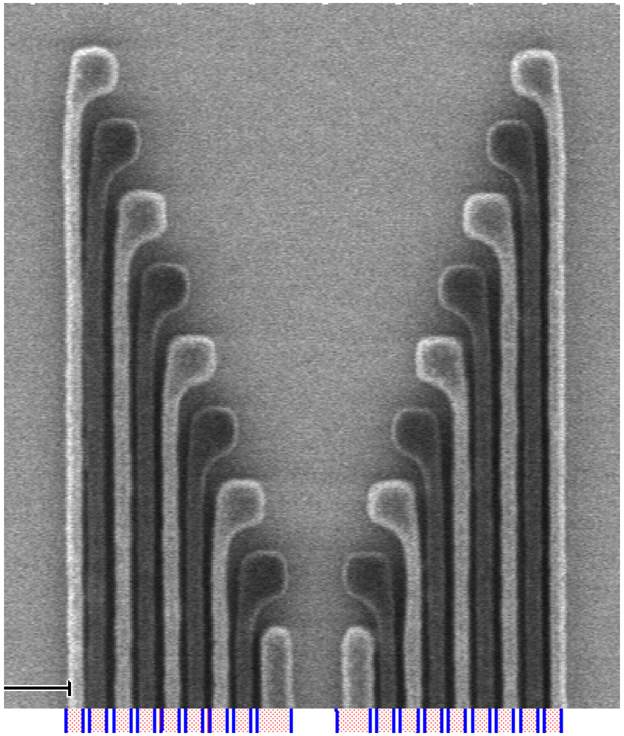

Pitch = 64nm

MASK A

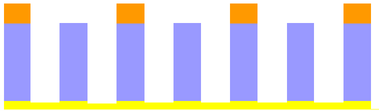


MASK B



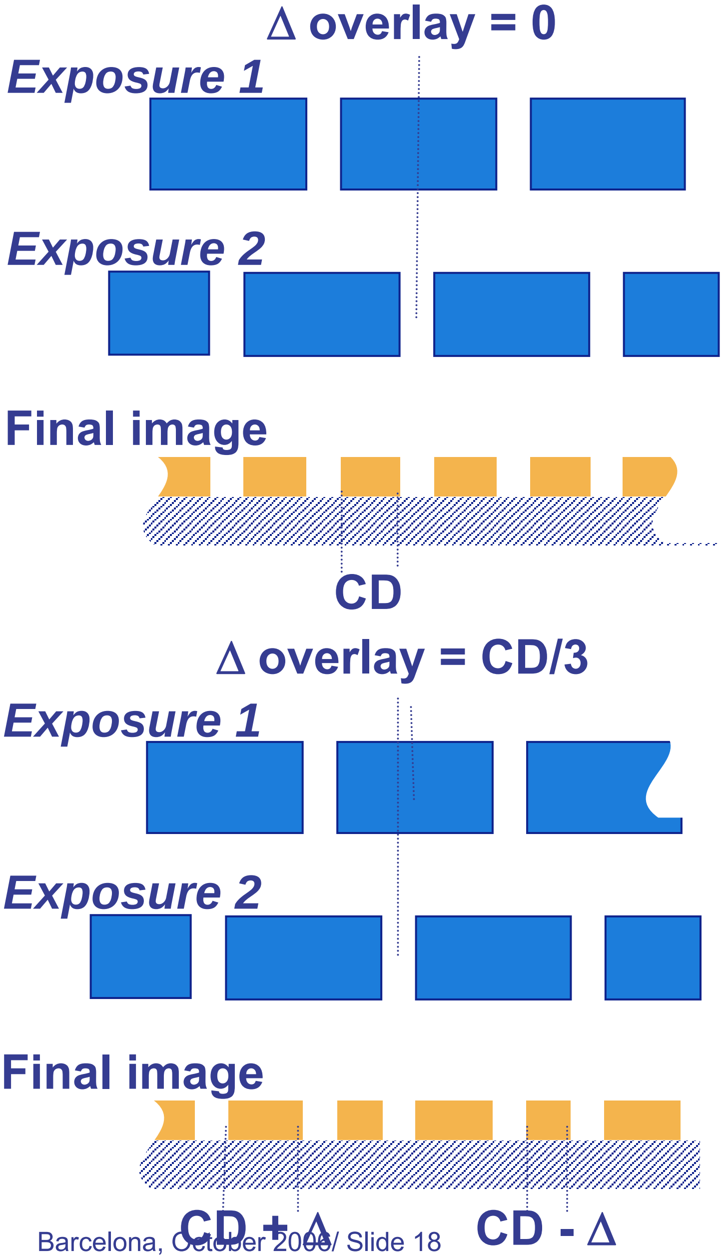


Hard mask
Poly

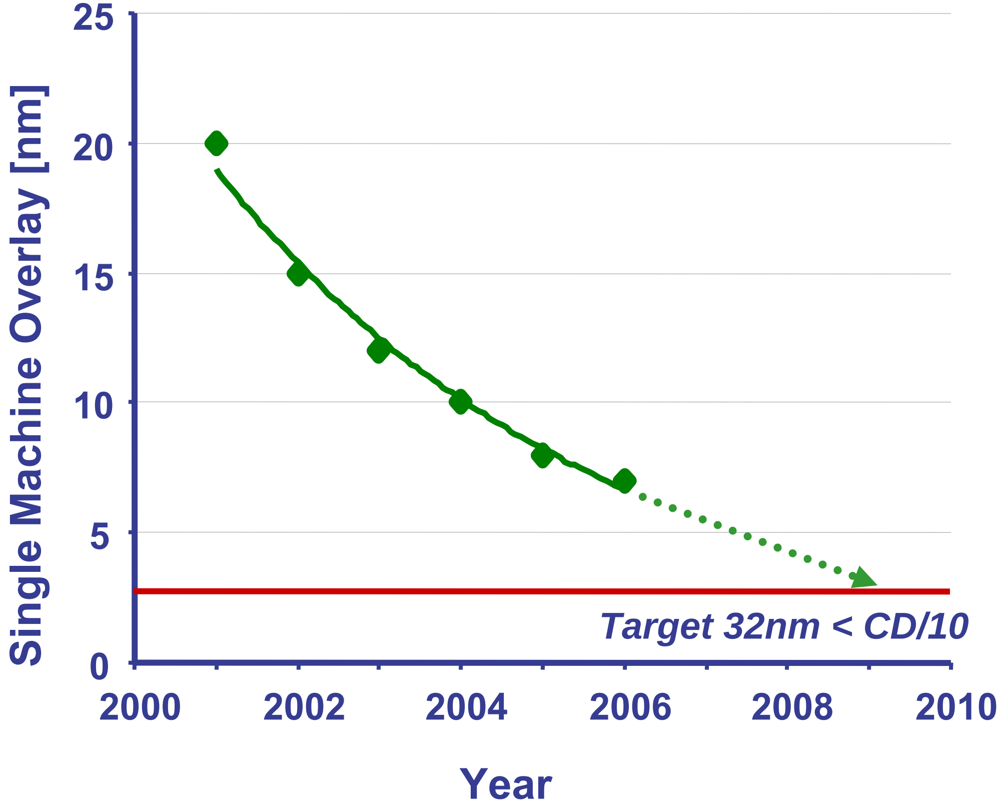


Co work ASML, Imec, Synopsys and Mentor Graphics

Double trench patterning: overlay induced CD change



TWINSCAN™ Overlay Learning

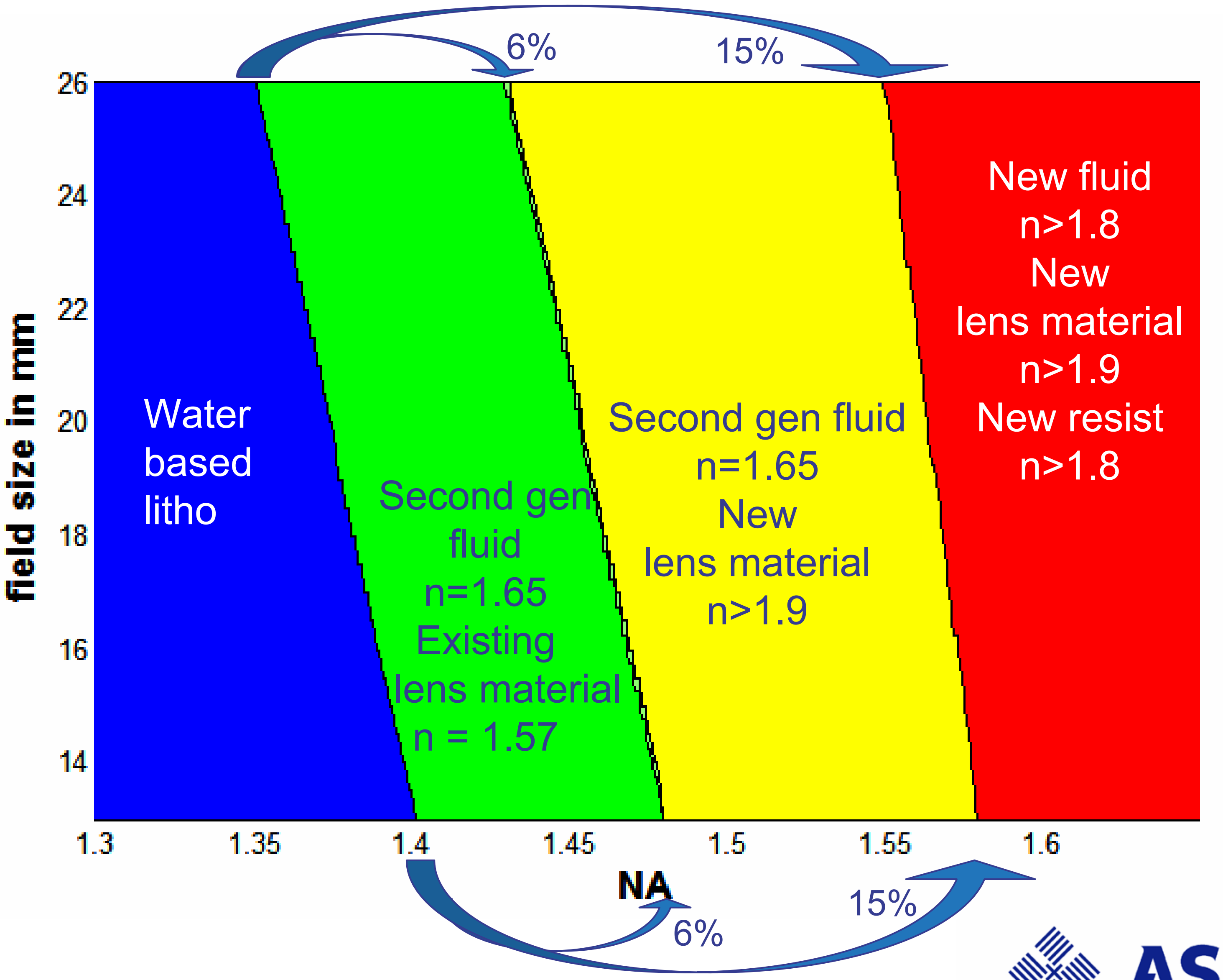


32-nm half pitch with 193 immersion extremely challenging

	half pitch	100	65	45	32	22	16	11
	year		2005	2007	2009	2011	2013	2015
λ [nm]	NA							
248	0.80	0.32						
193	0.93		0.31					
	1.20		0.40	0.28				
	1.35			0.31	0.22	0.15		
	1.55				0.26	0.18		
13.5	0.25				0.59	0.41		
	0.35					0.57	0.41	
	0.45						0.53	0.37

NA 1.55 requires new liquid, new glass to extent to 32nm

Apertures, field sizes and refractive indices



EUV the only high volume opportunity

	half pitch	100	65	45	32	22	16	11
	year		2005	2007	2009	2011	2013	2015
λ [nm]	NA							
248	0.80	0.32						
193	0.93		0.31					
	1.20							
	1.35					0.15		
	1.55				0.26	0.18		
13.5	0.25				0.59	0.41		
	0.35					0.57	0.41	
	0.45						0.53	0.37

EUV required for 32 nm as cost reduction for double patterning and more extendable technology than non water immersion

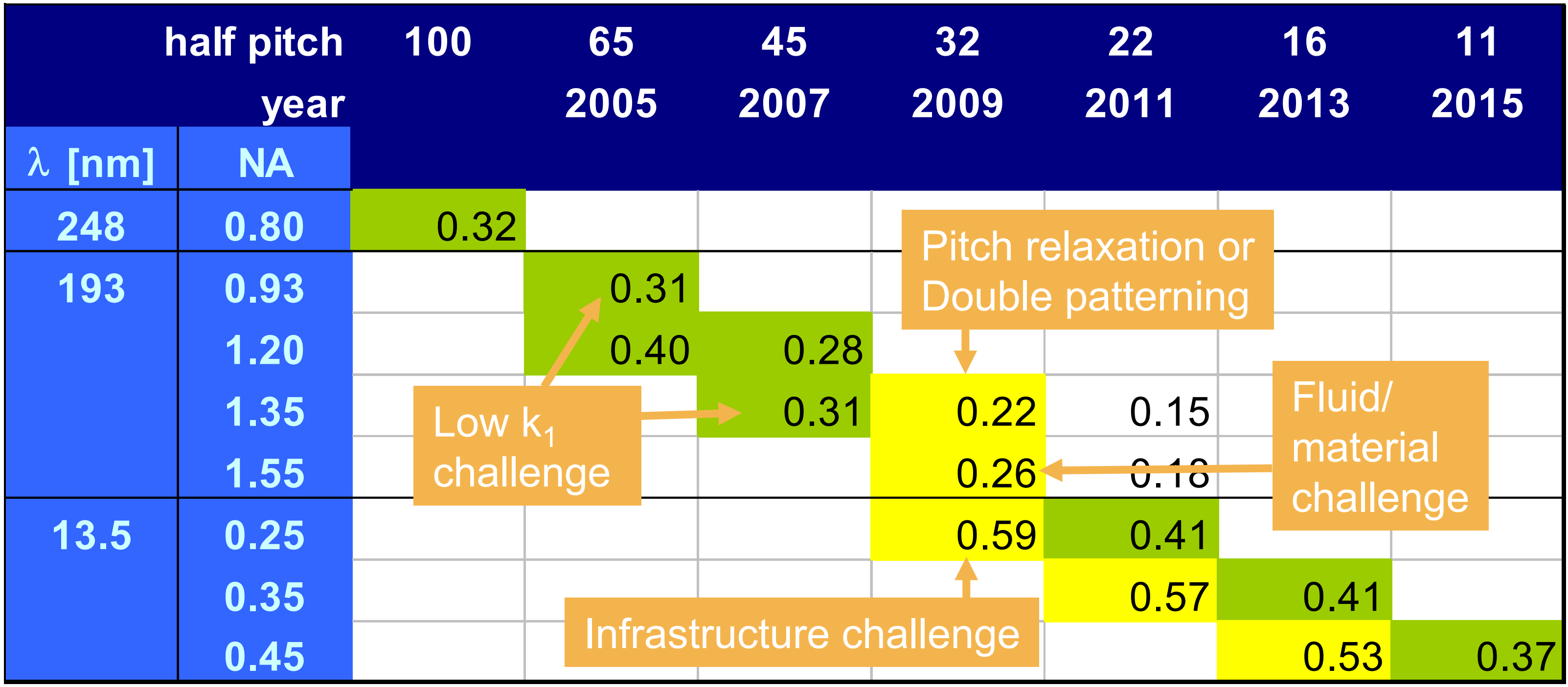
Arrival at IMEC and Albany Nanotech (Aug.’06)

Albany

IMEC

EUV development systems are being installed at two customer sites

Likely technology roadmap



	half pitch	100	65	45	32	22	16	11
	year		2005	2007	2009	2011	2013	2015
λ [nm]	NA							
248	0.80	0.32						
193	0.93		0.31					
	1.20		0.40	0.28				
	1.35			0.31	0.22	0.15		
	1.55				0.26	0.18		
13.5	0.25				0.59	0.41		
	0.35					0.57	0.41	
	0.45						0.53	0.37

Pitch relaxation or Double patterning

Low k_1 challenge

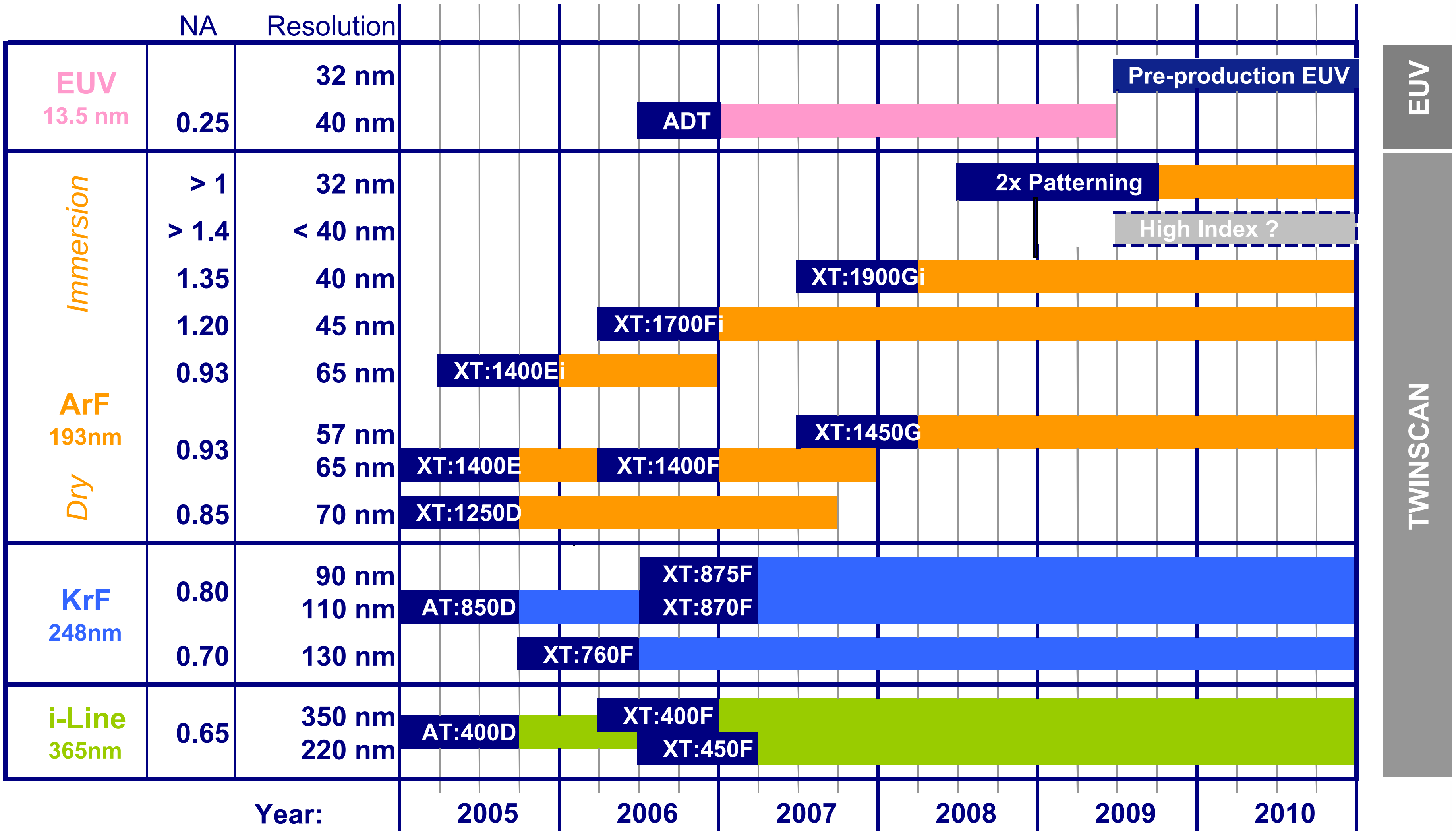
Fluid/ material challenge

Infrastructure challenge

🟩 likely

🟨 opportunity

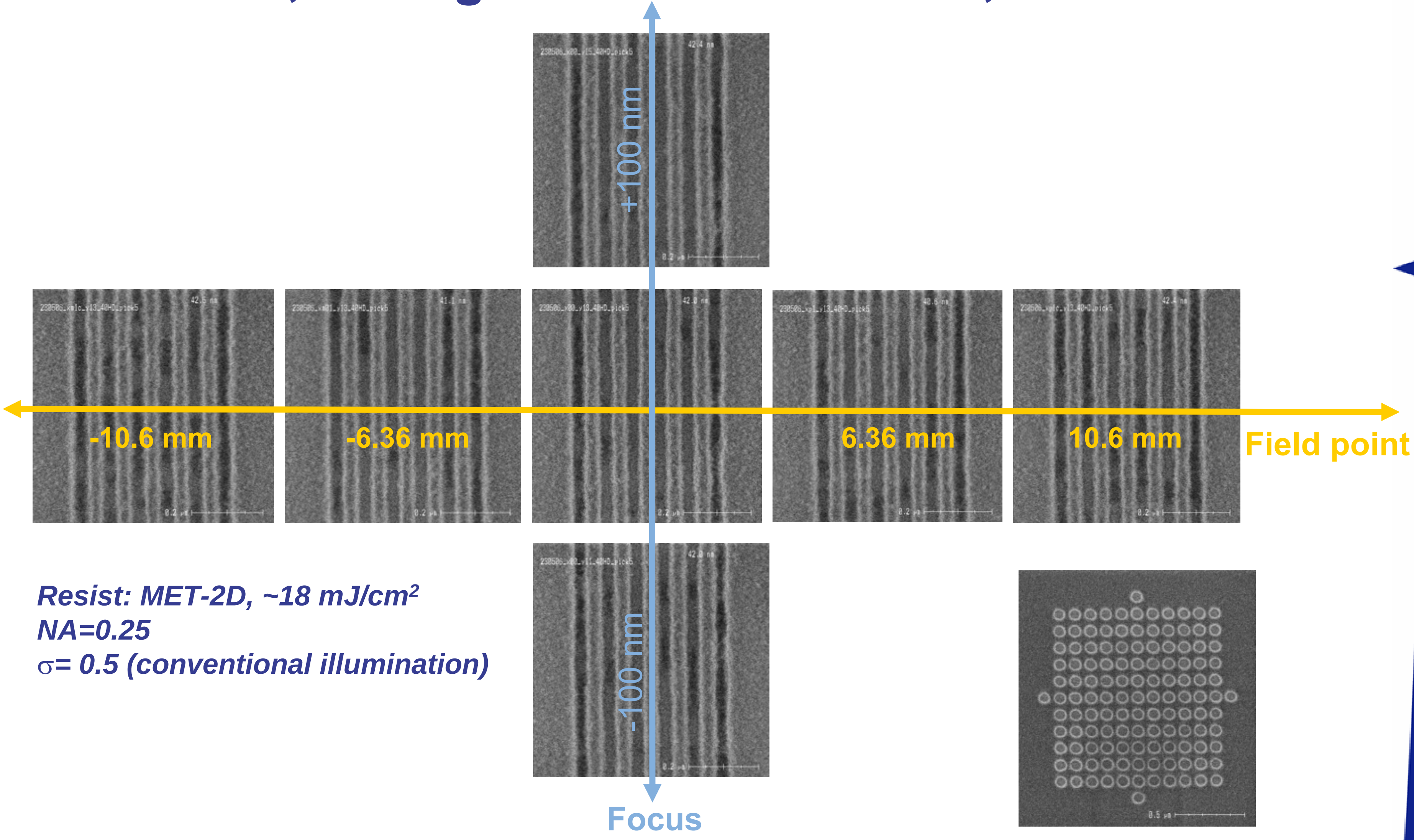
ASML 300mm Product Roadmap



Content

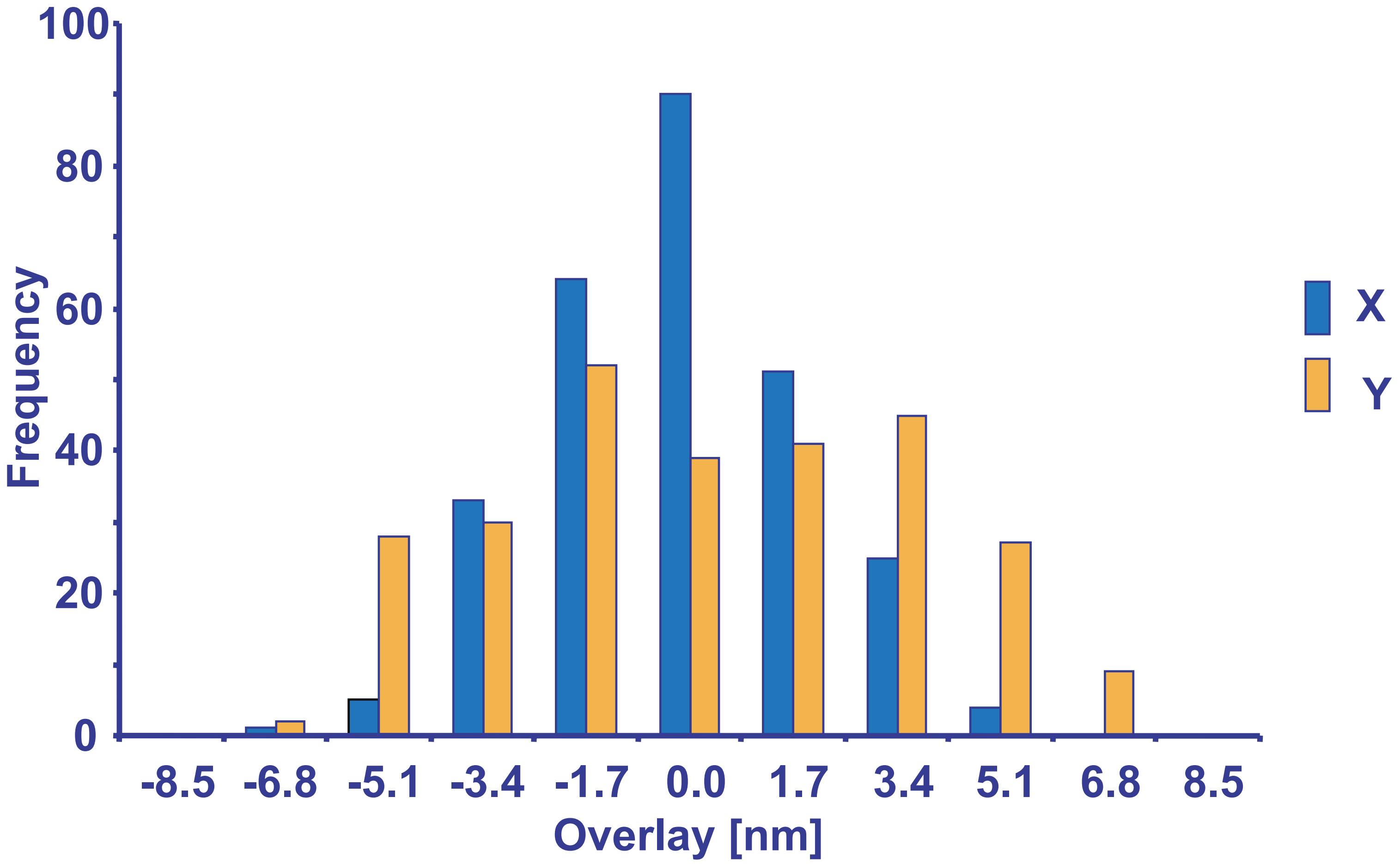
- Lithography will remain key driver for shrink
- Need for shrink continues
- **The only cost effective extendable lithography option: EUV**
- EUV partnering and infrastructure
- Conclusion

Full field, through focus 40-nm lines, 55 contacts



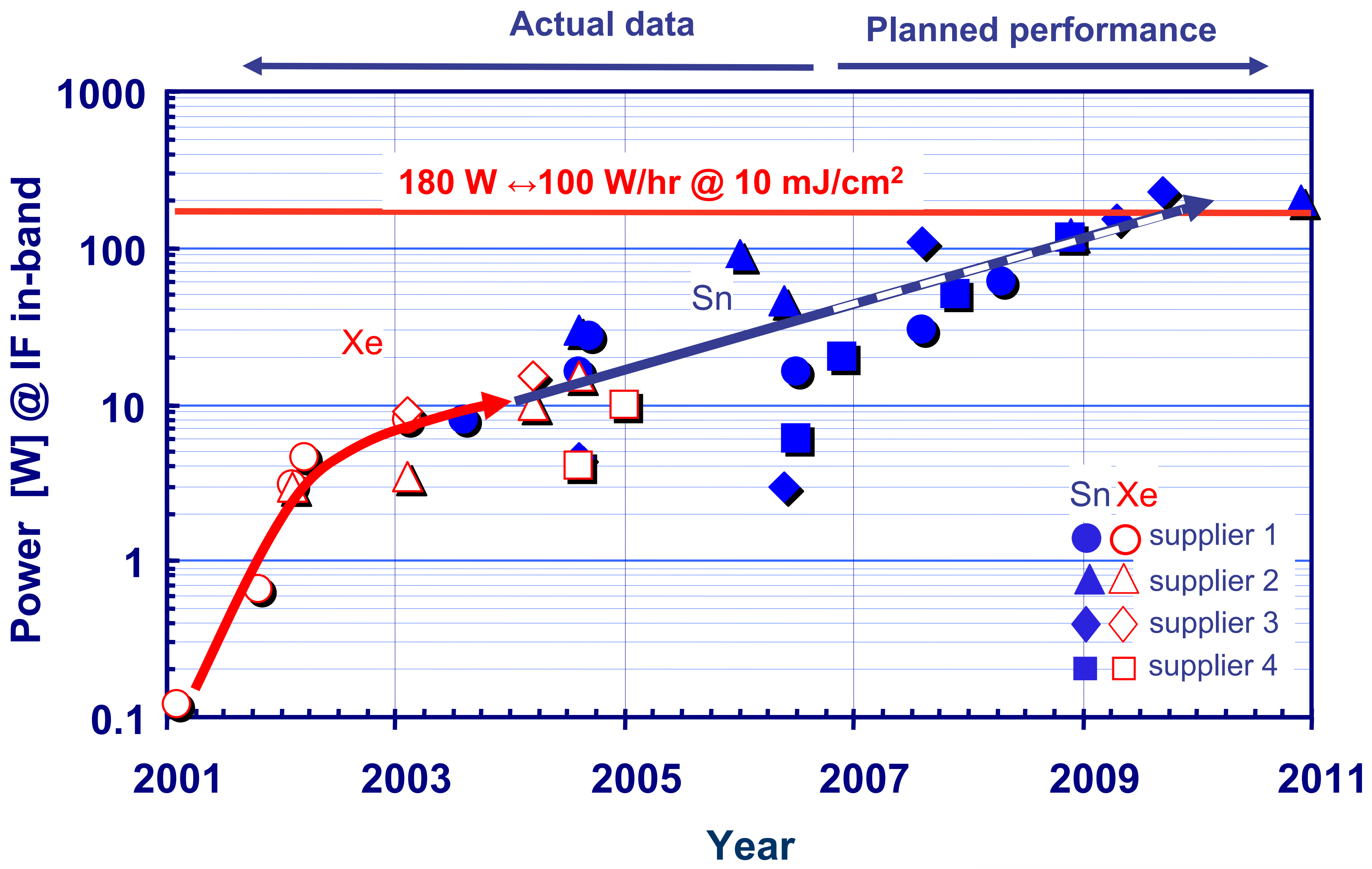
Resist: MET-2D, ~18 mJ/cm^2
NA=0.25
σ= 0.5 (conventional illumination)

Scanning, full field, EUV overlay 7 nm

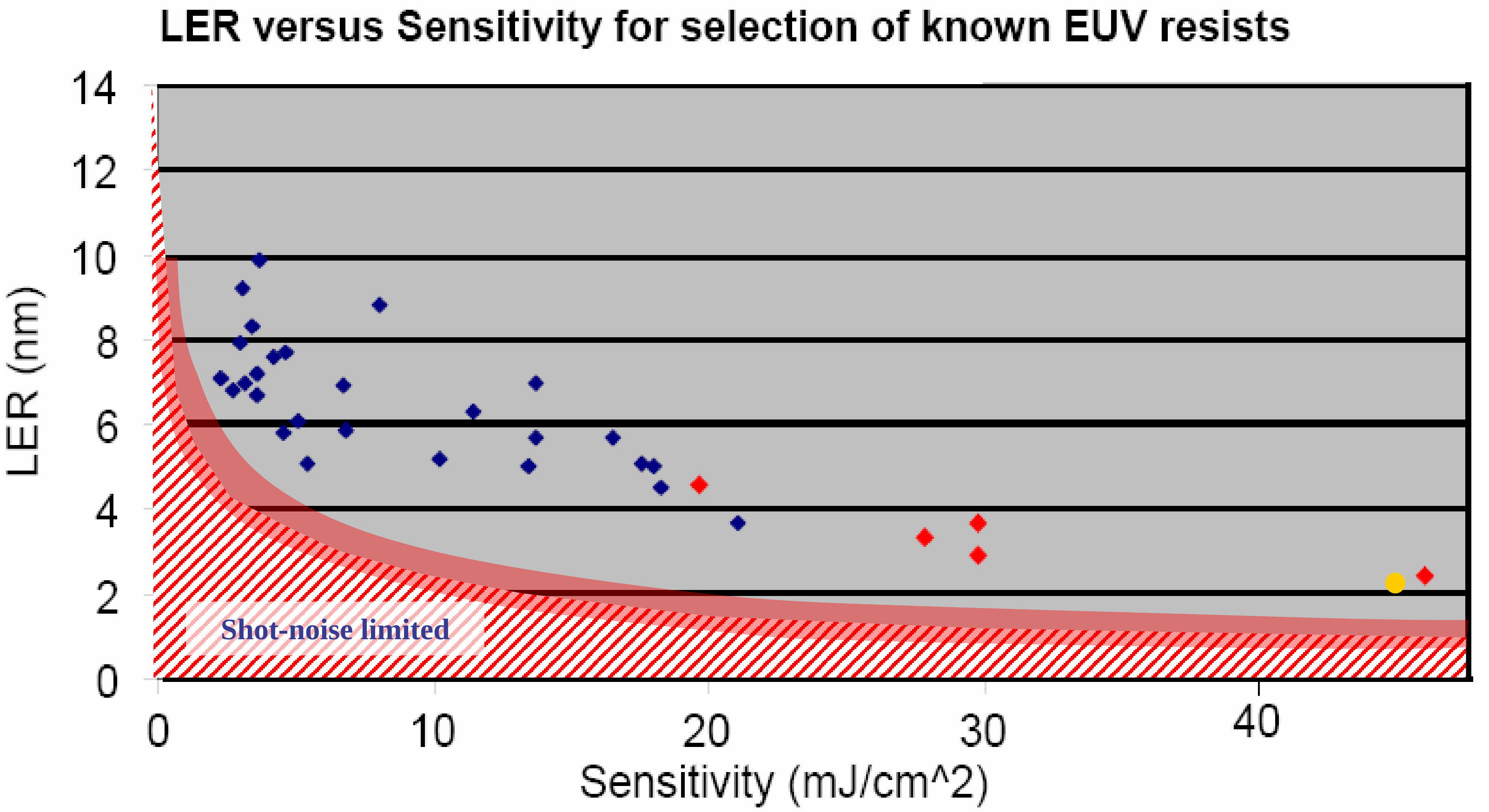


Corrected for X/Y shifts

Source power progress has been increasing



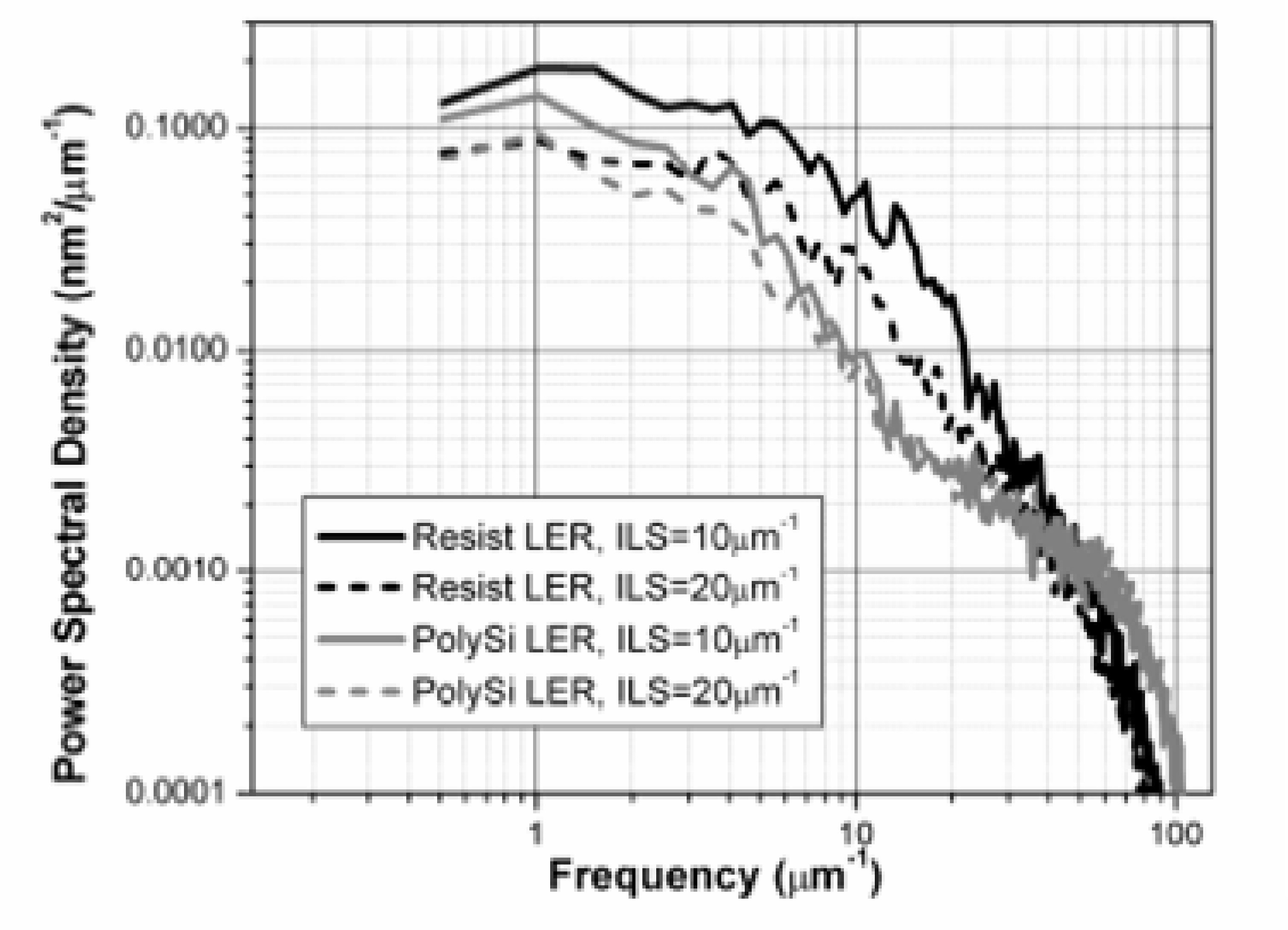
Resist shot noise likely not the Line Edge Roughness limitation


LER versus Sensitivity for selection of known EUV resists

Status: Line Edge Roughness (HVM Spec): < 1.6 nm
Line Edge Roughness (Best Current): ~ 2.3 nm

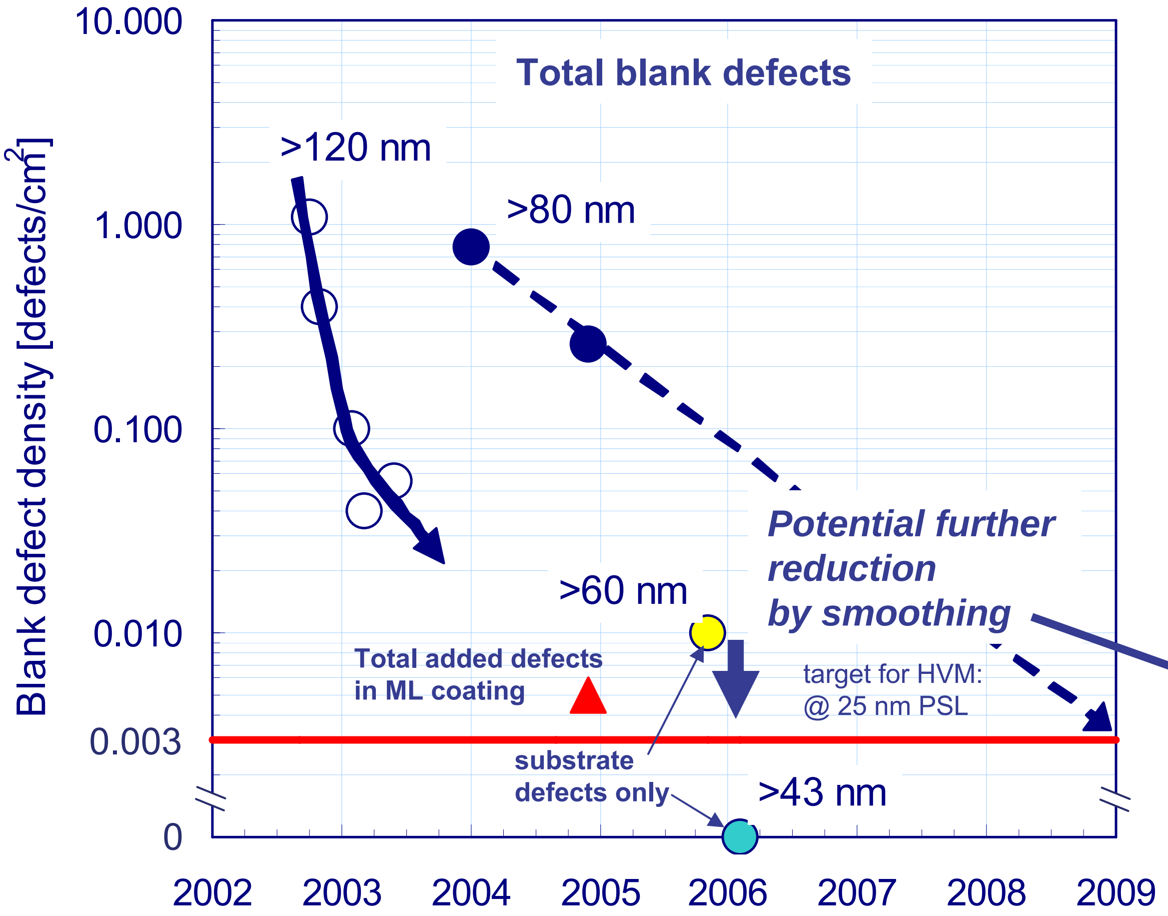
Source: Bruno La Fontaine, IEEE workshop 06

Non litho post processing improved LER

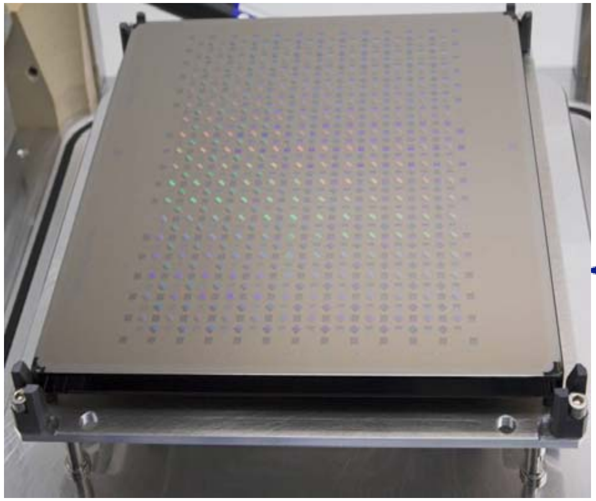


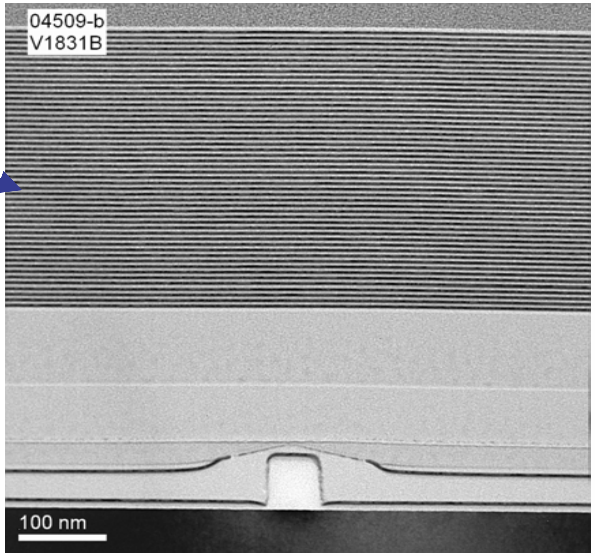
Source Pawloski, SPIE microlithogrphy '06

Progress in blank defect density reduction



EUV test mask

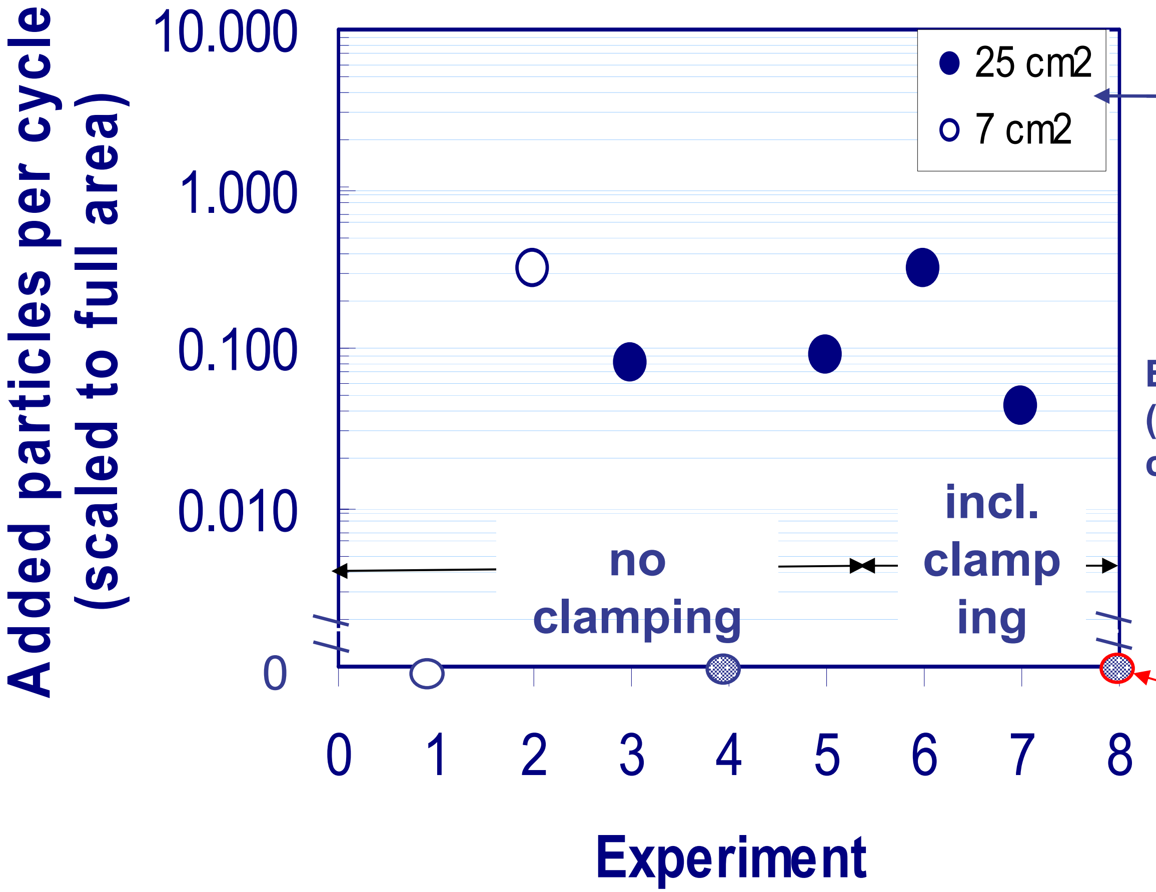




Data from:

- ○● P. Seidel (ISMT), 3rd *International EUVL Symposium*, Miyazaki, Japan (2004).
- ▲ Press release ISMT (*http://www.sematech.org/corporate/news/releases/20041220.htm*), December 20, 2004
- ● Presentation Asahi Corp., 4th *International EUV Symposium*, San Diego, USA (2005).
- ● Solid State Technologies, zero defects >43nm on quartz substrate @ ISMT (20-Feb-2006).

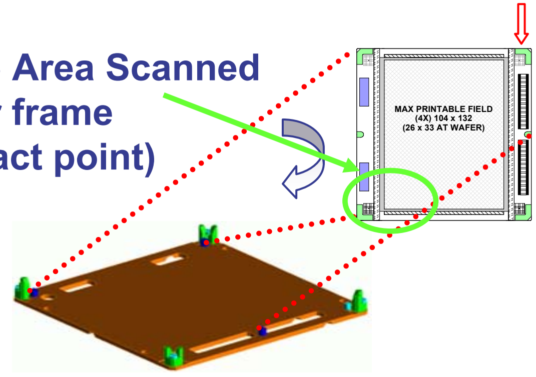
Zero added particles per reticle exchange required



size of scanned area in the measurement (mask active area = 14x14cm^2 ≈ 200cm^2)

particle size: >75 nm

Edge Area Scanned (near frame contact point)



0 added defects After 70 cycles Edge scan

No clear customer consensus for 32 nm, EUV preferred for 22 nm

Customer Lithography preferences for 32 nm & 22 nm (2 year roadmap)

Litho Technology	32nm node / 2009	22nm node/ 2011
ArFi NA = 1.35	2	0
ArFi NA >1.35	3	2
Double Patterning	3	1
EUV	4	8
Other	2	3

EUV preferred for Memory Immersion (single or double exposure) preferred for Logic

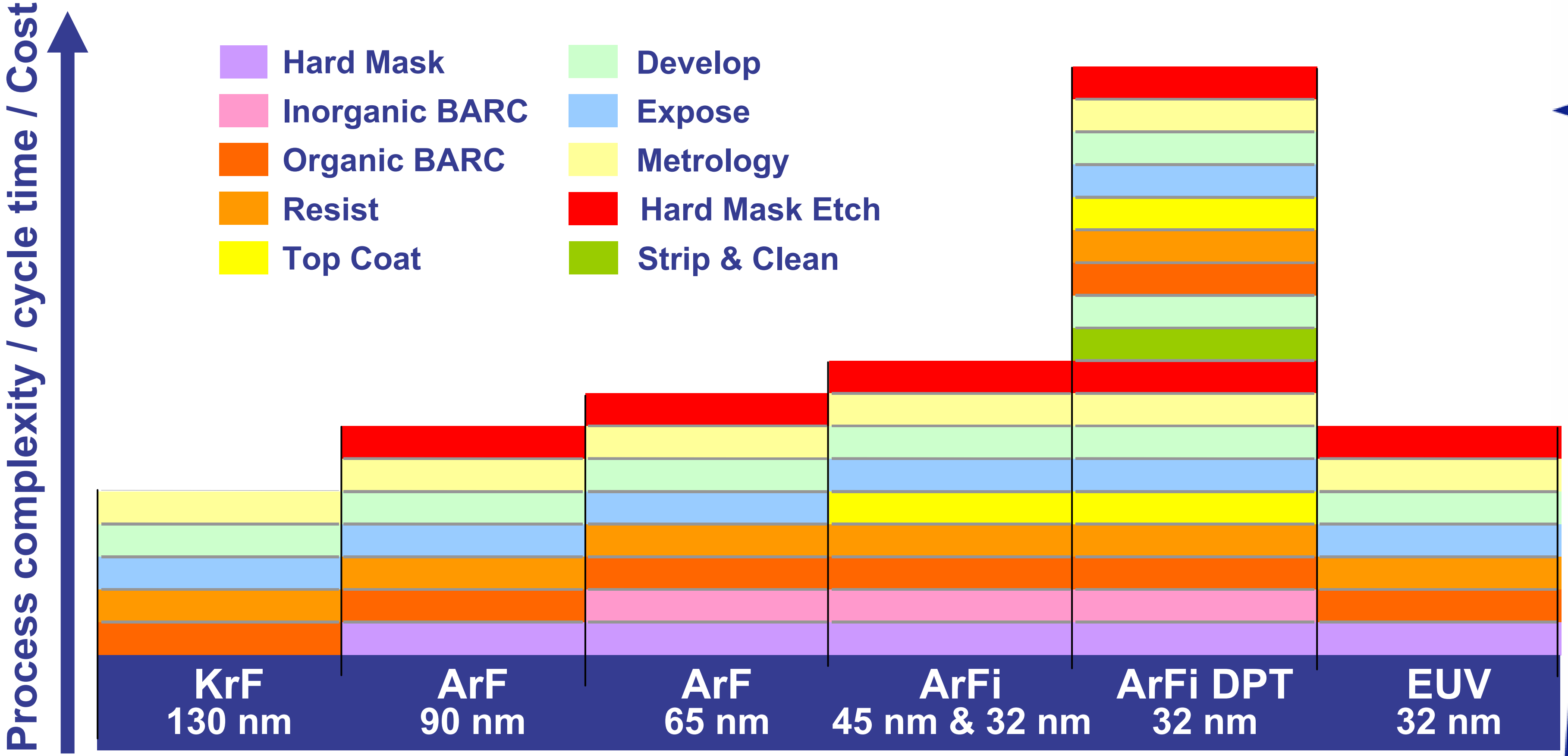
EUV preferred

Poll of 14 customers, ASML 32nm Choices Meeting, San Francisco 24 Jan 06

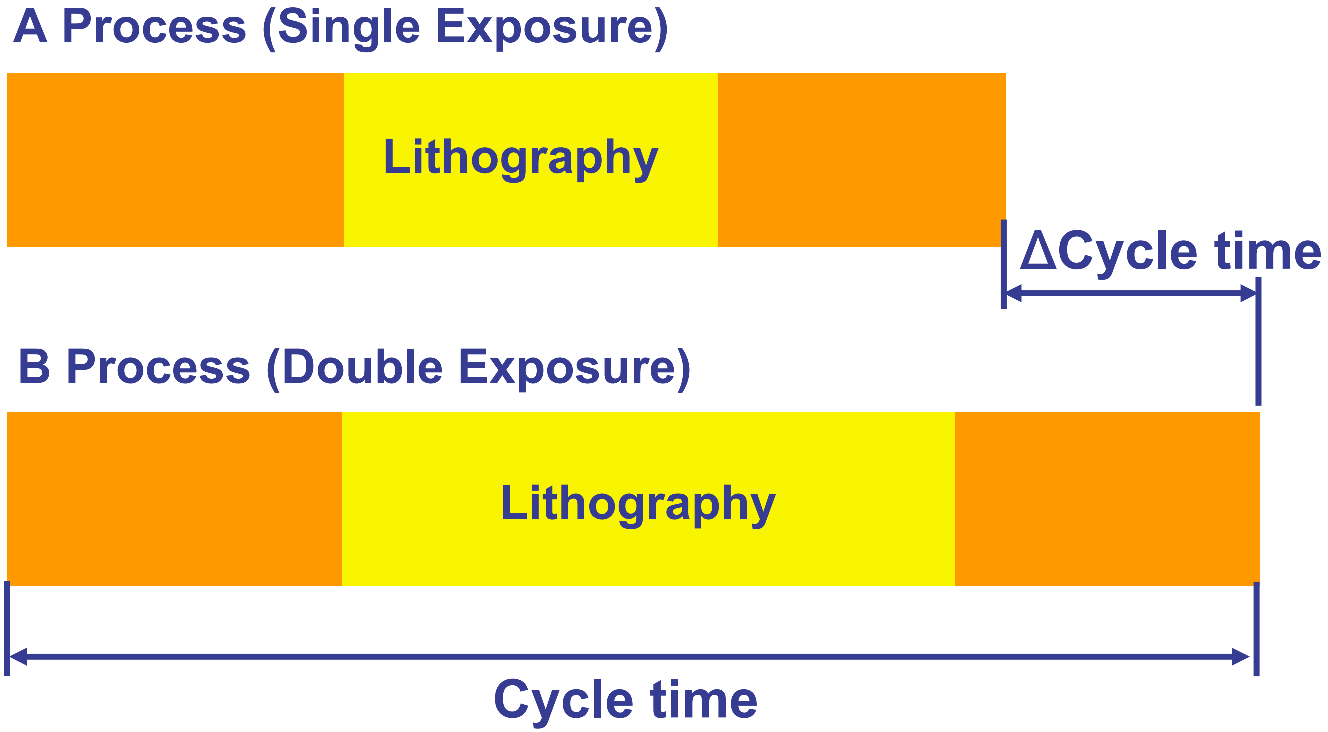
Historic reduction stepper imaging technology changes

Technology	Incubation time [yr]	Production Insertion	Diffraction limit [nm]	Incremental Improvement %
436 nm/air	-	1980	109	-
365 nm/air	3	1989	91	19
248 nm/air	9	1995	62	47
193 nm/air	7	2002	48	28
157 nm/air	Failed	-	39	23
193 nm/water	3	2006	34	44
193 nm/HI	> 6	>2010	29	15
13 nm/ vacuum	>10	>2010	3.3	1031

Increased litho process complexity drives cost



Cycle time of multiple exposure strategies increases



Higashiki, Toshiba, Santa Clara, SPIE march 06

Content

- Lithography will remain key driver for shrink
- Need for shrink continues
- The only cost effective extendable lithography option: EUV
- **EUV partnering and infrastructure**
- Conclusion

EUV at Research Institutes

- In August, ASML shipped EUV Alpha Demo Tools to the College of Nanoscale Science and Engineering (CNSE) of the State University of New York (SUNY) at Albany, N.Y., and to IMEC in Leuven, Belgium.
- ASML is integrating these tools on-site to prepare them for full-system qualification enabling EUV development.
- Major semiconductor base will have EUV access at these sites: STMicron, Philips, Qimonda, Infineon, Intel, IBM, Toshiba, Sony, Freescale, AMD, MEI, NEC, Samsung, TSMC.
- EUV infrastructure will be driven through above developments.

Continuous progress of EUV infrastructure through partners

- Carl Zeiss
- Cymer
- Philips Extreme
- Rohm and Haas Electronic Materials
- Toppan Photomasks
- XTREME technologies

EXTREME ULTRAVIOLET LITHOGRAPHY

EXTATIC, 2001-2005,

EUVSources, 2001-2004,

EXTUMASK, 2001-2004,

EXCITE, 2002-2005,

more Moore: 2004-2006,

“push the limits of lithography to enable
and exceed the requirements for the 22 nm node”

ASML, SIGMA-C SOFTWARE, PHYSTEX, IMAGINE OPTIC, XTREME TECHNOLOGIES, PHILIPS EXTREME UV, FOCUS, EPPRA, XENOCS, SAGEM DEFENSE SECURITE, AMTC, CARL ZEISS SMT, CARL ZEISS LO, PHILIPS, AZEM, MEDIA LARIO, SCHOTT LITHOTEC, TNO, ENEA, IMEC, CEA, TU Delft, Russian Academy of Science: Inst. of Spectroscopy, IPM, UNIVERSITAET MAINZ, NCSR, CNRS, FhG, UNIVERSITAET BIELEFELD, FOM, ELLETRA, University of Burmingham

EUV achievements More Moore consortium

- Sources
  - Introduction of tin as plasma
  - Introduction of rotating disc electrodes
  - Full size transmission Spectral Purity Filter prototype for suppression of out-of-band EUV radiation
- Optics
  - multi layers improvement resulting in 70 % mirror reflectance
  - Demonstration of reduced flare level (10%)
- Work on molecular resists
- System
  - Air gauge flow sensor feasibility in the leveling concept of a 32 nm EUV tool.
- Metrology
  - CD/overlay metrology prototype, demonstrating 32 nm capability
  - Development of a non destructive Photo Emission Electron Microscope suitable for maskblank defect evaluation

EXTREME ULTRAVIOLET LITHOGRAPHY

EXTATIC, 2001-2005,

EUVSources, 2001-2004,

EXTUMASK, 2001-2004,

EXCITE, 2002-2005,

more Moore: 2004-2006.

EAGLE, 2006-2008,

“develop the technology for an EUV lithographic platform for high volume manufacturing”

ASML,
FOM,
Carl Zeiss SMT AG,
Philips EUV,
Xtreme Technologies,
Alcatel,
Sagem,
Media Lario

European Project partners

ADVANCED MASK TECHNOLOGY CENTER

ENEA C.R. Frascati

Sagem Défense Sécurité
Groupe SAFRAN

Imagine Optic

AIS

SIGMA-C

ELDIM

SCHOTT lithotec

Launched by Motorola
freescale semiconductor

Xenocs

ALCATEL THALES

Infineon technologies

AZ Electronic Materials

Universität Bielefeld
Fakultät für Physik

IOM

Fraunhofer Institut
Integrierte Systeme und Bauelementetechnologie

Media Lario Technologies

TU Delft

ST

PTB

eppra
European Pulsed Power Research Applications

FOCUS GmbH
Instruments for Electron Spectroscopy and Surface Analytics

JOHANNES GUTENBERG UNIVERSITÄT MAINZ

FOM

imel

XTREME technologies

ioe

CNRS
CENTRE NATIONAL DE LA RECHERCHE SCIENTIFIQUE

cea leti

PAUL SCHERRER INSTITUT
PSI

INSTITUTE OF SPECTROSCOPY
RUSSIAN ACADEMY OF SCIENCES
1968

PHILIPS

TNO

TASC

JENOPTIK JENA
Laser.Optik.Systeme.

Information Society Technologies

MEDEA+
System Innovation on Silicon

elettra

AIXUV
EUV-Technology

imec

PhysTeX

ZEISS CARL ZEISS SMT

ASML

Content

- Lithography will remain key driver for shrink
- Need for shrink continues
- The only cost effective extendable lithography option: EUV
- EUV partnering and infrastructure
- **Conclusion**

Lithography roadmap

- Water-based immersion will capture the 40-nm half pitch using 1.35-NA 193-nm lithography.
- Non water-based immersion needs new lens materials to increase resolution capability significantly:
  - Without new lens material, new fluid technology full field resolution advantage limited to 6%. Progress not sufficient to give economic return to equipment supplier and its user.
  - New lens material technology availability will push any product implementation beyond 2009.
- EUV technology acceptance is growing but still not ready for production environment.
- Hence double patterning is the only option for production in the 2008-2009 time frame. ASML will support this with sufficient overlay and productivity on their products in time.

The promises of EUV

- Process complexity and cycle time will go up and EUV now becomes a cost and cycle time reduction opportunity. Cost reduction to be achieved by single exposure, single mask and low OPC content.
- EUV mask and process infrastructure will be developed facilitated by the IMEC and Albany program in order to achieve above objective.
- EUV is the main contender for 32 nm and beyond, and the only possible cost effective lithography option with multiple node extendibility.
- ASML has received its first order for EUV pre-production system for delivery in 2009 and is seeking more customers to drive production EUV capability.

ASML

Commitment