Engineering Tests Stand (ETS) Updates: Lithographic and Tool Learning

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outline

Objective: Summarize this year's lithographic and tool learning obtained using the ETS.

- Introduction:
 - Top-level ETS specifications
 - ETS goal and major learning
- Experiments from the ETS user facility
 - Intel
 - AMD
 - Motorola
 - Infineon
- Conclusion



ETS top-level specifications



2003 Antwerp

Major goal for the ETS was to demonstrate the feasibility of EUVL technology

- World's first fully-integrated, full-field scanning EUVL exposure tool designed, built and tested
- → Industry wide recognition of EUVL technology
- All sub systems tested and verified in vacuum
 - LTEM mask substrates
 - Ultra-thin resist process developed to replace TSI approach
 - Highest average brightness laser developed by TRW
 - 40x increase in LPP source power achieved
 - First high-throughput EUV condenser developed
 - Hydrocarbon control in ETS for long-life optics
 - Achieved <3 nm jitter in full-speed scanning maglev stages
 - Control system with 15 controllers and 433 components developed
- No major surprises!!



The ETS has been an important tool to accelerate EUVL learning

Lithographic learning

- Static and scanned imaging
- Flare measurements
- Resist characterization
- Dose control
- Process window measurement
- Reticle characterization

Environmental learning

- Condenser lifetime
- Contamination mitigation
- Projection system lifetime
- In-situ cleaning
- Resist outgassing
- <u>System learning</u>
 - Vibration environment
 - Thermal management
 - Vacuum system development



Source characterization

- Conversion efficiency
- EUV output stability
- Thermal testing
- New source configurations
- <u>Sensor development</u>
 - EUV dose sensors
 - Aerial Image Monitor (AIM)
 - Through-the-Lens imaging
 - New EUV sensor testing



ETS as an user facility

ETS system operation this year has focused on membercompany experiments, but tool learning continued...

- 4 LLC companies performed various experiments to learn EUV specific issues.
 - AMD, Infineon, Intel, and Motorola
- Tool learning continued.
 - Response of system to environmental perturbations
 - Stability of LPP source operation
 - Condenser erosion
 - Dose control using sensor measurements
 - Dose uniformity (scan and cross-scan directions)
 - Reticle e-chuck performance
 - Resist performance
- 10 standard masks were printed with the ETS during the halfyear period



Intel ETS exposure runs

- Flare measurements and characterization
- Flare variation compensation experiments
- Process window measurements with flare
- Line defect study
- Negative tone resist

Manish Chandhok, Wed 10/2, 9:05AM, Optics I

"Measurement of the Impact of Flare on Line Width Roughness and Correlation with Aerial Image Metrics"



Flare characterization: CD sensitivity to flare



Vary window size to increase flare





intel

Flare Variation Compensation (FVC)



Using the model based FVC techniques, the target CD variation can be achieved in the presence of flare.



For the ETS, CD range after FVC = 1.3 nm (a factor 10 decrease)



Infineon ETS Exposure Runs

- Cr and TaN absorber masks
- Process window analysis
- Si and hardmask substrates
- Shot noise investigations



Stefan Hirscher, Wed 10/1, 9:45AM, Tool I

"Advances in EUV Lithography Development for Sub-50nm DRAM Nodes"





Cr & TaN Absorber Mask Performance Comparison



Performance of Cr- and TaN-absorber masks comparable

Ultimate resolution limit: 70 nm

Process Window Comparison of Simulation and Experiment

nfineon



Wafer process consumes 25 – 50 % of the process window
IMPROVE RESIST PROCESS

Motorola ETS exposure runs

- Process window study for iso and dense features
- Printing of SRAM bitcells
- Line-end shortening measurements
- Flare compensation experiments
- Defect printability study





CD's as a Function of Nominal Size and Pitch through Defocus



- Process windows limited by more isolated features (min. DoF for $k_1 = 0.75$ is ~ 1.25 μ m)
- For 32nm node technology, 1D-OPC may be required for CD control, independently of flare compensation





SRAM Bitcell Lithography

First demonstration of SRAM bitcell printing with EUV lithography.





- Drawn line size = 100 nm, drawn pitch = 340 nm
- No OPC applied
- Measured line size = 100 nm





AMD ETS exposure run

 Comparison of imaging performance with a Cr/SiO₂ absorber mask and an etched-multilayer binary mask (EMBM).



EUVL Symposium 2003 Antwerp

Comparison of Cr/SiO₂ mask with etchedmultilayer binary mask (EMBM)



Masks used

Schematic of shadowing effect

ETS prints in the center of the process window

Shadowing effect – Larger H-V bias observed for

Larger H-V bias observed for absorber masks than for etched-multilayer masks (EMBM)

Current status and future of ETS

- The main chamber of the ETS has been put to sleep as of July 2003.
- High-power laser-produced plasma operation continues to support condenser erosion studies supported by International SEMATECH.
- All equipment will be maintained intact for the immediate future.



ETS wins 2003 R&D 100 award





Key message

The ETS completed its original task. Two years of the ETS operation has shown that EUV has no surprises!

- All aspects of EUV lithography have been successfully demonstrated in the ETS– components, metrology, masks, control, etc.
- Various experiments were performed by LLC member companies, and much lithographic learning has been obtained.
- All lithographic experiments have been verified with modeling.



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