Recent progress of EUV blanks development

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Outline

• Challenges in EUV mask blanks
• HOYA roadmap
• Defect reduction in ML
  • Killer defects
  • Mitigatable defects
• Other parameters
• Summary
Challenges in EUV mask blanks

- Defect control in Absorber
  - Reflectivity
  - Patterning

- Defect control in Ru cap layer
  - Durability

- Defect control in Mo/Si multilayer
  - Reflectivity
  - Uniformity
  - Stress
  - Roughness

- Defect control on LTEM substrate
  - Flatness control
  - Local slope
  - CTE

- Defect control in Backside film
  - Durability (mechanical performance)
  - Adhesion
  - Resistivity
Challenges in defect reduction

- Most of the challenges in EUV mask blanks are in defects.
- But defects are not unique to EUV. Defect reduction and stable supply are essential to lithography blanks in general.
- HOYA is the only blanks supplier that covers optical (ArF, KrF), EUV, and LCD.
# Technology relationship

<table>
<thead>
<tr>
<th>ArF blank technology</th>
<th>EUV blank technology</th>
</tr>
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<tbody>
<tr>
<td>Defect control of quartz</td>
<td>Defect control of LTEM</td>
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<tr>
<td>Defect control of Mo/Si multilayer</td>
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<tr>
<td>Defect control of films</td>
<td>Defect control of films</td>
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<tr>
<td>• Ta binary (ABF)</td>
<td>• Ta alloy absorber</td>
</tr>
<tr>
<td>• Cr absorber (TFCx, EBTx)</td>
<td>• CrN backside film</td>
</tr>
<tr>
<td>Flatness (~200nm, single side)</td>
<td>Flatness (~30nm, both sides)</td>
</tr>
<tr>
<td>Methodology tools</td>
<td>Methodology tools</td>
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<tr>
<td></td>
<td>ABI</td>
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<tr>
<td>DUV control</td>
<td>DUV reflectivity control</td>
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<td></td>
<td>EUV reflectivity control</td>
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<tr>
<td>Matured production engineering. Commitment to HVM.</td>
<td>Automated blank manufacturing line.</td>
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</table>
## EUV Blanks General Roadmap (2012~2018)

<table>
<thead>
<tr>
<th>CY</th>
<th>2012</th>
<th>2013</th>
<th>2014</th>
<th>2015</th>
<th>2016</th>
<th>2017</th>
<th>2018</th>
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</thead>
<tbody>
<tr>
<td>Exposure tool plan</td>
<td></td>
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<tr>
<td>Pilot line</td>
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<tr>
<td>HOYA EUV blank</td>
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</tr>
<tr>
<td>Defects [SEVD]</td>
<td>≤30 @55nm</td>
<td>≤30 @30nm</td>
<td>≤30 @25nm</td>
<td>≤30 @23nm</td>
<td>≤30 @21nm</td>
<td>≤30 @19nm</td>
<td>≤30 @17nm</td>
</tr>
<tr>
<td>Flatness</td>
<td>80 nm</td>
<td>60 nm</td>
<td>40 nm</td>
<td>30 nm</td>
<td>30 nm</td>
<td>30 nm</td>
<td>30 nm</td>
</tr>
</tbody>
</table>

- **PPT: NXE3100 (27nmhp)**
- **HVM: NXE3300B/3350B (22-16nmhp)**

**EUV Blanks Improvement/Development**

- Built EUV Line [New IBD, Automated line etc.]

**EUV Blanks Improvement/Development**

- Key EUV Blanks for 22-16nmhp
  - Low defect ML blank
  - High substrate flatness

- CA resist
- Ta alloy absorber
- Ru_A cap
- Mo/Si multilayer (ML)
- Backside film: CrN

* Target values are in general. It depend on layers
What is defect control in multilayer?

1. Killer defect control
   • A defect going across patterns, unrepairable.
   • It has to be zero.

2. “Mitigatable” defect control
   • Defect mitigation with fiducial marks

Developed effective FM process

- FM image
- Repeatability in JBX

- Defect repair technologies demonstrated in BACUS 2015
ML Blank Defect Reduction Strategy

**Small defects**  [Phase defects]

**Large defects**  [Amplitude defects]

**Target:** \( \leq 30@23\text{nm} \) in 2015

Zero killer defects

**ML Blank Defects**

Defect source of small defects:
- Pit: Caused by polishing process
- Bump: Residual material

Defect source of large defects:
- Mostly caused by IBD process
- Particle from Inner parts
- Peeling off from shields

- HOYA is doing continuous process improvement to meet the target
- ML deposition process using IBD: Shield, Target, Condition etc.
- Polishing and Cleaning process on Substrate.

HOYA
HOYA EUV Blank Defect Reduction Trend (High Grade)

Defect counts in 100x100mm

- @60nmSiO2
- @25nmSEVD
- @34nmSEVD
- @23nmSEVD

Defect counts


EUVL symposium 2015
HOYA Ru-ML Blank Defect Quality
(Teron, High grade)

Area: 132x104mm (max. exposure area)

**Plate #1**
- 7 defects: >25nm SEVD
- 8 defects: >23nm SEVD

**Plate #2**
- 3 defects: >25nm SEVD
- 7 defects: >23nm SEVD
Killer defect control

"Killer defect free" yield

H2/13  H1/14  H2/14  H1/15  H2/15

Killer (large-sized) defects are well controlled.
Substrate Flatness Quality Trend Update

Flatness trend (2007-2014)

Average flatness of high class substrate in each year

- Substrate flatness has been steadily improving to around 30nm.
- 20nm Flatness was demonstrated in current polishing line.

Actual spec should be decided through feedback of IP error on wafer.
## BOW control options: Backside film

<table>
<thead>
<tr>
<th>Back side Film</th>
<th>CrN Standard (Production)</th>
<th>CrN</th>
<th>TaB</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thickness</td>
<td>20nm</td>
<td>70nm</td>
<td>70nm</td>
</tr>
<tr>
<td>Sheet Resistance</td>
<td>&lt;100 Ohm/sq.</td>
<td>&lt;100 Ohm/sq.</td>
<td>&lt;100 Ohm/sq.</td>
</tr>
<tr>
<td>Bow Target</td>
<td>500nm</td>
<td>&lt;300nm</td>
<td>&lt;150nm</td>
</tr>
<tr>
<td>ASML Requirement</td>
<td>Passed</td>
<td>Passed</td>
<td>Passed</td>
</tr>
</tbody>
</table>

**Typical bow quality**

- 508nmBow
- 262nmBow
- 52nmBow

ASML Requirement: Passed
Summary

Defect performance:
• It is still one of the largest challenges, but significant progress has been achieved in quality and yield.
  • Killer defects
  • Mitigatable defects

Other key parameters and metrology:
• Challenges to measurement tool accuracy.
• Litho impact estimation to clarify relevant specification.
• Escalation of inspection cost.

To move forward to HVM:
• Increased run-rate. Positive cycle for improvement.
• Support from stakeholders for investment toward HVM.
Thank you for your attention!