IEUVI Organization

IEUVI Board

Chair: Paolo Gargini ITRS
Organizer: Yumiko Takamori IEUVI/Intel
Kurt Ronse, IMEC (EU), Stefan Wurm, SEMATECH (US), Ichiro Mori, EIDEC

IEUVI Technical Working Groups (TWG)

Mask ITWG

Long He,
Jim Wiley, John Zimmerman,
Frank Goodwin, Pawitter Mangat,
Obert Wood, Markus Bender,
Takashi Kamo,

Resist ITWG

Yu-Jen Fan
Serge Tedesco (EU) CEA / LETI
Patrick Naulleau (US) LBNL
IEUVI Mask ITWG
October 26, 2014, Washington DC., USA

TWG Committee/co-Chairs:
Long He, Jim Wiley, John Zimmerman,
Frank Goodwin, Pawitter Mangat, Obert Wood,
Markus Bender, Takashi Kamo,
<table>
<thead>
<tr>
<th>Start</th>
<th>Finish</th>
<th>Topic</th>
<th>Topic Lead</th>
</tr>
</thead>
<tbody>
<tr>
<td>2:00 PM</td>
<td>2:15 PM</td>
<td>Introduction</td>
<td>Long He (SMT/Intel)</td>
</tr>
<tr>
<td>2:15 PM</td>
<td>2:30 PM</td>
<td>Lasertec EUV Mask Inspection Tool Activities</td>
<td>Hiroki Miyai (Lasertec)</td>
</tr>
<tr>
<td>2:30 PM</td>
<td>2:45 PM</td>
<td>Mask Blank Multilayer Defect Mitigation with ABI Tool</td>
<td>Hidehiro Watanabe (EIDEC)</td>
</tr>
<tr>
<td>2:45 PM</td>
<td>3:00 PM</td>
<td>SEMI P48 Fiducial Mark Standard Status</td>
<td>Long He (SMT/Intel)</td>
</tr>
<tr>
<td>3:00 PM</td>
<td>3:15 PM</td>
<td>Mask Blanks: Moving Towards HVM</td>
<td>Frank Goodwin (SMT)</td>
</tr>
<tr>
<td>3:15 PM</td>
<td>3:40 PM</td>
<td>--- break ---</td>
<td></td>
</tr>
<tr>
<td>3:40 PM</td>
<td>3:55 PM</td>
<td>Gudeng EUV Carrier Progress Update</td>
<td>Paul Chen (Gudeng)</td>
</tr>
<tr>
<td>3:55 PM</td>
<td>4:10 PM</td>
<td>Entegris EUV Carrier Progress Update</td>
<td>Huaping Wang (Entegris)</td>
</tr>
<tr>
<td>4:10 PM</td>
<td>4:25 PM</td>
<td>EUV Pellicle Working Group Update</td>
<td>Chris Krautschik (Intel)</td>
</tr>
<tr>
<td>4:25 PM</td>
<td>4:40 PM</td>
<td>Berkeley MET Tool Upgrade: Scope and Status</td>
<td>Patrick Naulleau (LBNL)</td>
</tr>
<tr>
<td>4:40 PM</td>
<td>5:00 PM</td>
<td>Round Table Discussion</td>
<td>All</td>
</tr>
<tr>
<td>5:00 PM</td>
<td></td>
<td>Adjourn</td>
<td></td>
</tr>
</tbody>
</table>
IEUVI Mask TWG: Broad Representation

About 66 attended last Mask TWG, representing over 36 companies

Regional representations of companies

- Asia-Pacific: 17
- EU: 7
- US: 12

Attendance and company representation
Mask TWG Mission & Objectives

Mission:
Ready EUV mask technology and infrastructure for high volume manufacturing

Objectives:
- Identify mask technology and infrastructure gaps for EUVL implementation
- Build consensus for industry action
Key EUV Mask Challenges for HVM (February 2014)

Mask Infrastructure mostly is NOT ready.

- Capability to detect and verify defects at needed sensitivities is not ready, for mask, mask blank, and mask substrate.
- Capability to mitigate mask blank defects is not ready.
- Capability to prevent masks from particulate contamination is not ready.

HVM solution for mask blanks is NOT available.
Mask Blanks: Moving Towards HVM

Frank Goodwin\textsuperscript{1}, Alin Antohe\textsuperscript{1}, Patrick Kearney\textsuperscript{1}, Long He\textsuperscript{1,2},
HoJune Lee\textsuperscript{1,3}, Dave Balachandran\textsuperscript{1}, Anil Karumuri\textsuperscript{1},
Stefan Wurm \textsuperscript{1,4}, Kevin Cummings\textsuperscript{1}

1: SEMATECH, 257 Fuller Road, Albany, NY 12203
2: Intel Corporation, 2200 Mission College Blvd. Santa Clara, CA 95054
3: SAMSUNG, San #16 Banwoi-Dong, Hwasung-City, Gyeonggi-Do 445-701 Korea
4: GLOBALFOUNDRIES, 2600 Great America Way, Santa Clara, CA 95054
Recent Mask Program Successes

SEMATECH Achieves Breakthrough Defect Reductions in EUV Mask Blanks (Press Release: May 6, 2014)

- Confirmed IBD capable of depositing mask blanks with 0 defects at size > 100nm (SiO2 equivalent)

Details and further achievements presented during Symposium

- EUV Mask Blank Manufacturing Solution Within Reach: Immediate Challenges; Long He, SEMATECH/Intel (Invited)
  - Session 2: Monday 11:15 AM – 11:40 AM
- Recent Advances in Mask Blank Deposition and Defect Reduction; Frank Goodwin, SEMATECH
  - Session 11: Wednesday 4:10 PM – 4:30 PM
IBD Defect Trend [2003- present]
Mask blanks processed at SEMATECH

Mask Blank Defect Density Trend (@>73nm SiO₂ equiv.)

- Defect density of all defects per mask blank
- Includes substrate and handling defects
- Data is measured on the LaserTec M1350 over 14.2x14.2cm² area

• EUVL Mask Blank Production for HVM
  - Improvements needed to meet industry defect requirements
  - Large size “Killer” defects still present
  - Recent gains where made with the substrate quality
  - IBD multilayer process yields are not good

EUVL Symposium
Substrate challenges

The majority of total mask blank defects originate from substrate defects and are decorated during deposition. Simultaneously meeting substrate finish, figure (flatness), roughness and defect specifications is a significant challenge.

- Substrates are amorphous in nature, making it difficult to control CMP.

Reaching figure and finish specifications requires several iterations between global and local polish.

- This creates defects such as scratches or embedded particles.

The surface physical and chemical properties are modified by the polish steps and do interact with the cleaning processes.

- Tight management and control between final polish and cleans to ensure cleaning does not introduce additional defects.
**Substrate Defects**

**Majority of substrate defects are not detected during inspection**

- Most defects only become visible after ML deposition due to decoration
- Deposition techniques have been developed to enhance decoration of substrate defects
  - Indirect measurement – population sampling
  - Adds to cycle time and reduces learning cycles
  - Adds complexity to data analysis

**Enhanced substrate inspection capability is needed**

- Current technology **not able to detect sub-35nm pits** (SiO₂ equiv.) or shallow scratches
- Plans for actinic inspection tools will not address this gap
Progress has occurred

- SEMATECH has recently demonstrated significant EUV mask blank multilayer yields on both total- and adder-defects (Si-capping).
  - 4% yield of total-defect free mask blank multilayers, @54nm, SiO2-equivalent
  - ~40% yields on ≤3 total-defects, @80nm
  - ~80% yields on ≤3 adder-defects, @80nm
  - Good correlation between EIDEC and IMEC on inspected and printed mask defects

A manufacturing solution for EUV mask blanks is within reach. Improvements in both tooling and deposition technologies are required.

(Reassessment will be needed when inspection capability becomes available below 50nm.)
EUV Pellicle Working Group (PWG) Update

Oct 26, 2014

Pawitter Mangat, Ph.D., MBA
GLOBALFOUNDRIES, Inc

Christof Krautschik
Intel Corporation

Acknowledgements: M. Goldstein, Intel Corporation
Pellicles have a long history of protecting reticles. The proof of concept for full field pellicles is being led by ASML. The Working Group will help to facilitate and guide the pellicle commercialization and align the industry on necessary development and infrastructure activities.
Full field pellicle realized, imaging performance unaffected as evaluated by joint effort by NXE users an half field pellicle.
## EUV Pellicle Requirements

### HVM EUV pellicle requirements vs. status (July ‘14)

<table>
<thead>
<tr>
<th>Item</th>
<th>Full size proto expected (Phase 1 targets)</th>
<th>Current status (July ‘14)</th>
<th>HVM Requirement</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pellicle material requirements</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pellicle film EUV transmission</td>
<td>&gt; 80% single pass</td>
<td>86% (Half size)</td>
<td>90% single pass</td>
</tr>
<tr>
<td>EUV transmission spatial non-uniformity (half range)</td>
<td>&lt; 0.4%</td>
<td>0.6 % (50x50mm)</td>
<td>&lt; 0.4%</td>
</tr>
<tr>
<td>EUV intensity in scanning slit @ pellicle</td>
<td>&gt; 1.5 W/cm² (80 W)</td>
<td>1.8 W/cm² (&gt; 80% survivability)</td>
<td>5 W/cm² (250 W)</td>
</tr>
<tr>
<td>Lifetime</td>
<td>~160 hrs</td>
<td>5 hrs (heatload test)</td>
<td>~315 hrs</td>
</tr>
<tr>
<td>Pellicle + frame requirements</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Standoff distance during scanning</td>
<td>2 ± 0.5 mm</td>
<td>2 ± 0.5 mm</td>
<td>2 ± 0.5 mm</td>
</tr>
<tr>
<td>Max. acceleration during scanning</td>
<td>50 m/s²</td>
<td>50 m/s²</td>
<td>100 m/s²</td>
</tr>
<tr>
<td>Max. ambient pressure rate of change</td>
<td>n/a (open frame; film-feasibility only)</td>
<td>n/a (open frame)</td>
<td>&lt; 3.5 mbar/s</td>
</tr>
<tr>
<td>Pellicle frame width</td>
<td>5 mm</td>
<td>5 mm</td>
<td>2 mm</td>
</tr>
<tr>
<td>Pellicle impact on imaging performance [CDU over a wafer]</td>
<td>&lt; 0.3 nm @ 27 nm L/S</td>
<td>0.15 nm @ 27 nm L/S</td>
<td>&lt; 0.1 nm @ 22nm LB/S later 16 nm L/S</td>
</tr>
</tbody>
</table>

ASML will:
- continue further improvement of pSi film material properties
- investigate frame concepts for pellicle integration

Semicon West PWG update, 2014
Potential Impact Areas

(1) Pellicle Spec./Materials
- Reticle design manual
- Mask writer?
- Nomenclature

(2) Frame/Vents/Filters
- Frame design/Spec.
- Filter solution
- Adhesive / outgassing

(3) Mounting/adhesives
- Pel. Removal / Re-Pel.
- Tooling and process dev.
- Qualification tools

(4) Particles
- Specs
- Qualify shedding
- Qualify membrane
- Removal/repair

(5) Carrier Impact/Handling
- Inner POD redesign
- Qualification
- New Metrology tools

(6) Inspection / AIMS
- Mask requirements
- Maximum volume claim
- Testing and qualification

(7) Lifetime/Long-term stability
- Membrane robustness
- AMC on Mask surfaces
- Back side Cleans with Pel

Other—Standards, ASML-Customer-Supplier Ownership
Engagement Plan Status

✓ Engagements in progress

➤ Pattern Mask Inspection: KLA-Tencor; Carl Zeiss
  ❑ Compatibility with Handling critical

➤ Handling: Gudeng; Entegris
  ❑ Shipping of masks with pellicles-Current Gap (needs to be included)

✓ Independent Engagements between Suppliers/Customers

➤ Pellicle Suppliers: Mitsui and FST
  ❑ Strategy to ship pellicles needs to be included

✓ Open for Engagement, when needed

➤ Characterization: EUV Technologies, TNO

➤ Pellicle Inspection & Mounting: Lasertec, Rorze (New Tool proposal)

➤ Cleaning: Suss MT-Pro (Gen3 -in Design)

➤ Specific pellicle FOCUS projects: IMEC/Sematech/CNSE

✓ Direct engagement with ASML: Availability of pellicle membrane samples
RESIST
<table>
<thead>
<tr>
<th>Time</th>
<th>Session</th>
<th>Speaker</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:30 AM - 8:00 AM</td>
<td>Registration and Continental Breakfast</td>
<td></td>
</tr>
<tr>
<td>8:00 AM - 8:10 AM</td>
<td>Welcome and Introductions</td>
<td>Y. Fan, SEMATECH</td>
</tr>
<tr>
<td>8:10 AM - 8:30 AM</td>
<td>ASML Update</td>
<td>N. Harned, ASML</td>
</tr>
<tr>
<td>8:30 AM - 8:50 AM</td>
<td>SEMATECH outgas testing update</td>
<td>Y. Fan, SEMATECH</td>
</tr>
<tr>
<td>8:50 AM - 9:10 AM</td>
<td>EIDEC outgas testing update</td>
<td>E. Shiobara, EIDEC</td>
</tr>
<tr>
<td>9:10 AM - 9:30 AM</td>
<td>NIST Outgas Testing update</td>
<td>R. Berg, NIST</td>
</tr>
<tr>
<td>9:30 AM - 9:50 AM</td>
<td>imec outgas testing update</td>
<td>I. Pollentier, imec</td>
</tr>
<tr>
<td>9:50 AM - 10:10 AM</td>
<td>IBM outgas testing update</td>
<td>D. Goldfarb, IBM</td>
</tr>
<tr>
<td>10:10 AM - 10:20 AM</td>
<td>Discussion</td>
<td>S. Inoue, EIDEC &amp; All</td>
</tr>
<tr>
<td>10:20 AM - 10:30 AM</td>
<td>Break</td>
<td></td>
</tr>
<tr>
<td>10:30 AM - 10:50 AM</td>
<td>ITRS Roadmap updates</td>
<td>M. Neisser, SEMATECH</td>
</tr>
<tr>
<td>10:50 AM - 11:10 AM</td>
<td>Negative tone molecular EUV resist</td>
<td>A. Robinson, University of Birmingham</td>
</tr>
<tr>
<td>11:10 AM - 11:30 AM</td>
<td>Secondary electrons study</td>
<td>G. Denbeaux, CNSE at SUNY Poly</td>
</tr>
<tr>
<td>11:30 AM - 11:50 AM</td>
<td>TEL Process Optimization Update</td>
<td>T. Saito, TEL</td>
</tr>
<tr>
<td>11:50 AM - 12:00 PM</td>
<td>EUV Photoresist Contrast Curve microtool</td>
<td>R. Perera, EUV Technology</td>
</tr>
<tr>
<td>12:00 PM - 12:10 PM</td>
<td>Summary and discussion</td>
<td>Y. Fan, SEMATECH</td>
</tr>
<tr>
<td>12:10 PM</td>
<td>Lunch</td>
<td></td>
</tr>
</tbody>
</table>
## Outgas Tools Status and Throughput

<table>
<thead>
<tr>
<th>Test site</th>
<th>Status</th>
<th>Samples tested in 2013</th>
<th>Current Throughput (samples/month)</th>
</tr>
</thead>
<tbody>
<tr>
<td>NIST</td>
<td>up</td>
<td>25</td>
<td>14</td>
</tr>
<tr>
<td>EIDEC</td>
<td>up</td>
<td>167</td>
<td>20 - 30</td>
</tr>
<tr>
<td>imec</td>
<td>up</td>
<td>36</td>
<td>20</td>
</tr>
<tr>
<td>SEMATECH</td>
<td>up</td>
<td>164</td>
<td>20 – 30*</td>
</tr>
<tr>
<td>Total</td>
<td></td>
<td>392</td>
<td>74 - 94</td>
</tr>
</tbody>
</table>

* Based on 12/7 operation

- **Industry request: 250 per month, same as MET tools**
Resist Imaging Performance Tracking

- First round 2014 results don’t show any improvement in photospeed to LWR/CDU tradeoff
- Resists with higher outgassing that meet the new ASML specification are just starting to be tested
- Two resist producers (Dow and Kumho) have reduced effort on developing new EUV resists
- Some of novel resist materials have shown promising results
Design of Experiment and Results

- Labels: PAG - PU - Quencher throughout the entire experiment
- Each resist component has high and low concentration, and higher concentration leads to higher outgassing was expected
- CG (nm) is linearly scaled with dose from the first screening
Conclusion

- SEMATECH EUVT continues to deliver sufficient tool usage for member company resist outgas testing
- RR test is still on-going and key parameters have been identified
- Facilitate novel resist outgas testing
- Continue to work with all resist suppliers towards family test
  - We believe SEMATECH is the first group to certify a resist family with WS-based outgas test, press release underway
  - ASML agreed that 3 samples per family is sufficient for all resist suppliers (LHH, MHH, HHH), and next goal would be 1 sample per resist family for all resist suppliers
  - Does this help EUV resist development?
Collaborative Work on Reducing Inter-Site Gap

- imec, NIST, SEMATECH and EIDEC have been proceeding the collaborative work to reduce the inter-site CG gap under the advisory of ASML just after we recognized the big gap in RR2.

- We concluded one of the potential root causes of the gap is most likely from the gap of the average wafer temperature among test sites and the violation of contamination limited regime (non-CLR).
  
  ✓ Three test sites have measured the wafer temperature using wireless wafer thermometer (SensArray), and one site will measure very soon.

  → Around 29-30 deg as representative temperature

  ✓ All sites have evaluated 5 model resists for comparing CG, analyzing the correlation with outgassing and checking CLR.

  → Need to increase EUV/EB power to obtain CLR for the new criteria (CG < 10-nm).

  → Need more discussion on RGA analysis

- We also agreed to match the factor A/PS among the test sites. (A: exposure area, PS: pumping speed)

  → imec confirmed the effect of A/PS matching.
Meeting Summary and Action Items

- **Round robin testing update**
  - Potential root causes of the gap is most likely from the gap of the average wafer temperature among test sites and the violation of CLR
  - Commercial EUV resist needed for calibration
  - New common area / pumping speed proposed. Tentative schedule posted.

- **Family testing update**
  - Experimental results verified through multiple resist families. Boundary condition for PAG, PU, and quencher defined.
  - 3 samples (LHH, MHH, HHH) per family is sufficient for all resist families
  - 1 sample per family for all resist suppliers needed

- **CAR material improvement needed**
  - Higher outgas material for imaging evaluation

- **Non-CA material outgas testing**
  - Reduced thickness allowed
  - Testing procedure are being investigated
**Photo condensed Molecular Metal Oxides - inpria**

- **Tin** not present in any significant different quantity versus the control.
- **Outgassing** is inline with CAR resists specs - procedure for non-CAR still to be developed.

1. Waiver from ASML to print up to 20 wafers on imec NXE3100
2. Gen2a, Gen2b sample exposed
3. Now exploring new samples with higher contrast

---

### 1st round (March '14)

<table>
<thead>
<tr>
<th>VPD-ICP-MS</th>
<th>at/cm²</th>
</tr>
</thead>
<tbody>
<tr>
<td>Detection Limit (at/cm²) DL</td>
<td>1.00E-10</td>
</tr>
<tr>
<td>Control, Not processed (at/cm²)</td>
<td>8.00E-09</td>
</tr>
<tr>
<td>Monitor, back-side (pre-coat) (at/cm²)</td>
<td>6.00E-09</td>
</tr>
<tr>
<td>Monitor, front-side (pre-coat) (at/cm²)</td>
<td>4.00E-09</td>
</tr>
<tr>
<td>Monitor, back-side (post-coat) (at/cm²)</td>
<td>2.00E-09</td>
</tr>
<tr>
<td>Monitor, front-side (post-coat) (at/cm²)</td>
<td>2.00E-09</td>
</tr>
</tbody>
</table>

**PASSED**

### 2nd round (July '14)

<table>
<thead>
<tr>
<th>VPD-ICP-MS</th>
<th>at/cm²</th>
</tr>
</thead>
<tbody>
<tr>
<td>Detection Limit (at/cm²) DL</td>
<td>7.00E-10</td>
</tr>
<tr>
<td>Control, Not processed (at/cm²)</td>
<td>8.00E-09</td>
</tr>
<tr>
<td>Monitor, back-side (pre-coat) (at/cm²)</td>
<td>6.00E-09</td>
</tr>
<tr>
<td>Monitor, front-side (pre-coat) (at/cm²)</td>
<td>4.00E-09</td>
</tr>
<tr>
<td>Monitor, back-side (post-coat) (at/cm²)</td>
<td>2.00E-09</td>
</tr>
<tr>
<td>Monitor, front-side (post-coat) (at/cm²)</td>
<td>2.00E-09</td>
</tr>
</tbody>
</table>

**PASSED**

### Cleanable contamination

<table>
<thead>
<tr>
<th>Exposure</th>
<th>Sn at%</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.00</td>
</tr>
<tr>
<td>2</td>
<td>0.01</td>
</tr>
<tr>
<td>3</td>
<td>0.04</td>
</tr>
</tbody>
</table>

**RGA:**
- All spectra suggest no non-cleaneable elements (metal) in the outgassing, only hydrocarbons.

---

**Non-cleanable contamination**

- XPS-test Sn at%
  - 1: 0.00
  - 2: 0.01
  - 3: 0.04 (5σp3)

**XPS testing indicates no significant amount of Sn in the WS contamination!**

---

**22HP - 50 mJ/cm² Gen2a resist 1st expo in NXE3100**

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EUVL Symposium
ON GOING EIDEC-IMEC COLLABORATION

- **EIDEC tasks:**
  - EUVL mask with IMEC layout on a commercially available blank (good compromise quality). **Blank preparation and mask making** arranged among EIDEC members.
  - Provide the full set of **actinic blank inspection** results obtained on ABI tool (including size info and/or ways to sort the data) and patterned mask inspection results.

- **Imec tasks:**
  - **Expose** this mask on **NXE3100** using standard resist process
  - Run **wafer inspection** followed by repeater analysis
  - **Correlate the results** to the EIDEC provided inspection data (both in forward and backward sense)
Question: Where are we?
EUV: Past, Present and Future

- 1985. First papers on EUV
- 1991. First demonstrations
- 1995. Why is this fab circular?
- 1996. The Nat Lab are shutting down EUVL!
- **2001.** EUV LLC Demonstration.
  - IEUVI Started (EUV LLC, ASET)
- 2002. First EUVL Symposium
- 2006. First 2 prototypes shipped
- **2010.** First NXE shipped
- 2013. 8w/hr, 55W demonstrated
- **2014.** 500w/day, 80W demonstrated, NA>0.5 concept
- **201X.** HVM?
BUT INDUSTRY IS NEVERTHELESS CONTINUING TO MAKE PROGRESS
Incubation Time

Strained Silicon
→ 1992->2003

HKMG
→ 1996->2007

Raised S/D
→ 1993->2009

MultiGates
→ 1997->2011

~ 12-15 years
CMOS Future Directions

1970-2004

Traditional Scaling

2005-2014

Equivalent Scaling

2000-2014

Integrated Solutions

2010-20XX

New Devices

2010-20XX

More Moore

70% / 2-3year

Features

70% / 2-3year

SOC, SIP, 3D

2X Performance / 2-3year

Nanotech

From My Files

ITRS 7/11/1998

EUVL Symposium
Nanoelectronics: An International Perspective

By Mihail C. Roco
NSF and NNI

Paolo Gargiul
ITRS Chairman
Intel

Discoveries and innovations in nanotechnology are flourishing worldwide. Centers of excellence and research networks with long-term programs supporting nanoelectronics, nanomagnetics, and nanophotonics have been created in the United States (U.S.), Europe, Japan, and other parts of the world. The National Nanotechnology Initiative (NNI) has provided a long-term scientific focus, a partnership approach, and a means of environmentally responsible funding the field in the United States since 2000. The program also inspired and partially motivated nanotechnology R&D activities in about 60 other countries. Creative programs of similar investment scale are underway in Europe and Asia. In Europe, the FP7 program organizes all the EU research initiatives including in nanoelectronics into four categories: Cooperation, Ideas, People, and Capacities. For each objective, there is a specific program corresponding to the main areas of EU research policy. In addition, a European Commission program in Future Emerging Technologies (FET) addresses the disruptive approaches to nanoelectronics. In Japan, the Ministry of Education, Culture, Sports, Science, and Technology (MEXT) promotes nanotechnology research and development and supports a network among researchers to provide cross-sectional, comprehensive support across research institutions and research fields. For example, MEXT also provides opportunities for outside researchers to use large and special facilities and equipment. Japan also has the New Energy and Industrial Technology Development Organization (NEDO), which contributes research and development activities in a variety of nanoelectronic programs, e.g., their Next-Generation Semiconductor Materials and Process Technology (MIRAI) Project.

In the first ten years, the research focus in the U.S. has been on uncovering nanoscale phenomena and on synthesizing nanostructured components to improve existing products. For illustration, researchers and man...
Device and Architecture Outlook for Beyond CMOS Switches

Many new devices that are being studied as replacements for CMOS are discussed in this paper; early results for benchmarking and performance comparison are presented for some of the devices.

By Kerry Bernstein, Fellow IEEE, Ralph K. Cavin, III, Life Fellow IEEE, Wolfgang Porod, Fellow IEEE, Alan Seabaugh, Fellow IEEE, and Jeff Welser, Senior Member IEEE
Switching Time and Energy, Closer Look

- Limited by Capacitor charging
- Limited by spin dynamics
- Potentially Nonvolatile
- Steep turn-on/off (TFETs)
- Magneto-electric

Diagram showing a graph with axes labeled 'Energy, fJ' and 'Delay, ps', with markers for different technologies such as GpnJ, SpinFET, CMOS LP, HJTFET, IIIvTFET, gnTFET, SWD, STT/STT, STOlogic, ASLD, NML, CMOS LP, SMG, STTtriad. The graph illustrates the trade-offs between energy consumption and delay for different technologies.
2013 ITRS ITWGsa

1. System Drivers
2. Design
3. Test & Test Equipment
4. Process Integration, Devices, & Structures
5. RF and A/MS Technologies
6. Emerging Research Devices
7. Emerging Research Materials
8. Front End Processes
9. Lithography
10. Interconnect
11. Factory Integration
12. Assembly & Packaging
13. Environment, Safety, & Health
14. Yield Enhancement
15. Metrology
16. Modeling & Simulation
17. MEMs
The Device Roadmap is Very Healthy!
SOC: The Ultimate Customizable Building Block

- SOC Design methodology
  - Define required functionalities to enable product
  - Select building blocks to provide the required functionality
  - Assemble the building blocks in a single die

- Assemble the components from characterized fabrics

- Wire them up and determine yielded cost and overall test and packaging costs

Multiple dice are combined in a single die at the required functionality

Year 2001
EUVL Symposium
MM+MtM=Heterogeneous Integration

More than Moore: Diversification
- Analog/RF
- Passives
- HV Power
- Sensors
- Actuators
- Biochips

Baseline CMOS: CPU, Memory, Logic
- 130nm
- 90nm
- 65nm
- 45nm
- 32nm
- 22nm
- 16nm

Beyond CMOS

Year 2006

More Moore: Miniaturization

Non-digital content System-in-package (SiP)

Combining SoC and SiP: Heterogeneous Integration

Information Processing
- Digital content System-on-chip (SoC)

Interacting with people and environment

EUVL Symposium
On January 9, 2007 Steve Jobs announced the iPhone at the Macworld convention, receiving substantial media attention,[16] and that it would be released later that year. On June 29, 2007 the first iPhone was released.
A WiFi-only model of the tablet was released in April 2010, and a WiFi+3G model was introduced about a month later.

EUVL Symposium
Increasing Degree of Integration

Degree of Integration

2007 2008 2009 2010 2011 2012 2013

- LPDDR3
- ARMv8 ISA
- LTE
- Integrated wireless
- Integrated BT
- 1080p Video
- W-CDMA
- ARMv7 ISA
- GHz Application processor
- LPDDR2
- GPU
- ARMv6 ISA

Qualcomm Snapdragon™ Family
Number of ICs in a Smart Phone

Increase: Demand for more functions

Decrease: Highly integrated AP

#IC in a smartphone

Inside the Apple A7 from the iPhone 5s
(Courtesy of Chipworks)

1 billion transistors on a die 102 mm²
Trends in Number of ICs, Antennas and Sensors
Figure MEMS  Sensors trends for handsets, presented by Len Sheynblat, Vice President of Technology, Qualcomm CDMS Technologies, at MIG’s M2M 2012 Workshop, Pittsburg PA.
Heterogeneous Systems

Year 2014

Heterogeneous Components — describes devices that do not necessarily scale according to “Moore's Law,” and provide additional functionalities, such as power generation and management, or sensing and actuating.

Source: Georgia Tech PRC, http://www.prc.gatech.edu/overview/images/etpc.jpg
Yesterday

200 Million Processors for PCs

Today

300 Million Processors for PCs

300 Million Processors for Tablets

1 Billion+ Processors for phones
Tracking Semiconductor Unit Growth

Source: IC Insights
2014 ITRS Overview
ITRS 2.0
Paolo Gargini
Chairman ITRS
Fellow IEEE
I-Fellow JSAP

October 13-15, 2014
Korea
In the 80s and 90s the Semiconductor Industry was constituted by Integrated Device Manufactures (IDM)

- Standard components (e.g. Memory and Microprocessors) were produced by IDM and assembled into systems by OEMs

In the past 10 years the Semiconductor Industry has evolved into a distributed industry

- Design team and manufacturing teams are no longer in a single company
- Custom SoC and SIP are the dominant building blocks of electronic systems
- Design houses and foundries represent the new foundation of the Semiconductor Industry

The 2014/15 ITRS has been restructured to represent the new ecosystem
Beyond 2020

Customized Functionality
Outside System Connectivity
System Integration
Heterogeneous Integration
More than Moore
More Moore
Beyond Moore

ITRS 2012

EUVL Symposium
Beyond 2020

Themes
- System Integration
- Outside System Connectivity
- Heterogeneous Integration
- More than Moore
- Beyond Moore
- More Moore
- Manufacturing

ITWGs
- System Integration
- Outside System Connectivity
- Heterogeneous Integration
- Heterogeneous Components
- Beyond CMOS
- More Moore
- Manufacturing
**Definitions of 7 Focus Topics**

**System Integration**—studies and recommends system architectures to meet the needs of the industry. It prescribes ways of assembling heterogeneous building blocks into coherent systems.

**Outside System Connectivity**—refers to physical and wireless technologies that connect different parts of systems.

**Heterogeneous Integration**—refers to the integration of separately manufactured technologies that in the aggregate provide enhanced functionality.

**Heterogeneous Components**—describes devices that do not necessarily scale according to “Moore's Law,” and provide additional functionalities, such as power generation and management, or sensing and actuating.

**Beyond CMOS**—describes devices, focused on new physical states, which provide functional scaling substantially beyond CMOS, such as spin-based devices, ferromagnetic logic, and atomic switch.

**More Moore**—refers to the continued shrinking of horizontal and vertical physical feature sizes to reduce cost and improve performance.

**Factory Integration** consists of tools and processes necessary to produce items at affordable cost in high volume.
Assessment of Driving Forces

Internet of Things
Data Input, Access & Processing Environment

Applications
- Mobile Comm. & Information
- Smart Automotive
- Big Data
- Green/Energy Technology
- Medical/Health

More than Moore
- Heterogeneous Integration
- Heterogeneous Components

Systems Integration

More Moore

Beyond Moore

Outside System Connectivity

Global Responsibility

Focus Responsibility

Factory Integration (Manufacturing)

System Output
Inputs to FI

P. Gargini
# Smart Phone Metrics

## TABLE V: Summary of scaling trends of smartphones.

<table>
<thead>
<tr>
<th>Input Metrics</th>
<th>Metrics</th>
<th>Metric Evolution</th>
</tr>
</thead>
<tbody>
<tr>
<td>#AP cores</td>
<td>1.0 × 1.14 (^{(\text{Year}−2007)})</td>
<td></td>
</tr>
<tr>
<td>#GPU cores</td>
<td>2.0 × 1.26 (^{(\text{Year}−2007)})</td>
<td></td>
</tr>
<tr>
<td>Max frequency (GHz)</td>
<td>2.3 × 1.04 (^{(\text{Year}−2011)})</td>
<td></td>
</tr>
<tr>
<td>#MPixels of display</td>
<td>0.7 × 1.27 (^{(\text{Year}−2013)})</td>
<td></td>
</tr>
<tr>
<td>Memory BW (Gb/s)</td>
<td>16000 × 1.19 (^{(\text{Year}−2011)})</td>
<td></td>
</tr>
<tr>
<td>#Sensors</td>
<td>7 + (\text{Year} − 2009) × 0.85</td>
<td></td>
</tr>
<tr>
<td>#Antennas</td>
<td>7 + (\text{Year} − 2009) × 0.4</td>
<td></td>
</tr>
<tr>
<td>#ICs</td>
<td>10 − (\text{Year} − 2009) × 0.15</td>
<td></td>
</tr>
<tr>
<td>Cellular data rate (MB/s)</td>
<td>5.25MB/s until 2022, 21.6MB/s afterwards</td>
<td></td>
</tr>
<tr>
<td>WiFi data rate (Mb/s)</td>
<td>75Mb/s until 2015, 850Mb/s afterwards</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Output metrics</th>
<th>Board area ((cm^2))</th>
<th>See Figure 6</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>System power ((mW))</td>
<td>See Figure 6</td>
</tr>
</tbody>
</table>
Abstract Block Diagrams of Products

Evolution trends for microservers:
1. Highly integrated accelerators
2. Extreme low-power cores
3. Optical interconnects

Projection beyond 2013 (Alt-1)

Projection beyond 2013 (Alt-2)
### TABLE VII: Summary of scaling trends of microservers.

<table>
<thead>
<tr>
<th>Metrics</th>
<th>Metric Evolution</th>
</tr>
</thead>
<tbody>
<tr>
<td>#MPU cores per rack unit</td>
<td>16 × 1.19&lt;sup&gt;Year=2013&lt;/sup&gt;; Year ≤ 2019</td>
</tr>
<tr>
<td></td>
<td>45 × 1.12&lt;sup&gt;Year=2019&lt;/sup&gt;; Year ≥ 2019</td>
</tr>
<tr>
<td>Max frequency (&lt;i&gt;GHz&lt;/i&gt;)</td>
<td>3.46 × 1.04&lt;sup&gt;Year=2013&lt;/sup&gt;</td>
</tr>
<tr>
<td>DRAM capacity (&lt;i&gt;GB&lt;/i&gt;) per rack unit</td>
<td>128 × 1.58&lt;sup&gt;Year=2013&lt;/sup&gt;</td>
</tr>
<tr>
<td>DRAM BW (&lt;i&gt;GB/s&lt;/i&gt;)</td>
<td>51.2 × 1.26&lt;sup&gt;Year=2013&lt;/sup&gt;</td>
</tr>
<tr>
<td>Off-MPU BW (&lt;i&gt;GB/s&lt;/i&gt;)</td>
<td>64 × 1.28&lt;sup&gt;Year=2013&lt;/sup&gt;; Year ≤ 2019</td>
</tr>
<tr>
<td></td>
<td>285 × 1.18&lt;sup&gt;Year=2019&lt;/sup&gt;; Year ≥ 2019</td>
</tr>
<tr>
<td>MPU frequency × #Cores (&lt;i&gt;GHz&lt;/i&gt;) per rack unit</td>
<td>55 × 1.24&lt;sup&gt;Year=2013&lt;/sup&gt;; Year ≤ 2019</td>
</tr>
<tr>
<td></td>
<td>45 × 1.16&lt;sup&gt;Year=2019&lt;/sup&gt;; Year ≥ 2019</td>
</tr>
</tbody>
</table>
Technology Node Scaling

Today’s Challenge

2013 ITRS
EUVL Symposium

From My Files
The Different Ages of Scaling

① Geometrical Scaling
① Reduction of horizontal and vertical physical dimensions in conjunction with improved performance of planar transistors

② Equivalent Scaling
① Reduction of only horizontal dimensions in conjunction with introduction of new materials and new physical effects. New vertical structures replace the planar transistor

③ 3D Power Scaling
① Transition to complete vertical device structures. Heterogeneous integration in conjunction with reduced power consumption become the technology drivers
Summary

1. Reduction of blank defects resumed after equipment upgrades
2. Good correlation between mask defects and printed defects
3. Pellicle multi-step engagement plan formulated, is this enough?
4. Good progress in mask infrastructure
5. No much progress in resist except for the hope of non-CAR resists
6. Good progress in outgassing round robin
7. 500 wafers/day demonstrated, 80W source power demonstrated but is this progress fast enough?
8. Half-pitch of 32-26nm reported
9. Industry volume continues to go up propelled by phones, tablets and PCs
10. Device roadmap very healthy
11. ITRS 2.0 addressing system integration, heterogeneous integration, outside connectivity as new recognized industry drivers