



Role of mask in cost and capability dynamics for sub 14nm patterning

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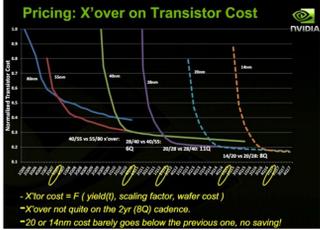
Abstract

Regardless of the direction in future patterning technology at 10nm and beyond, a mask based patterning process will surely help enable the technology roadmap and also play a pivotal role in design cost and cycle time optimization. State of the art wafer patterning utilizes a complex assembly of 193nm based multi-patterning mask layers, resolution enhancement techniques such as mask phase shifting and a careful co-optimization of tools, software, mask and materials to deliver the total patterning solution. Whether this existing approach is extended through 7nm and beyond or gradually replaced with an alternative such as EUV lithography, we will have many opportunities and challenges to tune the performance, cost and delivery speed of advanced patterning processes.

We will discuss the interplay between mask cost, substrate size, mask layer count and patterning approach for various sub 14nm patterning scenarios. How these factors might impact device cost, design starts and cycle time through access to advanced mask making processes and equipment will be presented as well.

Introduction

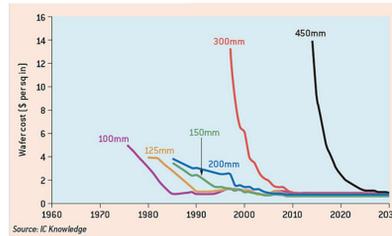
- Since the 28nm node, the industry has been able to double the amount of transistors in a single device, but not at lower cost.



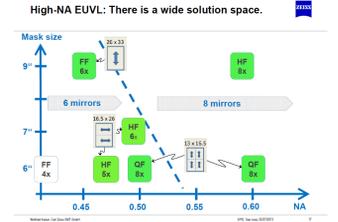
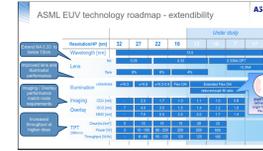
- Escalating wafer costs takes away the higher transistor density gains



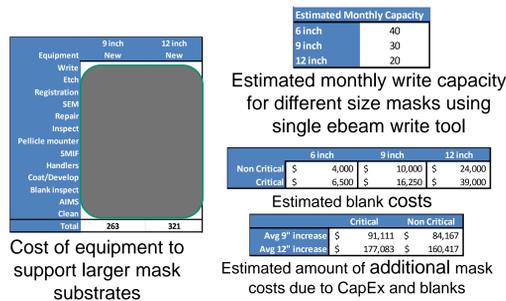
- Larger wafer diameters have historically helped control costs, this philosophy be applied to masks to improve ArF productivity



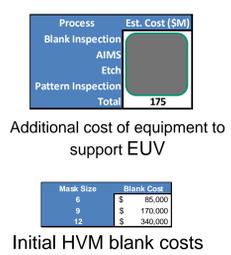
- Can these investments be leveraged for high NA EUV options?
 - Scanner roadmap predicts end of 0.33 NA single patterning at 13 nm feature size. For smaller features EUV double patterning or high NA EUV is required



Cost Model Assumptions



EUV Assumptions



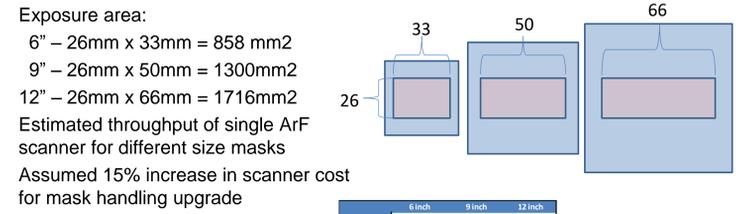
Mask Cost Assumptions

Mask Size	Critical			Non-Critical		
	N10	N7	N5	N10	N7	N5
6	\$ 150,000	\$ 165,000	\$ 181,500	\$ 60,000	\$ 66,000	\$ 72,600
9	\$ 241,111	\$ 265,222	\$ 291,744	\$ 144,167	\$ 158,583	\$ 174,442
12	\$ 327,083	\$ 359,792	\$ 395,721	\$ 220,417	\$ 245,458	\$ 266,734

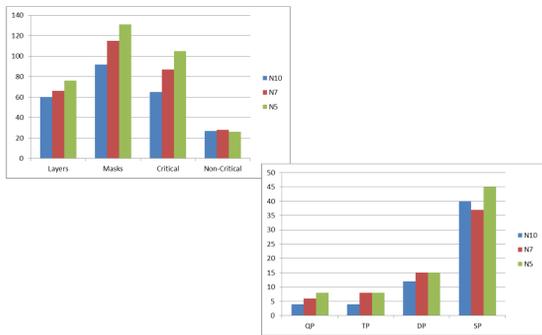
Node	Monthly Volume		
	N10	N7	N5
6	5	10	15
9	10	20	30
12	15	30	45

Mask volume per month based on set requirements

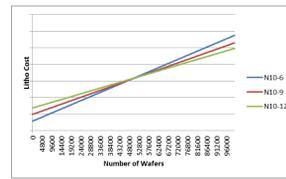
Mask Area Assumptions



Set Composition - Optical only

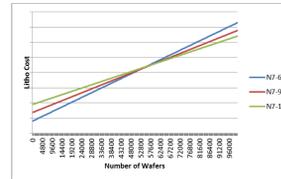


N10 ArF Litho Cost



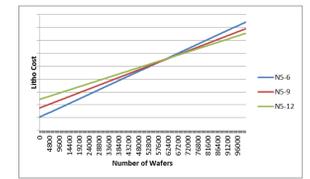
- Crossover for cost benefit is ~50k wafers
- 8% litho cost improvement for 9 inch and 14% for 12 inch @ 100k wafers

N7 Arf Litho Cost



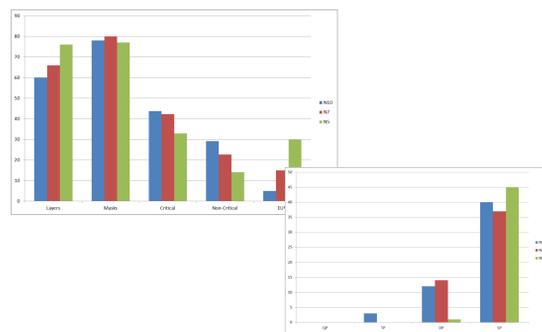
- Crossover for cost benefit is ~55k wafers
- 7% litho cost improvement for 9 inch and 12% for 12 inch @ 100k wafers

N5 ArF Litho Cost

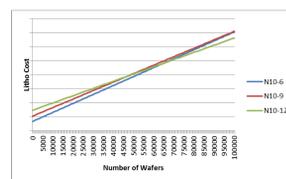


- Crossover for cost benefit is ~60k wafers
- 6% litho cost improvement for 9 inch and 10% for 12 inch @ 100k wafers

Set Composition - with EUV

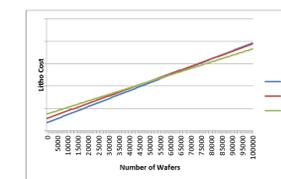


N10 Litho Cost with EUV



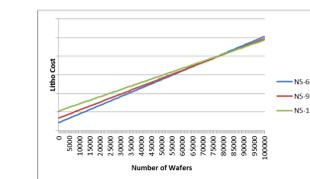
- Crossover for cost benefit is ~65k wafers
- 1% cost improvement for 9 inch and 8% for 12 inch @ 100k wafers

N7 Litho Cost with EUV



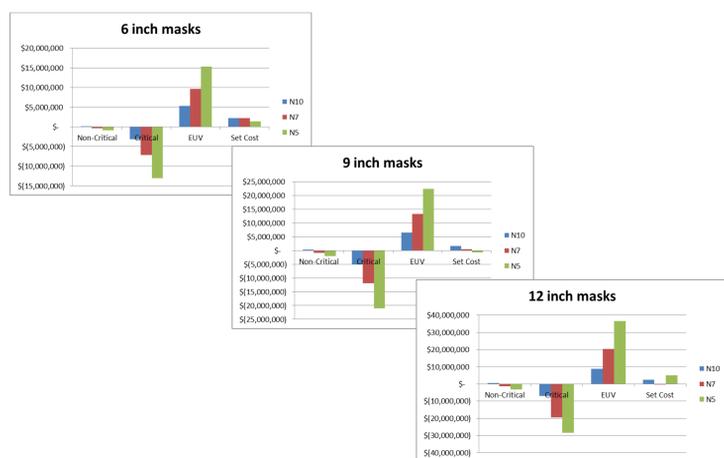
- Crossover for cost benefit is ~50k wafers
- 1% cost improvement for 9 inch and 7% for 12 inch @ 100k wafers

N5 Litho Cost with EUV



- Crossover for cost benefit is ~60k wafers
- 2% cost improvement for 9 inch and 4% for 12 inch @ 100k wafers

Mask Set Cost Difference - ArF only to EUV



Summary

- Larger substrates offer larger field size that allow more chips/field and fewer fields/wafer increasing scanner productivity
- Modest ArF wafer volumes are required to reach cost parity with 6 inch substrate
- Projected increase in productivity of ArF scanners can help reverse rising Litho cost trend
- Business model for large EUV substrates only makes sense if adopted with other wavelengths
 - Initial high EUV mask cost is not an impediment from being competitive with ArF
 - Improves multi-patterning strategy by allowing for more single or worst case double patterning
 - Scanner throughput will dictate product adoption
 - Early benefactors will be high volume runners
 - Earlier adoption (at any substrate size) will help drive crossover from ArF multi-patterning
- Modest Litho Cost improvement can be realized with EUV
 - Blank cost is key mask affordability driver, requires industry support
 - Increased volumes will reduce CapEx depreciation per mask
 - Continuous improvement of source power will only offer more long term gains

Cost Parity Crossover (k wafers)

Node	6 inch	9 inch	12 inch
N10	45	50	55
N7	50	55	60
N5	55	60	65

Cost Improvement @ 100k wafers

Node	6 inch	9 inch	12 inch
N10	0%	1%	8%
N7	0%	7%	12%
N5	0%	6%	10%

Cost Parity Crossover (k wafers)

Node	6 inch	9 inch	12 inch
N10	50	65	80
N7	75	90	105
N5	60	75	90

Cost Improvement @ 100k wafers

Node	6 inch	9 inch	12 inch
N10	0%	1%	8%
N7	0%	7%	12%
N5	0%	2%	4%