2014 International Symposium on EUVL

EUVL Convergence with Multi-Patterning Technologies

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Corporate Vice President and Deputy General Manager

Tokyo Electron Limited
Outline

Innovation and Inflection Points
Market factors, technical backdrop
How much trouble are we in???

N7 Patterning Trade-offs and Scenarios
EUV hybrid vs. iArF only options
Cost, Performance, Flexibility

Collaborative N7 Patterning R&D
Non-lithographic techniques to assist patterning
EUV assisted DSA

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Summary
The Innovation Cycle & Inflection Points

Innovation Index

Original Invention

Time to Innovate

Time

Why is this relevant to the talk?
Economic Drivers Fuelled by Technology Innovation

- **1970~ General-purpose Computer**
  - 1 unit per Company
  - 10^6 unit/Year

- **1980~ Workstation**
  - 1 unit per Office
  - 10^8 unit/Year

- **1990~ Personal Computer**
  - 1 unit per Employee
  - 10^9 unit/Year

- **2000~ Mobile Phone**
  - 1 unit per Person
  - 10^10 unit/Year

- **2010~ Ubiquitous**
  - Multiple units per Person

**Global Network**
- The Era of Sharing
- SNS
- Internet of Things
- Big Data
- Wearable device

**Business Use**
- 1 unit per Company
- 10^6 unit/Year

**Internet**
- 1 unit per Employee
- 10^8 unit/Year
- 1 unit per Person
- 10^9 unit/Year

**Personal Use**
- Multiple units per Person
- 10^10 unit/Year

**Networked Society**
- 1 unit per Person
- 1 unit per Office

Anyone, Anytime, Anywhere → Internet of Everything
Technology Roadmap: Innovation

Technology inflection points are interlinked, interdependent

Source: TEL based on ITRS
Historical Inflection Points

90nm (Planar Poly Gate)
- SiGe
- PMOS
- NMOS
- T. Ghani, et al., IEDM 2003

45nm (Planar RMG)
- PMOS
- K. Mistry, et al., IEDM 2003

22nm (FinFET RMG)
- C. Auth, et al., VLSI tech. 2012

Introduction of cut mask and local interconnect

Introduction of SADP and pitch split (LELE)

16x density over 5 generations of structure & material evolution
Inflection in Patterning (2D → 1D)

90nm (Planar Poly Gate)

T. Ghani, et al., IEDM 2003

45nm (Planar RMG)

K. Mistry, et al., IEDM 2003

22nm (FinFET RMG)

C. Auth et al., VLSI tech. 2012

Progressive use of 1D style, cut mask and pitch split…
Extendibility of SADP

SADP is extendible to 4x and 8x multiplication but there are many process steps needed.
# 193i Patterning Process Assumptions: Masks

## FEOL

<table>
<thead>
<tr>
<th>Level</th>
<th>32nm</th>
<th>10nm</th>
<th>7nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Active</td>
<td>193i</td>
<td>SADP + SE CUT</td>
<td>1 + 1 SAQP + LE2 CUT</td>
</tr>
<tr>
<td>Gate</td>
<td>193i + SE CUT</td>
<td>SADP + SE CUT</td>
<td>1 + 1 SADP + SE CUT</td>
</tr>
<tr>
<td>MOL</td>
<td>193i + 193i</td>
<td>LE2 + LE2</td>
<td>4 LE2 + LE3</td>
</tr>
</tbody>
</table>

## M1

<table>
<thead>
<tr>
<th>Level</th>
<th>32nm</th>
<th>10nm</th>
<th>7nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>V0</td>
<td>193i</td>
<td>LE2</td>
<td>2 LE3</td>
</tr>
<tr>
<td>M1</td>
<td>193i</td>
<td>LE3</td>
<td>3 SADP + LE3 Block</td>
</tr>
</tbody>
</table>

## V1

<table>
<thead>
<tr>
<th>Level</th>
<th>32nm</th>
<th>10nm</th>
<th>7nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>V1</td>
<td>193i</td>
<td>LE2</td>
<td>2 LE4</td>
</tr>
<tr>
<td>M2</td>
<td>193i</td>
<td>SADP + SE Block</td>
<td>1 + 1 SAQP + LE3 Block</td>
</tr>
</tbody>
</table>

| Mask Count | 9 Mask Count | 17 Mask Count | 25 Mask Count |

Source: Julien Ryckaert, imec

Mask count increases rapidly...and drives the cost
Scaling Cost Challenges

Fabless community openly discusses cost concerns...
Future of Fabrication (2D $\rightarrow$ 3D)

- **FinFET**
  - High-k + Metal Dep

- **Nano Wire FET**
  - High-k + Metal Dep
  - Oxide Removal
  - Oxidation for Rounding

- **Dummy Gate Removal**
  - Si (or SiGe) Removal
Sunrise or Sunset?
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   Market factors, technical backdrop
   How much trouble are we in???

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   EUV hybrid vs. iArF only options
   Cost, Performance, Flexibility

Collaborative N7 Patterning R&D
   Non-lithographic techniques to assist patterning
   EUV assisted DSA

Summary
Patterning “CFP” Tradeoff Triangle

\[ E_{PE} = \frac{RSS(OL, \Delta CD, LER)}{2} < \frac{Pitch}{4} \]

Performance - EPE

Design - Flexibility

Design - Flexibility

SAQP – ‘GRID’

SAQP – ‘KEEP’

SAQP – BLOCK/CUT

VIA Decomposition
### Process Assumptions for N7 (EUV intro)

<table>
<thead>
<tr>
<th>Layer</th>
<th>Pitch [nm]</th>
<th>193i patterning</th>
<th>EUV hybrid</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>FEOL</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Fin</td>
<td>21-24</td>
<td>SAQP + LE2 CUT</td>
<td>SAQP + EUV SE CUT</td>
</tr>
<tr>
<td>Gate</td>
<td>40-45</td>
<td>SADP + SE CUT</td>
<td>SADP + EUV SE CUT</td>
</tr>
<tr>
<td>MOL</td>
<td>40-45</td>
<td>LE2 + LE3</td>
<td>EUV SE + SE</td>
</tr>
<tr>
<td><strong>M1</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V0</td>
<td>40-45</td>
<td>LE3</td>
<td>EUV SE</td>
</tr>
<tr>
<td>M1</td>
<td>40-45</td>
<td>SADP + LE3 BLOCK</td>
<td>EUV SE</td>
</tr>
<tr>
<td><strong>Mx</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V1</td>
<td>45-51</td>
<td>LE4</td>
<td>EUV SE</td>
</tr>
<tr>
<td>M2</td>
<td>28-36</td>
<td>SAQP + LE3 BLOCK</td>
<td>SAQP + EUV SE BLOCK</td>
</tr>
</tbody>
</table>

**Mask count**

25 (193i) | 11 (3 + 8 EUV)

**EUV offers path to manage mask count**

Source: Julien Ryckaert, imec
Process Assumptions for N7 (FEOL)

<table>
<thead>
<tr>
<th>Layer</th>
<th>Pitch [nm]</th>
<th>193i patterning</th>
<th>EUV hybrid</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fin</td>
<td>21-24</td>
<td>SAQP + LE2 CUT</td>
<td>SAQP + EUV SE CUT</td>
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</tr>
<tr>
<td>MOL</td>
<td>40-45</td>
<td>LE2 + LE3</td>
<td>EUV SE + SE</td>
</tr>
</tbody>
</table>

EUV cut mask improves process margin

Source: Julien Ryckaert, imec
## Process Assumptions for N7 (M1)

<table>
<thead>
<tr>
<th>Layer</th>
<th>Pitch [nm]</th>
<th>193i patterning</th>
<th>EUV hybrid</th>
</tr>
</thead>
<tbody>
<tr>
<td>V0</td>
<td>48-58</td>
<td>LE3</td>
<td>EUV SE</td>
</tr>
<tr>
<td>M1</td>
<td>40-45</td>
<td>SADP + LE3 BLOCK</td>
<td>EUV SE</td>
</tr>
</tbody>
</table>

**Unidirectional M1**
- Spacer defined patterning
- Complex Block Patterns
- Complex MOL Scheme
- Limited by Min area and T2T

**Restricted-2D M1**
- L/S Design Flexibility (1.5D)
- Simplified MOL scheme
- Pitch Scaling Limited
- LER Increase vs. Spacer

Source: Julien Ryckaert, imec
EUV Benefits in N7 Mask Decomposition

\[ EPE_{\text{via-to-metal}} = f(CDU_{\text{via}}, LCDU_{\text{via}}, OL_1, OL_2, OL_3, OL_4, CDU_{\text{grid}}, LER_{\text{grid}}) \] ArFi

\[ EPE_{\text{via-to-metal}} = f(CDU_{\text{via}}, LCDU_{\text{via}}, OL_1, CDU_{\text{grid}}, LER_{\text{grid}}) \] EUV

Fewer masks reduce OL contribution to EPE
### EUV for Mx N7 Patterning

<table>
<thead>
<tr>
<th>Layer</th>
<th>Pitch [nm]</th>
<th>193i patterning</th>
<th>EUV hybrid</th>
</tr>
</thead>
<tbody>
<tr>
<td>V1</td>
<td>45-51</td>
<td>LE3 or LE4</td>
<td>EUV SE</td>
</tr>
<tr>
<td>M2</td>
<td>28-36</td>
<td>SAQP + LE3 BLOCK</td>
<td>SAQP + EUV SE</td>
</tr>
</tbody>
</table>

Block mask (193i) → 3 colors required

V1 grid (193i) → 3 or 4 colors required

32nm pitch means 90nm C2C

Diamond configuration requires 4 colors

Reduced BEOL mask complexity

Source: Julien Ryckaert, imec
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Summary
EUV Collaboration Ecosystem

- Mask suppliers
- Chemical suppliers
- Filter suppliers
- Measurement tool suppliers
- Inspection tool suppliers

16nm L/S@NXE:3300

with FIRM™ AZ Extreme™

AZ Extreme is a Trade mark of AZ Electronic Materials, a subsidiary of Merck KGaA, Darmstadt, Germany.
Patterning Equipment Set

Extensive collaboration amongst different processes
## Pattern Collapse Mitigation at 22nm HP

### Process Condition
- **Exposure tool:** NXE3100
- **Resist:** ESR1
- **Process:** 2.38% TMAH → DIW rinse → Surfactant rinse

<table>
<thead>
<tr>
<th></th>
<th>DIW (ref.)</th>
<th>AZ Extreme™ 10</th>
<th>AZ Extreme™ A</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Process Window Count</strong></td>
<td>18</td>
<td>21</td>
<td>21</td>
</tr>
<tr>
<td><strong>Resolution limit (nm)</strong></td>
<td>22</td>
<td>20</td>
<td>19</td>
</tr>
<tr>
<td><strong>Sensitivity at 22nm (mJ/cm²)</strong></td>
<td>13.9</td>
<td>14.3</td>
<td>13.9</td>
</tr>
<tr>
<td><strong>LWR at 22nm (nm)</strong></td>
<td>6.4</td>
<td>6.2</td>
<td>5.7</td>
</tr>
<tr>
<td><strong>Pattern size 22nm Half pitch (Top-Down SEM image)</strong></td>
<td><img src="image1.png" alt="DIW" /></td>
<td><img src="image2.png" alt="AZ Extreme™ 10" /></td>
<td><img src="image3.png" alt="AZ Extreme™ A" /></td>
</tr>
</tbody>
</table>

*Courtesy of EIDEC*

**lithography improvement using a Wet Clean process using surfactant rinse AZ Extreme™ A**
Contact Hole CDU/CER Improvement

Green: Improved
Red: Degraded

Inspection: CG4100
Samples: FEM from Albany MET
Factor: Track parameters
Response: CD, LCDU, CER

Increasing resist thickness and adding FIRM™ surfactant rinse improves post litho LCDU / CER
TEL Smoothing vapor phase process can improve LWR and CER
CD, CDU, CER Improvement using Etch

Post litho* ->

CD: 33.75nm
LCDU: 5.02nm
CER: 3.72nm

OPL open ->

CD: 23.99nm
LCDU: 2.15nm
CER: 1.93nm

Ox/SiN HM open

CD: 23.99nm
LCDU: 1.91nm
CER: 1.76nm

*work at Albany, etched on Tactras™

Etch shrink and transfer process improves LCDU and CER
PR Hardening with Etch DCS

DCS Technology

Pre Processing | H2 Cure w/o DCS | H2 Cure with DCS
---|---|---
EUV resist | 43.3nm | 56.5nm
Si-Substrate | Thickness of resist = 68.7nm

H2 Cure with DCS

Reformed Layer = 41.6nm

Pre Processing | Si-ARC Etch | H2 Cure | Mask Break
---|---|---|---
PR Height 51.1nm | 12.3nm | None (-13.7nm) | 15.0nm
LWR 4.8nm | LWR 4.4nm | LWR 3.8nm | LWR 3.2nm

DCS improves LER and resist durability during Etch process
32nm L/S Defect reduction with filters

**Defect Modes**
- Underlayer
- Collapse
- Embedded
- Large Bridging
- Micro Bridge
- Missing Pattern
- Protrusion

- Micro Bridge Defect reduction is the Key Challenge

**Reducing Defects**

- Target Defect Density (defects/cm²)
  - 0.70
  - 0.18
  - 0.12
  - 0.09

- 25% Reduction

**New resist filtering system lowers defects**

Yuhei Kuwahara/TEL – Philippe Foubert /imec et. al, SPIE 2014
30nm CH Defect reduction through rinse

Defect Modes
- Underlayer/SI
- Embedded
- Residue
- Partially closed hole
- Large irregular bridging

Reducing Defects
- Underlayer/SI
- Embedded
- Residue

Residue Defect reduction is the key Challenge

Defect Density (defects/cm²)
- April 2013 Resist E: 2.24
- EUVL 2013 Resist E: 1.37
- SPIE 2014 Resist E: 0.86

New rinse technique reduces defects

37% Reduction

Yuhei Kuwahara/TEL – Philippe Foubert /imec et. al, SPIE 2014
High Speed EUV

**Reference Case**
(single print EUV)

- PR
- Si-Arc
- OPL
- SiN
- Poly

- EUV 50wph

**This Project**
(mix & match / EUV & 193i SADP)

- PR
- SiN
- Poly

- EUV 150wph

- ALD

- 193i

- Combined Etch

- Spacer Etch

- Remove mandrel
- Spacer on inorganic substrate

- Final Etch

- Pattern

<table>
<thead>
<tr>
<th>Pattern</th>
<th>Reference Case</th>
<th>SADP Case</th>
</tr>
</thead>
<tbody>
<tr>
<td>Initial Resolution (at EUV)</td>
<td>16nm</td>
<td>32nm</td>
</tr>
<tr>
<td>Initial LWR</td>
<td>2.7nm</td>
<td>4.7nm</td>
</tr>
<tr>
<td>Resist Thickness</td>
<td>40nm</td>
<td>70nm</td>
</tr>
<tr>
<td>Exposure Dose</td>
<td>35mj/cm²</td>
<td>7mj/cm²</td>
</tr>
<tr>
<td>Final Resolution</td>
<td>16nm</td>
<td>16nm</td>
</tr>
</tbody>
</table>

New sequence reduces LER and improves CoO

Anton deVilliers/TEL Technology Center, America – Jerome Wandell/GLOBALFOUNDRIES et. al, SPIE 2014
Progress of HSEUV Process Optimization

<table>
<thead>
<tr>
<th>Process Stage</th>
<th>Top down images</th>
<th>Sensitivity / LER</th>
<th>Estimated thru-put</th>
</tr>
</thead>
<tbody>
<tr>
<td>HSEUV (15nm HP)</td>
<td><img src="image1" alt="Top down image" /></td>
<td>10.0 [mJ/cm²] / 5.4nm</td>
<td>93 wph (at 85W Source Power)</td>
</tr>
<tr>
<td>Reference (16nm HP)</td>
<td><img src="image2" alt="Top down image" /></td>
<td>53.0 [mJ/cm²] / 4.8nm</td>
<td>30 wph</td>
</tr>
</tbody>
</table>

Demonstrated higher throughput at same resolution; optimizing LER required
EUV and Directed Self-Assembly

<table>
<thead>
<tr>
<th></th>
<th>EUV Lithography</th>
<th>EUV + DSA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dose</td>
<td>105 mJ/cm²</td>
<td>32.1 mJ/cm²</td>
</tr>
<tr>
<td>LCDU</td>
<td>4.6nm</td>
<td>4.9nm</td>
</tr>
<tr>
<td>20nm Hole</td>
<td></td>
<td></td>
</tr>
<tr>
<td>60nm Pitch</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

K. Maruyama et al. EUVS 2012

H. –S. P. Wong et al. EIPBN 2012

Present

Torres et al. SPIE 2014

Can EUV provide relief for guiding pattern challenge?
DSA – Technology at an Inflection Point

- Normalized Defect Density [#/cm²]

- Continuously improving defectivity

- Missing Hole DSA Failure 27%
- DSA Failure 9%
- Others 64%

- DSA Specific Defects
  - DSA Failure
  - Missing Hole

- Other Defects
  - Large Material
  - Small Material
  - Embedded
  - Others
Summary

Key challenges for N7 patterning are reducing cost, improving EPE and increasing design flexibility.

Convergence of EUV and MP technologies could offer the EPE and flexibility advantages of each approach with reduced cost.

IDM/fabless design community collaboration essential to help make choices between patterning tradeoffs.
Upcoming EUVL Progress Reports

International Symposium on EUVL

Impact of Novel Defect Reduction Hardware on EUV Patterning Defectivity – Yuhei Kuwahara, TEL

Novel Processing Approaches to Enable EUV Lithography toward High Volume Manufacturing – Cecilia Montgomery, SEMATECH, TEL, et al.
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