Current status of EUV patterned mask inspection tool for hp 16 nm and beyond

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OUTLINE

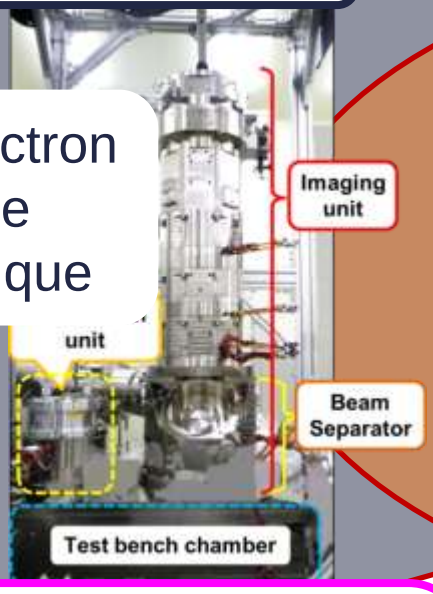
1. Introduction
2. Patterned mask Inspection (PI) tool development
3. Image processing to capture 16 nm sized defects
   - Defect detection capability
   - Capture rate estimation -Model and method-
   - Capture rate comparison -Higher throughput with larger pixel-
4. Summary and Future works

1. Introduction

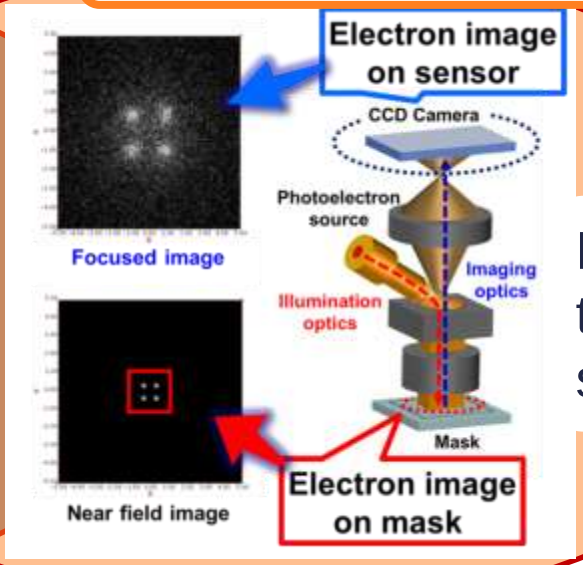
EIDEC investigates the technology of the patterned mask quality assurance for EUVL mask

PI tool development

Projection Electron Microscope (PEM) technique



Electron image analysis



Electron trajectory simulator

See poster P-MA-22: "Development of new Inspection System with Novel PEM and its Basic Performance Evaluation for EUV Mask", M. Hatakeyama, et al.

See poster P-MA-21: "Impact of incident electron energy on patterned EUV mask inspection", S. Iida et al.

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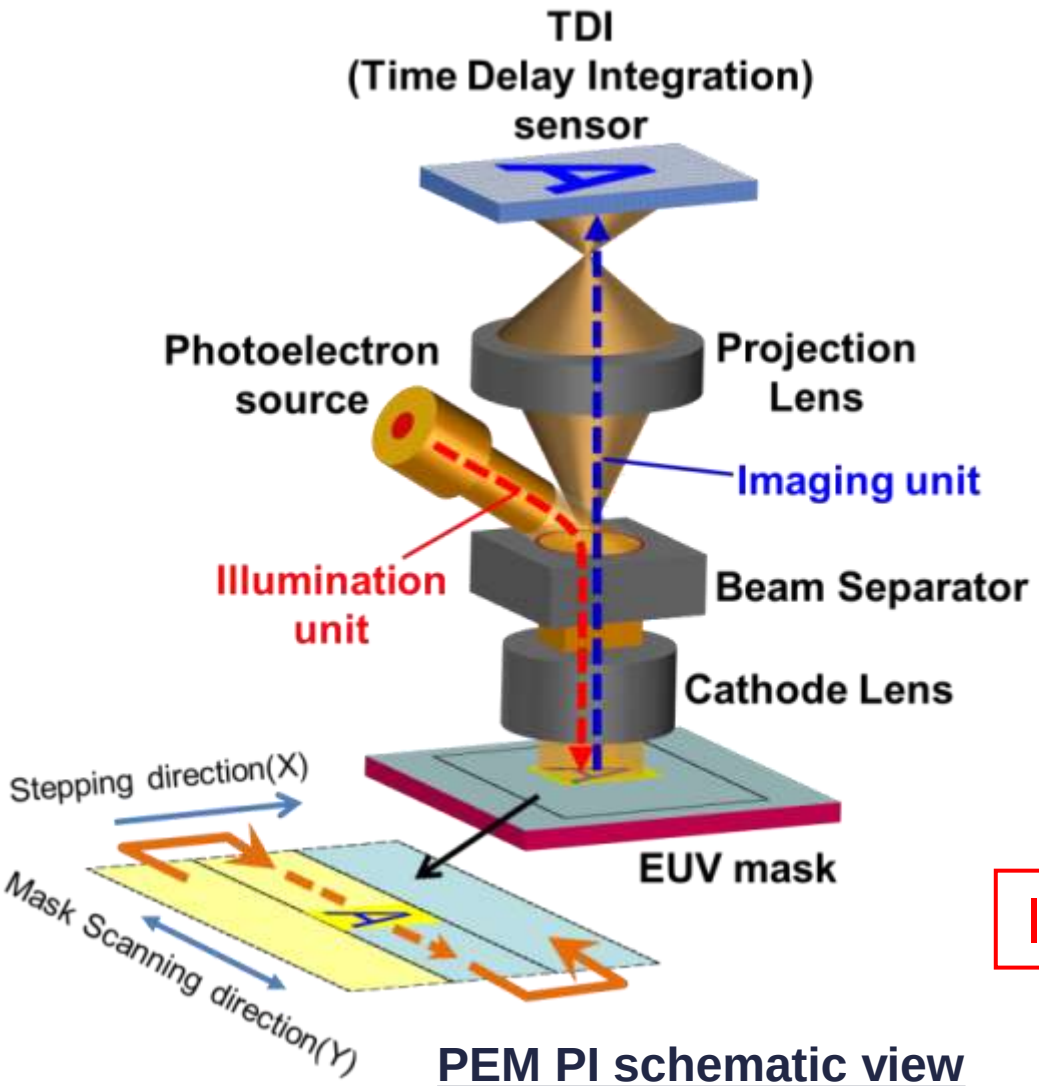
2. Patterned mask Inspection (PI) tool development

- Electron optics evaluation and tool integration have been completed
- Clear images were acquired by the integrated optics on test bench with a sample mask

Development of defect detection performance for 16 nm HVM and study on hp 11 nm PI technology are currently in progress

PEM's advantage for PI



PEM PI schematic view

PEM probes sample mask with areal illumination

free from probing electron current density limitation

Improve the inspection throughput

Hirano et.al., SPIE vol.8701

Improvements of PEM optics performance

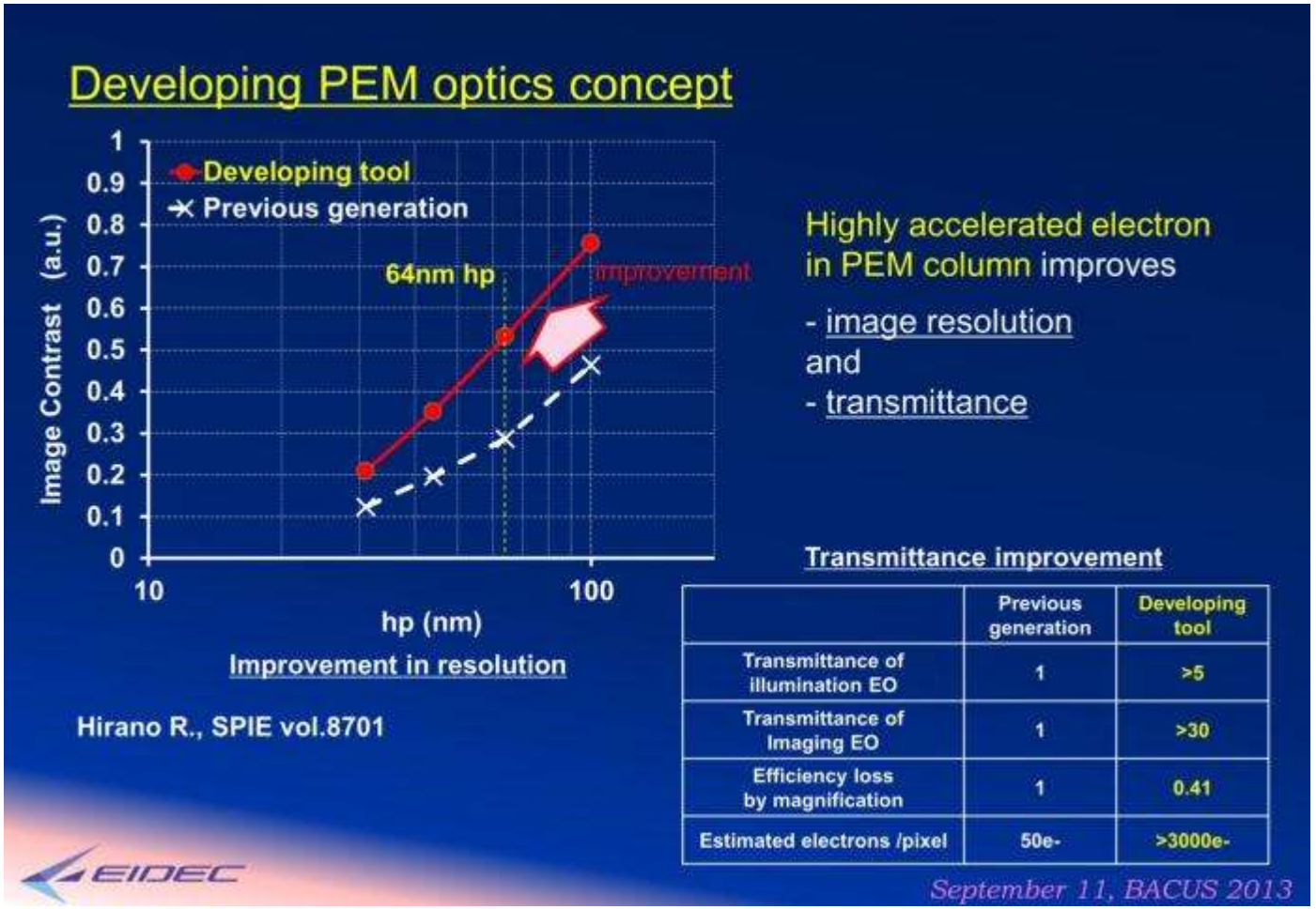


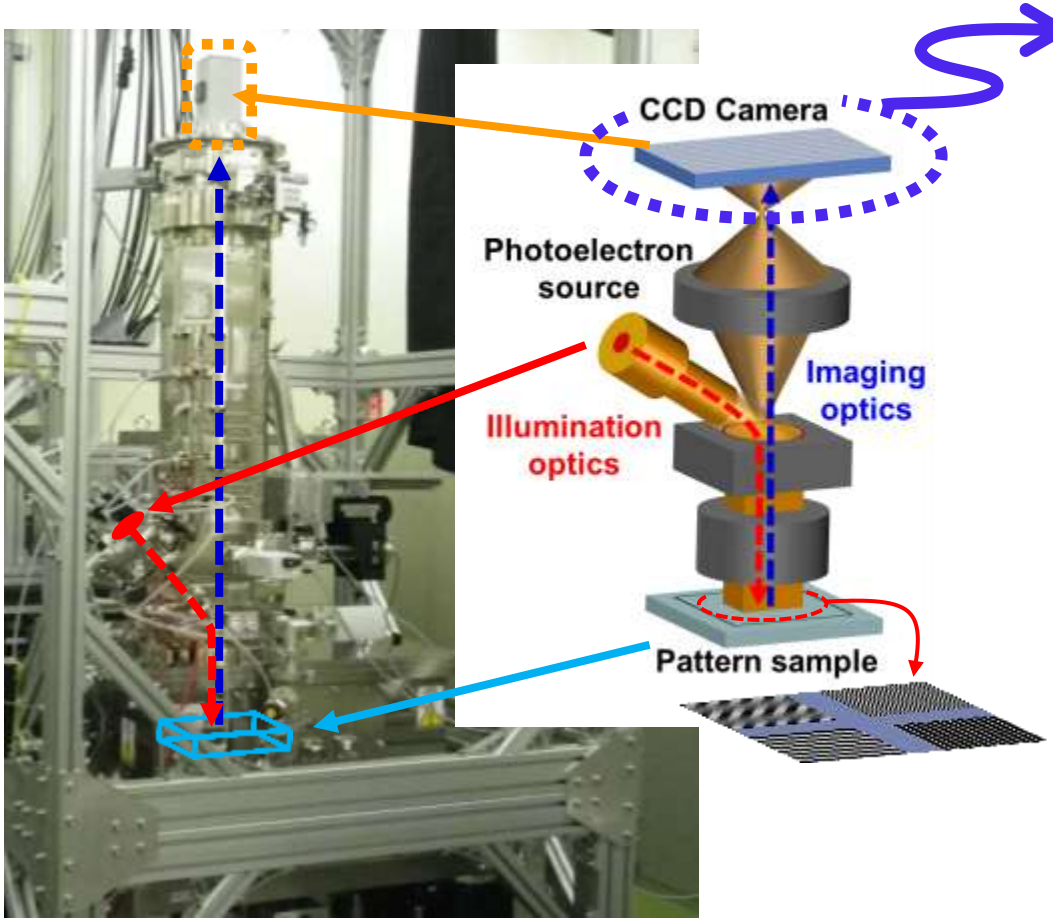
Image contrast at hp 64 nm pattern is consistent with designed value

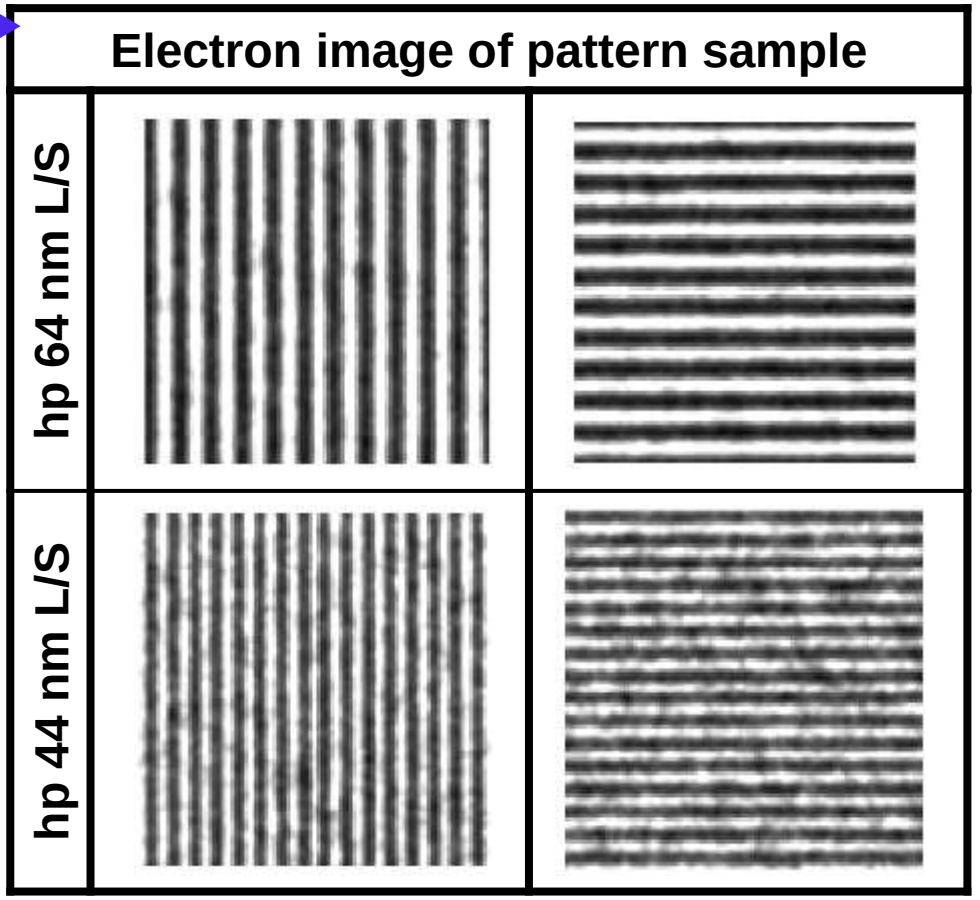
>3,000e- by developing tool

Watanabe et.al., BACUS 2013

Capturing higher resolution and higher SNR image

Image acquisition test of integrated optics





Hirano et.al., SPIE vol.8701

hp 64 nm and 44 nm L/S pattern images were successfully captured by the integrated PEM optics

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3. Image processing to capture 16 nm sized defects

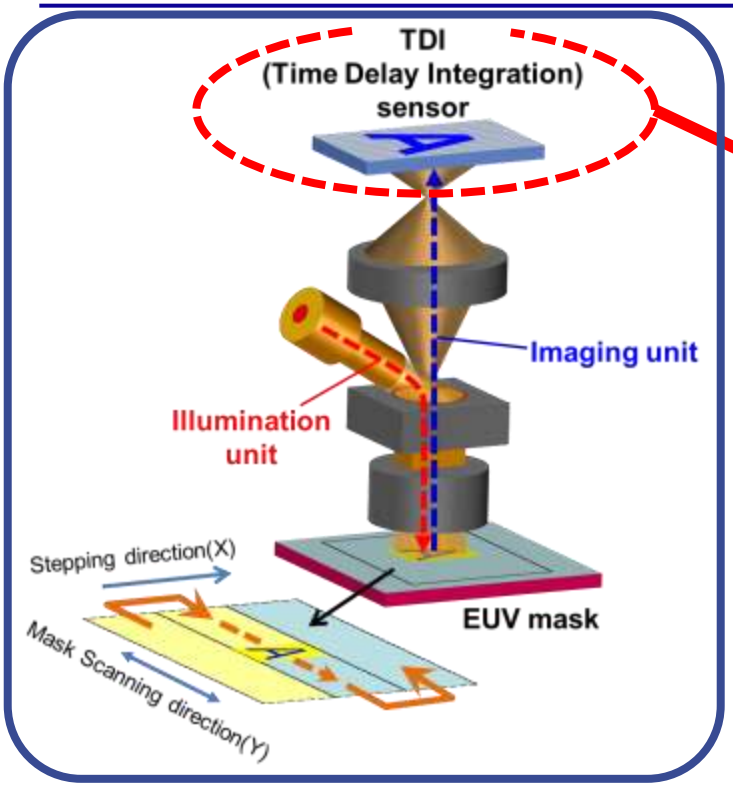
- Defect detection sensitivity evaluation of typical 16 nm defect was examined

- Capture rate comparison model and related methods are presented

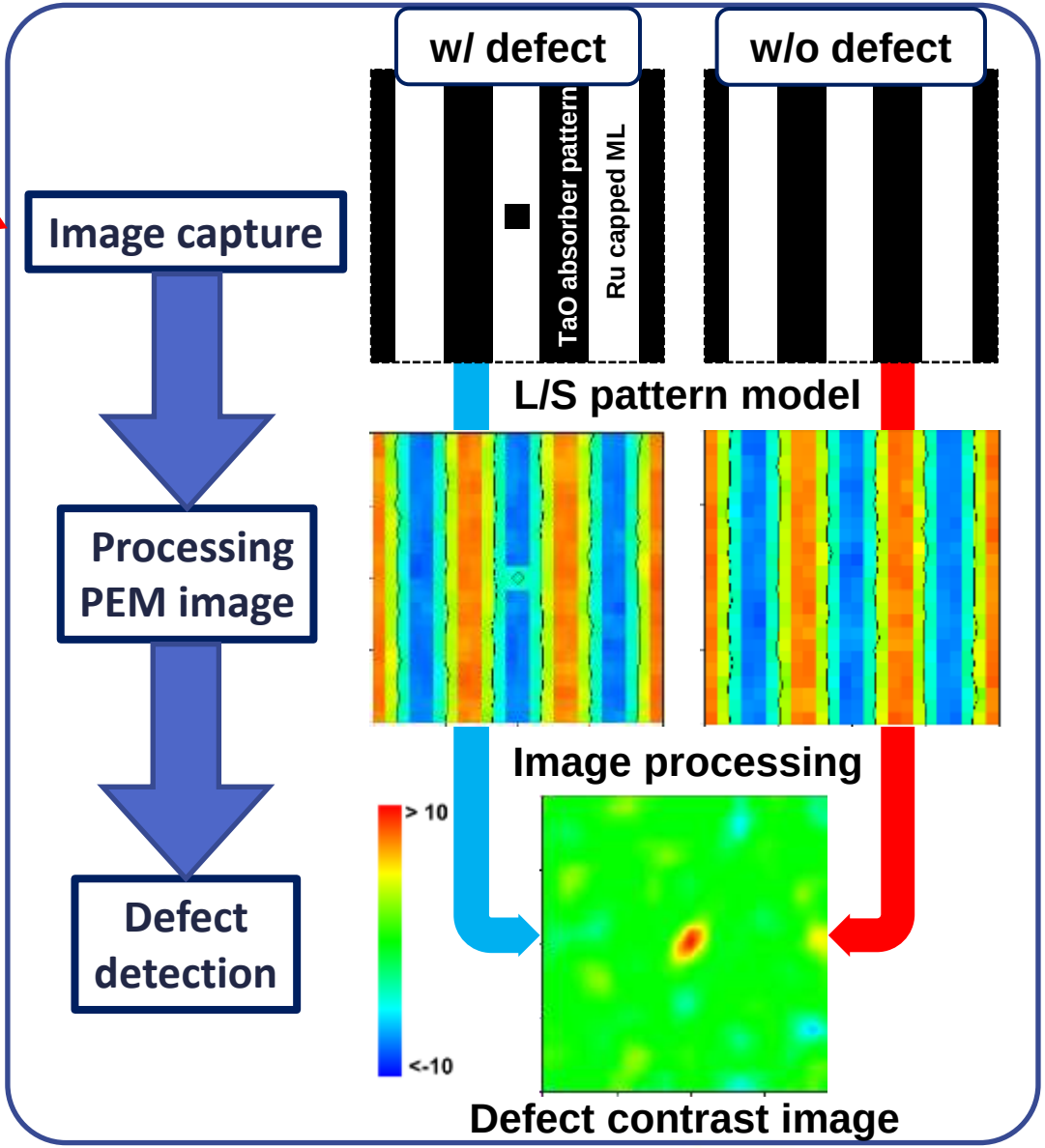
  100% capture rate of 16 nm defect was demonstrated

  Capture rate with larger pixel sizes are evaluated for higher inspection throughput

Image processing for hp 16 nm generation

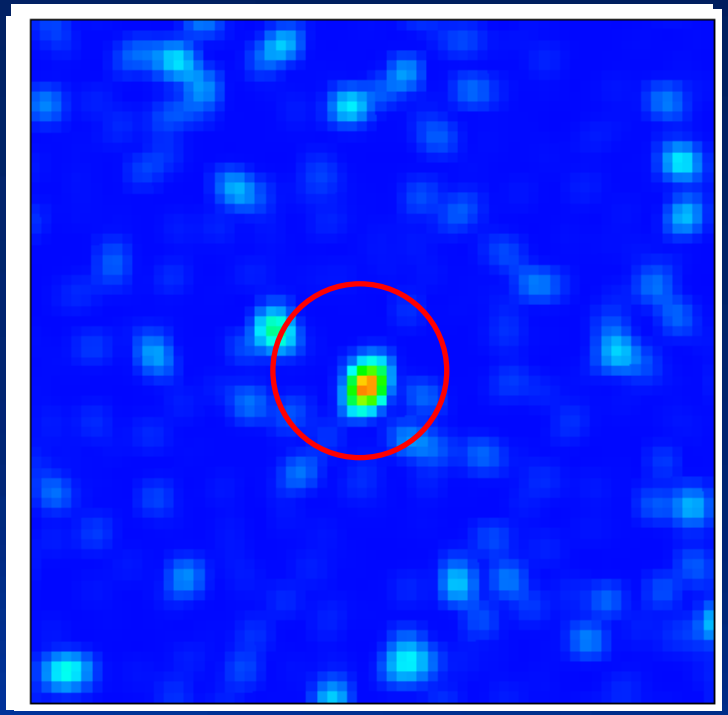


Defect detection by the defect contrast image

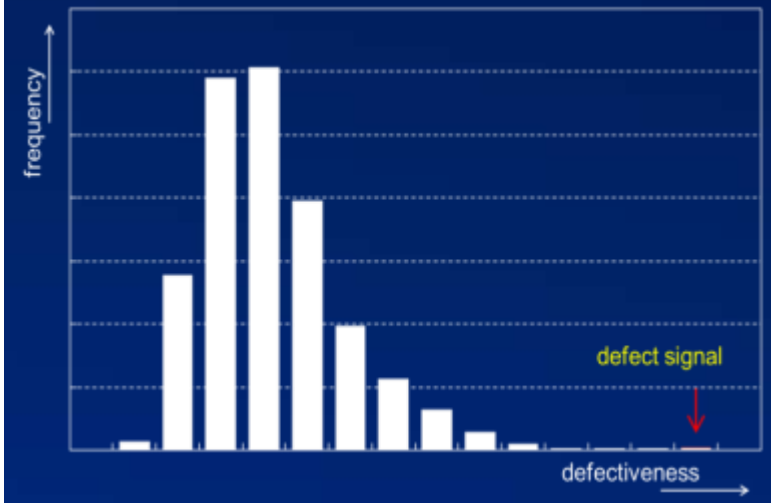


Processing PEM images

Defect identification by characteristic analysis



Defectiveness of 16nm pin dot



Defect signal identified by index of DEFECTIVENESS

Watanabe et.al., BACUS 2013

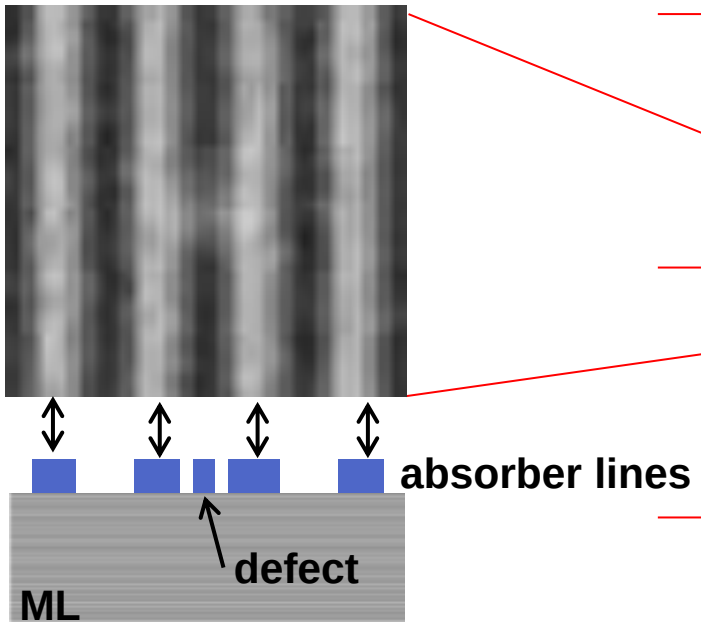
EIDEC

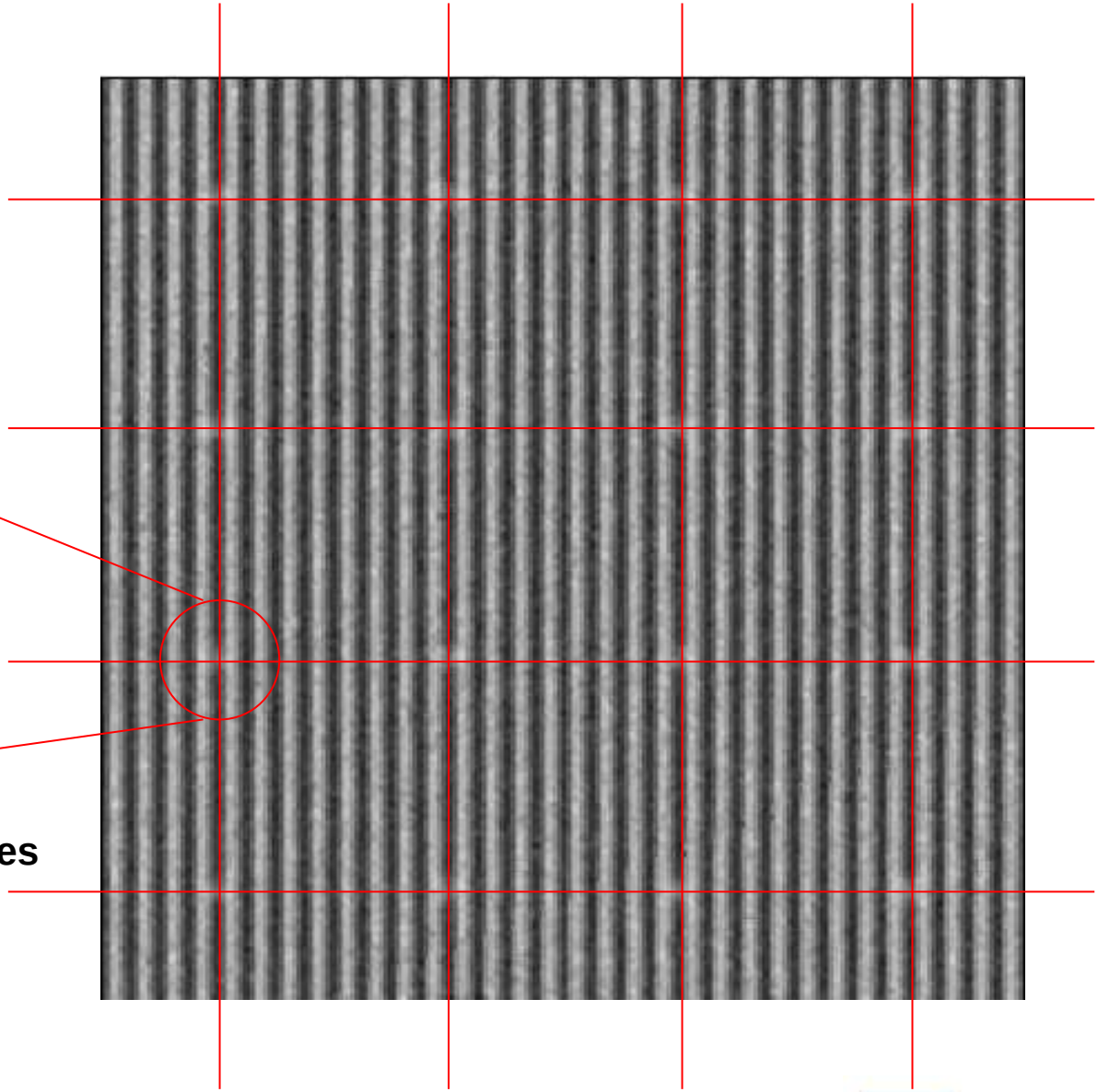
September 11, BACUS 2013

Achieve detection capability to capture 16 nm sized defect

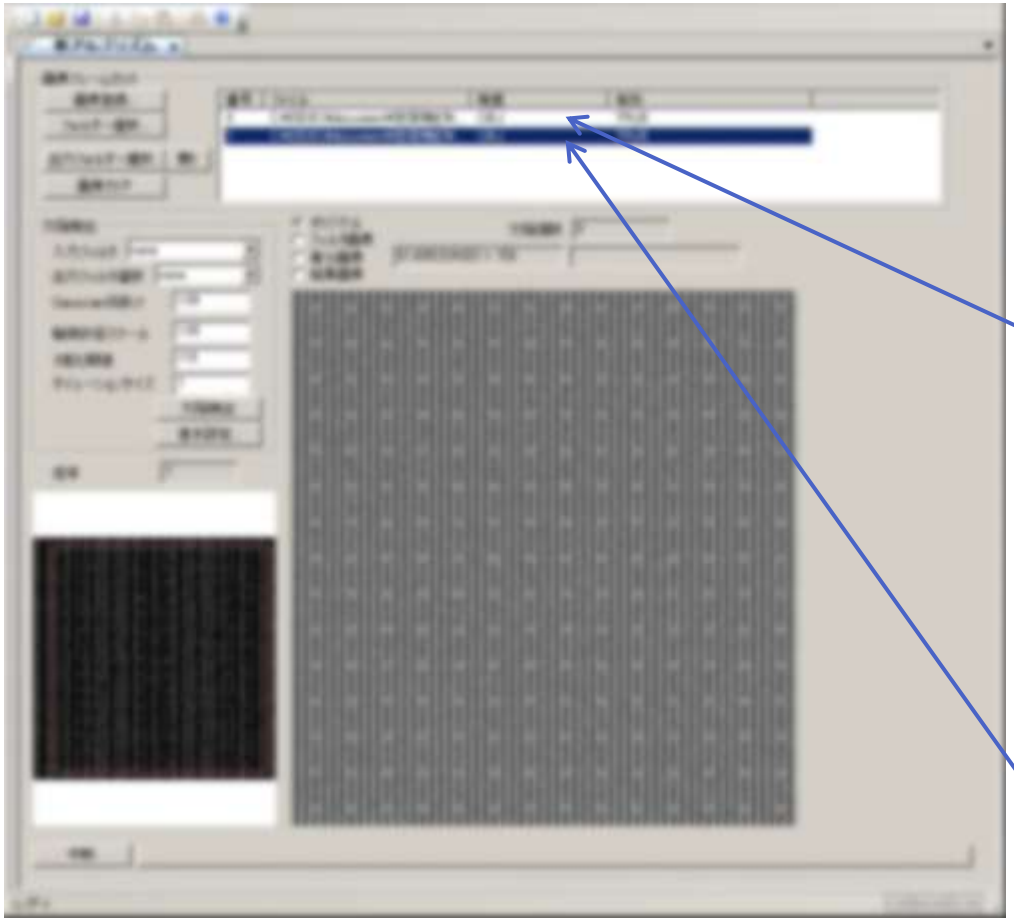
Capture rate comparison model

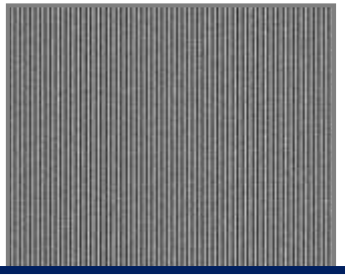
32nm pin dot array in 64nm dense lines (simulation image of 1keV incidence, 50 electron/16nm pixel)



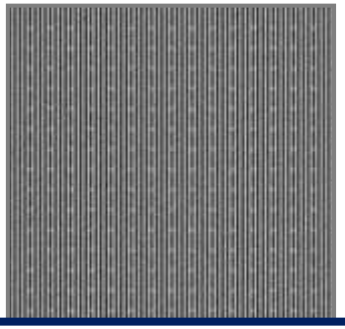


Capture rate estimation





Reference image



Defect array image

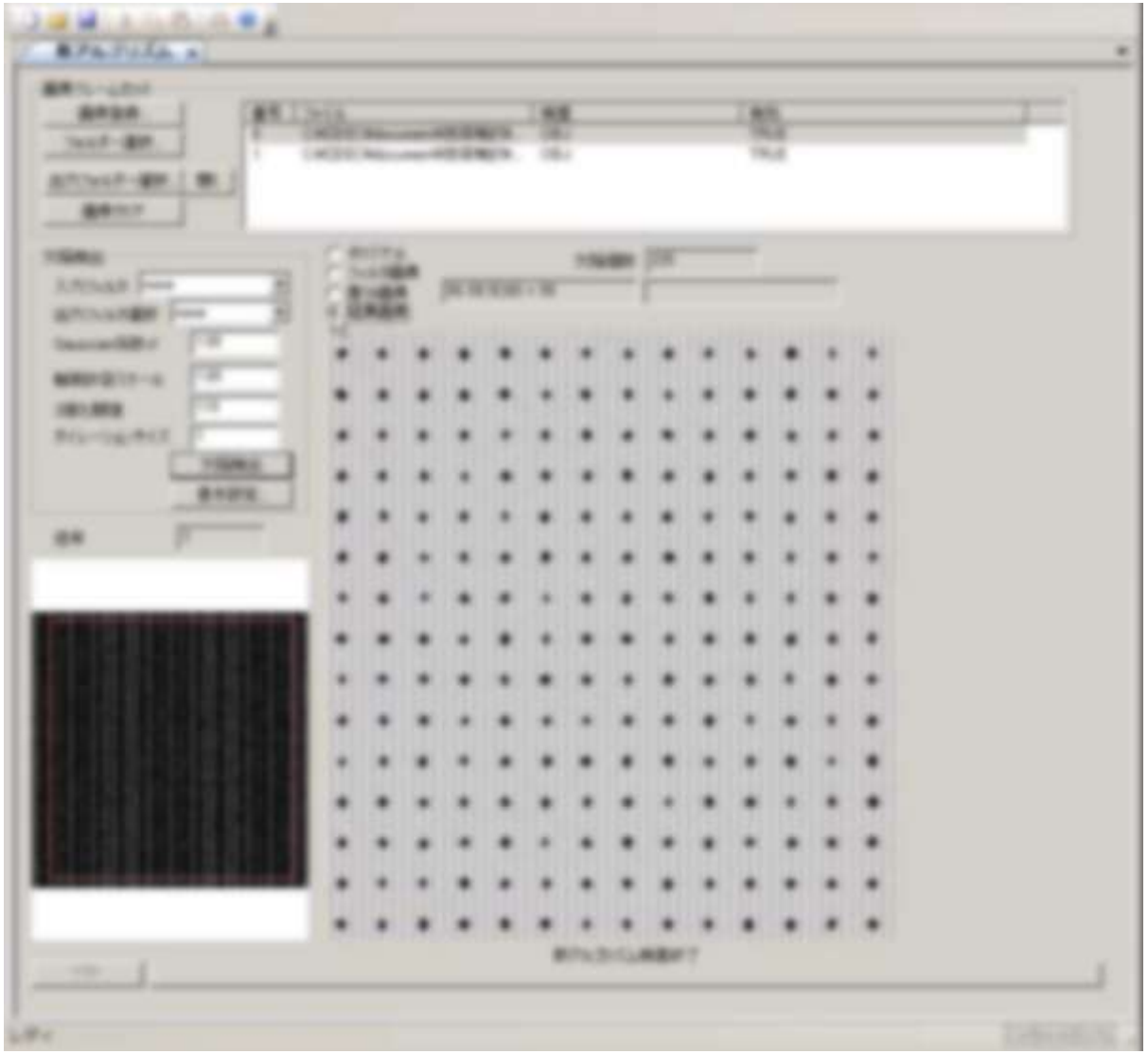
Input acquired Image

Alignment

Image difference

Defect identification

Capture rate estimation



Differential signal

↓

Defect signal:
More than sliced level

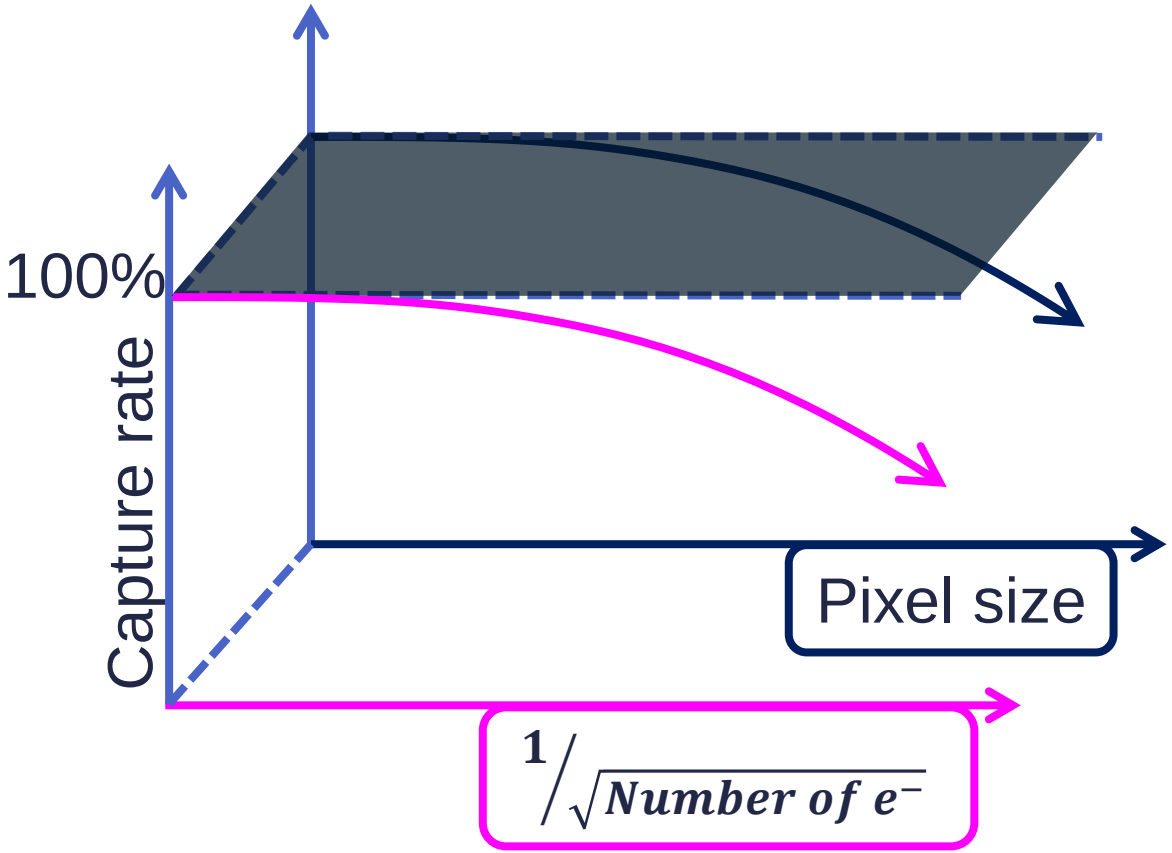
↓

Inspection capability:
Capture rate

Capture rate comparison -throughput improvement-

Defect capture rate

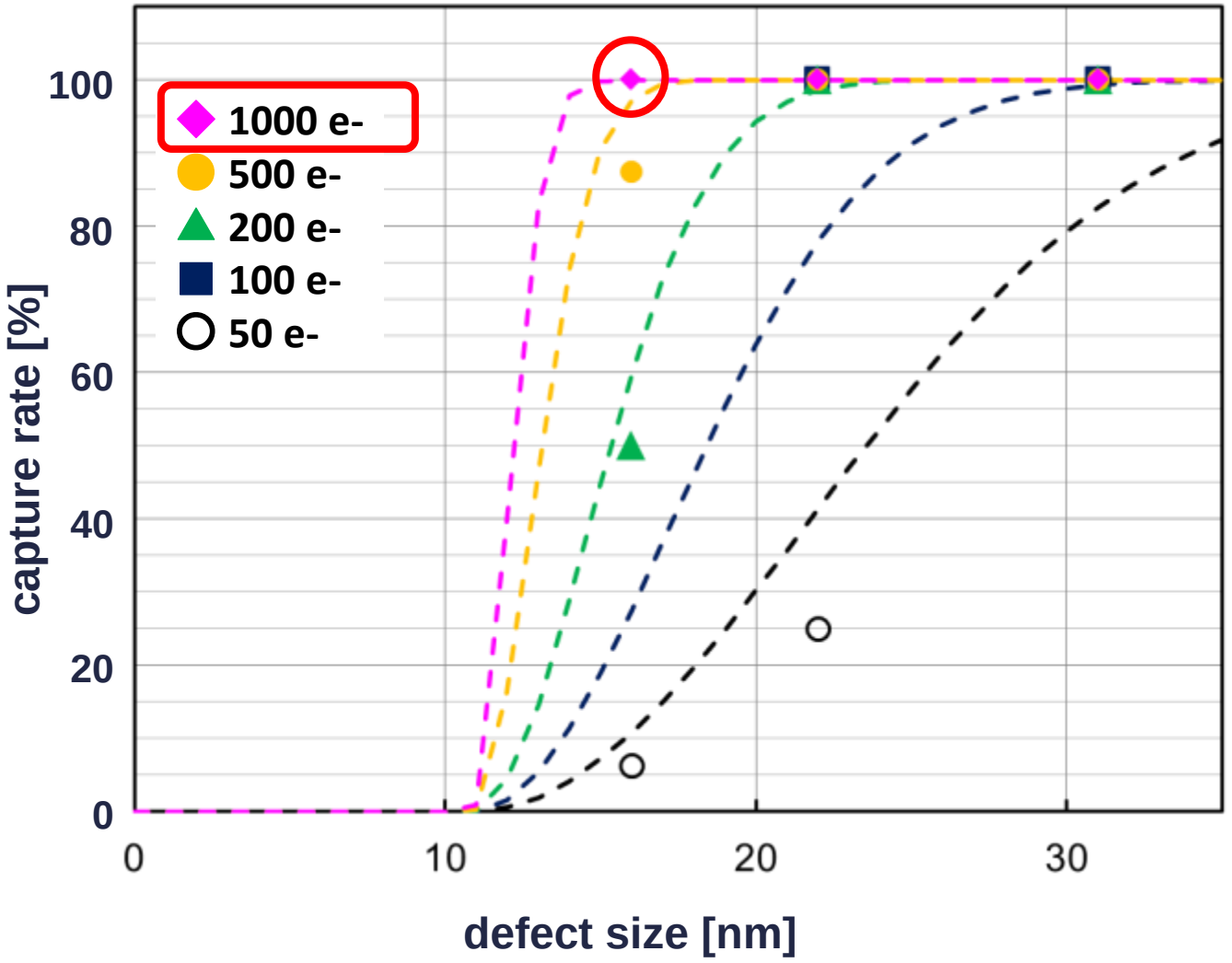
- Image contrast : sensor pixel size
- Image noise : number of e^-



Availability of larger pixel size

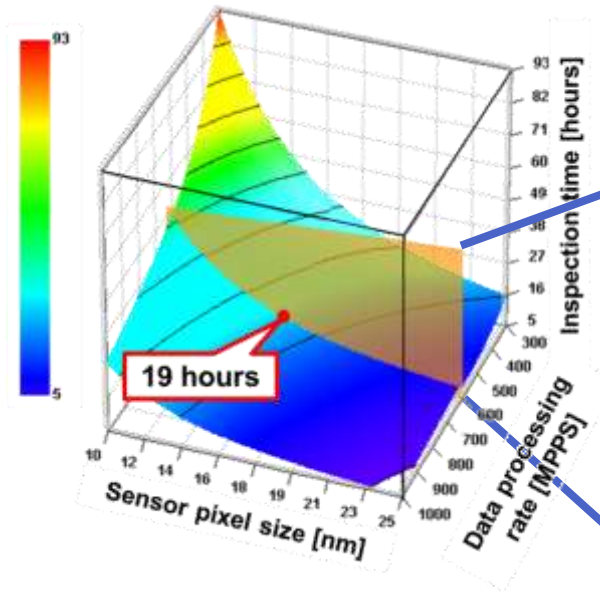
Capable of maintaining 100 % capture rate

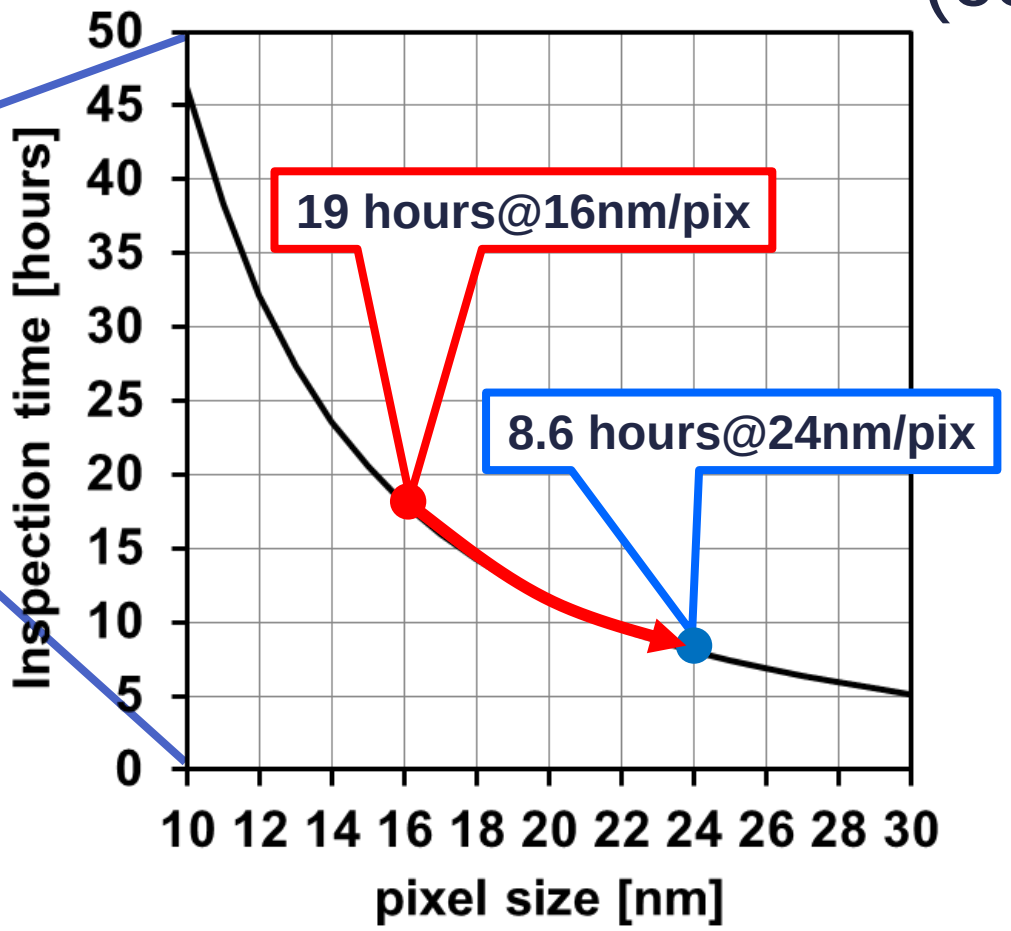
Capture rate comparison -throughput improvement- (cont'd)



Availability of 24nm pixel with sufficient intense electron illumination

Capture rate comparison -throughput improvement- (cont'd)





24nm/pix and 600MPPS data processing rate enables **8.6 hours** inspection.

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4. Summary and our Future work plans

- The expected image resolution by developing PI Electron Optics was verified.
- Identification of programmed defects on the mask of 16 nm size is verified by the developed image processing
- 24nm pixel size for image capture instead of 16nm enables 8.6 hours inspection per mask.

Next we will

- Complete the adjustment of PI tool for hp 16 nm HVM and will confirm full area inspection by March, 2014
- Develop noise reduction and signal enhancement techniques for hp 11 nm and beyond

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