EUV Mask Challenges, Status, and Closing the Remaining Technology Gaps

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SEMATECH
SEMATECH Champion Data

- Achieved 12 defects @ 45 nm or 8 defects @ 50 nm from M7360 inspection
  - 10 pits (from substrate), 1 handling defect, **1 defect from deposition**
- 65% reduction in defects from last year champion data (23 defects @50nm)
Yield analysis with M1350 (>70nm) and M7360 (>45 nm) [SiO$_2$ equiv.]

- Quality blanks: ~70% of yield below 30 defects >70nm from M1350
- 60% of Quality blanks have less than 30 defects >45 nm from M7360
- 20% of Quality blanks have less than 20 >45 nm from M7360
• 2015
  – Overall defect counts should meet requirements
  – Large size “Killer” defects still present

• HVM
  – Significant improvement needed to meet logic specifications

• Recent gains where made with the substrate
  – Reduction of cleaning induced defects
  – Substrate quality improvement at suppliers

• Process yields are not good
Substrate challenges

• Approximately 60%-65% of total mask blank defects originate from substrate defects

• Meeting simultaneously: substrate finish, figure (flatness), roughness and defect specifications is a significant challenge
  – Substrates are amorphous in nature, making it difficult to control CMP

• Reaching figure and finish specifications requires several iterations between global and local polish
  – This creates defects such as scratches or embedded particles

• The surface physical and chemical properties are modified by the polish steps and do interact with the cleaning processes
  – Tight management and control between final polish and cleans to ensure cleaning does not introduce additional defects
Substrate Defects

- Defect signature is different between suppliers
- Majority of substrate defects are not detection during inspection
  - Majority only become visible after ML deposition through decoration
  - Decoration through ML deposition is of limited value
    - Adds to cycle time and reduces learning cycles
    - Adds complexity to data analysis
- Will require substrate inspection capability
  - Current technology not able to detect sub-35nm pits (SiO2 equiv.) or shallow scratches
  - Plans for actinic inspection tools for mask blanks will not address this gap
EUV Substrate Gaps

- Defect levels, roughness and flatness specifications must be met for successful EUVL implementation.

### EUVL Substrate Requirements @22 nm HP node

<table>
<thead>
<tr>
<th>Specification</th>
<th>Source</th>
<th>Current Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>Defect size</td>
<td>ITRS 2011 Update</td>
<td>0 defects @ 40 nm+</td>
</tr>
<tr>
<td>Defect density</td>
<td>SEMI standards, 2009 update</td>
<td>0 defects @ 40 nm+</td>
</tr>
<tr>
<td>Roughness</td>
<td>P. Naulleau, LBNL</td>
<td>~0.05 nm</td>
</tr>
<tr>
<td>Flatness</td>
<td>ITRS 2011 Update</td>
<td>80-100 nm typical</td>
</tr>
<tr>
<td>Local Slope</td>
<td>ITRS 2011 Update</td>
<td>No issues</td>
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Mask Blank ML Deposition Challenges

• Approximately 20%-25% of total mask blank defects are deposition related
• Mask blank defectivity requirements have not yet been demonstrated
  – Large “killer” defects are a significant problem
    • Prohibits implementation of defect mitigation schemes
    • Comes from deposition tool and process
    • Detected on each mask blank SEMATECH has measured
  – Defect counts are close to meeting memory and pilot line logic requirements
    • Requires ~4X improvement to meet logic HVM specifications
• Deposition process yield
  – Quality deposition region is only 10%, at best, of overall process run
  – Target surfacing and burn-in critical
Tool and Process Limitations

• Limitations of deposition chamber and process
  – Overspray of ion source
  – Substrate Handling
  – Process yield, significant number of deposition cycles required to reach quality deposition region
  – Small process window for reflectance uniformity
  – Shield surfaces
  – Proximity of substrate to shields

• New Deposition Tool is Required
  – Cleaner, less divergent ion source
  – Chamber with a larger volume
  – New substrate location
    • May require flexibility to move substrate to multiple positions
  – Cleaner handling of substrates and mask blanks
    • May require dual pod solution
Optimized Ion Beam Profile For Defect Reduction

- Higher operating voltages/currents can give narrower focus on target
- New parameters give $< \frac{1}{4} \%$ of peak etch at edge of target
  - Does not completely eliminate sputtering of shields
EUV Mask Blank Gaps

- Defect levels, roughness, and reflectivity

<table>
<thead>
<tr>
<th>EUVL Mask Blank Requirements @22 nm HP node</th>
<th>Specification</th>
<th>Source</th>
<th>Current Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>Defect size</td>
<td>18 nm</td>
<td>ITRS 2011 Update</td>
<td>12 defects @ 45 nm+</td>
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<tr>
<td>Defect density</td>
<td>0.002 defects/cm2</td>
<td>Device Manufactures</td>
<td>0.043 defects/cm2</td>
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<tr>
<td>Roughness (rms)</td>
<td>0.05 nm</td>
<td>Defect Metrology</td>
<td>~0.14 nm</td>
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<tr>
<td>Reflectivity</td>
<td>65%</td>
<td>ITRS 2011 Update</td>
<td>63%-64%</td>
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</table>
Mask Blank Roadmap

### Blank defects

<table>
<thead>
<tr>
<th>Year</th>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
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<tbody>
<tr>
<td>2011</td>
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<td>2012</td>
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<td>2014</td>
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<tr>
<td>2015</td>
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**Pilot start**
- 1 defect > 150nm
- 27 defects < 150nm

**SMT**
- 19 defects > 50nm
- 8 defects > 50nm

### Industry Need

- **Memory**
  - 0: > 150 nm
  - 22 defects @ 50 < x < 150 nm
- **Logic**
  - 0: > 100 nm
  - 3 defects @ 50 < x < 100 nm

### Tool Capability

- **ML Dep.**
  - Veeco LDD1
  - New tool needed YE 12

### Substrate Inspection
- Available @35nm+
  - For substrate
- Low cost new tool needed: @25nm+
- Low cost new tool needed: @20nm+

### Blank Inspection
- Available @40nm+
  - For blanks
- Low cost new tool needed: @25nm+
- Actinic needed
- Low cost new tool needed: @20nm+
High Level Requirements for Actinic Blank Inspection

• Inspection requirements:
  – Substrate pits/bumps (phase defects) must be detected
  – Particles, even just under the capping or top multilayers (amplitude defects) must also be detected

• Classification and review requirements:
  – Review should accurately localize the defects so mitigation by pattern shifting can be used.
  – Defects should be classified, and near the sensitivity limit, reviewed to determine printability
Defect Trends of Suppliers

- Defect trends of mask blank suppliers are improving
- However, delivered mask blanks will have some defects
- Defect printing mitigation methods will be needed
Mask Layout Pattern Shift

• Position design layout so that all mask blank defects remain covered by the absorber

• Remaining questions:
  – Probability of eliminating all blank defects using pattern shift
  – Potential impact on field size
  – Allowed defect count and size distribution

• Successful pattern shift requires:
  – Excellent coordinate accuracy
  – Low-defect fiducial process
  – Infrastructure for sorting blanks and matching to mask patterning
  – All printable defects need to be detectable
Current EUV Mask Technical Gaps

• Challenges with defects continue:
  – Substrate Defects
    • Defects become visible after deposition
  – Multi-Layer Deposition
    • Killer defects from ML deposition still an issue
    • Low process yield
  – Defect free EUV masks
    • Mitigation of mask blank defects will be required
  – Metrology
    • What inspection capability existing is running out of steam
    • Inspection tools required to meet HVM requirement are not available

• Infrastructure
  – New generation of ML deposition tool is needed
  – Metrology and inspection tool development required
Closing the Gaps

• Mask blank suppliers maintaining their current roadmaps
• Consortia and Mask Blank Suppliers continue to work on EUV development
  – Substrate polishing and cleaning
  – ML Deposition tool and process optimization
• Consortia and Tool Suppliers are addressing tool gaps
  – Inspection tools
    • Mask Blank (substrate?)
    • Pattern Mask
  – Deposition
    • Next generation IBD tool
• Pre-production exposure tools
  – Increasing mask manufacturing cycles of learning
  – Driving focus on process yield across all areas of mask manufacturing
    • Lack of metrology tools demands wafer print for process and defect verification which is slowing learning
• Increased focus by industry on addressing HVM needs
Thank You
Accelerating the next technology revolution

Research

Development

Manufacturing