Progress and remaining challenges of EUV lithography for memory IC manufacturing

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✔ Closing
Patterning of memory IC

Extremely fine and dense patterns, while simple and repeating!

Lines and spaces

Contact holes

or together

LELE, Spacer ...
Hole pattern by crossing lines

- sub-resolution contacts formed by multiple crossing lines
Traditional LELE DPT

- for Complex layout in DRAM periphery

ArF immersion capable of memory patterning whatsoever with increased process complexity
Moore’s law in Economics

2X Bit growth every 2 years
=Bit price -50% every 2 years

Very cost sensitive business!
Virtue of lithography for memory

Productivity! Productivity! Productivity!

and

Resolution (CD uniformity) +
Corresponding overlay control (~20% of D.R. or less)
Defect control
Complexity of DPT and cost

※ Rudy Peeters (ASML) EUVL Symposium 2011
Simple economics of double patterning

☐ If
  • Cost increased by 1 DPT/SPT ~ 2%
  • Steps increased by 1 DPT/SPT, 10~15 steps (Capa. loss~3%)
  • Net die increase by shrink ~ 35%

+ Yield-loss, TAT loss,
  Layout design complexity,
  Clean Room consumption

Shrink will not help if too many D(S)PT layers are used
Scanner throughput is key for cost

- Patterning Cost vs. scanner throughput

First overcome D(S)PT, then get close to the level of ArF-I single
Unanswered question

**Economic**  
**User-friendly**  
**Versatile**  
**Lithography**

**Expensive**  
**Under-powered**  
**Vague**  
**Lithography**
Real source improvement

After NXE3100 install, observed real progress, though not sufficient for HVM

*Throughput : based on ASML ATP
History of 248nm & 193nm

10X power up for 9 years in 248nm, for 2.6 years in 193nm
How long for 25X gap in 13.5nm?
Improvement in next year very crucial, will decide the future

Source prediction
Progress continues in resolution

Yearly progress of EUV resolution performance

2007 2008 2009 2010 2011 2012
40nm 32nm 28nm 25nm 22nm 20nm

[,] conventional [,] dipole [,]

Strong dipole @IMEC

※ T. Wallow(GF) SPIE 2012

※ T. Wallow(GF) SPIE 2012

17.5nm hp 17nm hp 16nm hp
EUVL CD uniformity has improved significantly through various process optimization of resist, mask, and illumination modes.
Regarding C/H CD uniformity, EUV lithography is comparable with ArFi DPT.
Resist Screening: Local CD variation

- High sensitive with better performed resist is essential

Dose sensitivity of resist more and more important as EUV source reveals difficulty in increasing power level

※ K. Ban (SK hynix) SPIE 2012
On product overlay to ArF-i

 NXE3100 Matching overlay to NXT1950i

- Correction per exposure applied with linear alignment
Intra-field overlay error

- measured with fully rotatable mask

Field position dependent

Mask A @ ADT

- 17.5(X)/14.9(Y)

Mask B @ PPT

- 3.8(X)/6.1(Y)

Mask position dependent

- 2.46(X)/1.9(Y)

- 1.49(X)/2.15(Y)

Early result promising, considering mask flatness effect of EUV

※ B. Lee(SK hynix) EUVL Symposium 2011
Intra-field overlay after RegC®

- RegC applied to 193i mask only because of backside opacity of EUV mask

Carl Zeiss’ RegC®

Pre RegC®

Post RegC®

Intra-field term improvement 20%

4.74(X)/5.29(Y)

3.76(X)/4.18(Y)
EUV backside change required for RegC®

CrN openings for laser transmission

Transparent Conductive Material

Conductive film for Electrostatic chucking

Backside of EUV mask blank need to be changed for RegC application
Mask defect statistics

- Defect counts with different inspection tools

No strong correlation between blank/mask pattern/wafer pattern defects

A~F: contact hole / a~c: lines & spaces
Mask defect status quo

☐ Defect capture-ability of different inspection methods

- Mask PI
- SEM based on wafer
- Wafer PI

Total defect

31% Not printed on wafer
41% Not detected by wafer PI
28% Detected by wafer PI

Un-captured (?)

15% among 100% defects captured by Mask PI

Make wafer PI capture all defects recognized by SEM!
Mask operation; EUV vs. DUV

**EUV**
- Dual PODs, pods exchanger
- Inner POD(EIP)
- Particle adder
- Thermal deformation(?) haze

**DUV**
- Shipping box
- With pellicle
- Particle growth (haze)

Proc. SPIE 83220S-2
Mask operation; EUV vs. DUV

Requirements

- Mask Transportation within dual pods
- Pellicle if possible
- Keep Inner pods clean
  (inner pods inspection method)
- No adder during exposure
- Inspection of mask defect on wafer
- Mask cleaning at proper time

Dual PODs, pods exchanger

Inner POD(EIP)

Particle adder
Thermal deformation(?) haze
Particle adder by wafer inspection

3 adders during 7 batches for 10 days confirmed
Particle adder per pass on mask

NXE reticle defect adders performance is improving
Target: <0.01 Particles-per-reticle-pass (PRP)

At least, added particles should be zero during exposure
Mask transport within dual pods

- Ground transportation of 80km distance in 5 cycles of round trip

Pre inspection

Final inspection

No adder found on mask!
Test done on Gudeng, Entegris pods test will follow
Mask defects on memory

- Memory IC truth

1. 10~20 dies within a mask (chip size small)
2. Redundancy included
3. Defect in Cell/Core area can be repaired (not always)
4. Killer defect in peripheral circuit area with relatively low printability because of relaxed design rule
**How many particles?**

- probability of particle on mask

![Graph showing probability of getting particles vs. reticle load cycle](image)

- If 2% rework rate assumed as a guide-line, mask cleaning should be after every 2 batches @0.01 PRP
- Particle adder can be more than a increasing rework rate?
EUV readiness in overall flow

- Layout
- OPC: Flare/ shadowing
- Mask patterning
- Mask pattern inspection
- AIMS & Repair
- Blank
- Blank Inspection
- Resist/ Under-layer
- Pellicle-less Mask handling
- Wafer Patterning
- Wafer pattern inspection
- Etch
- Out gassing qualification
Mountain looks very steep and un-challengeable at far sight, but there always passages to climb over as we get close
Thank You...