IEUVI Update

Oct 19, 2011

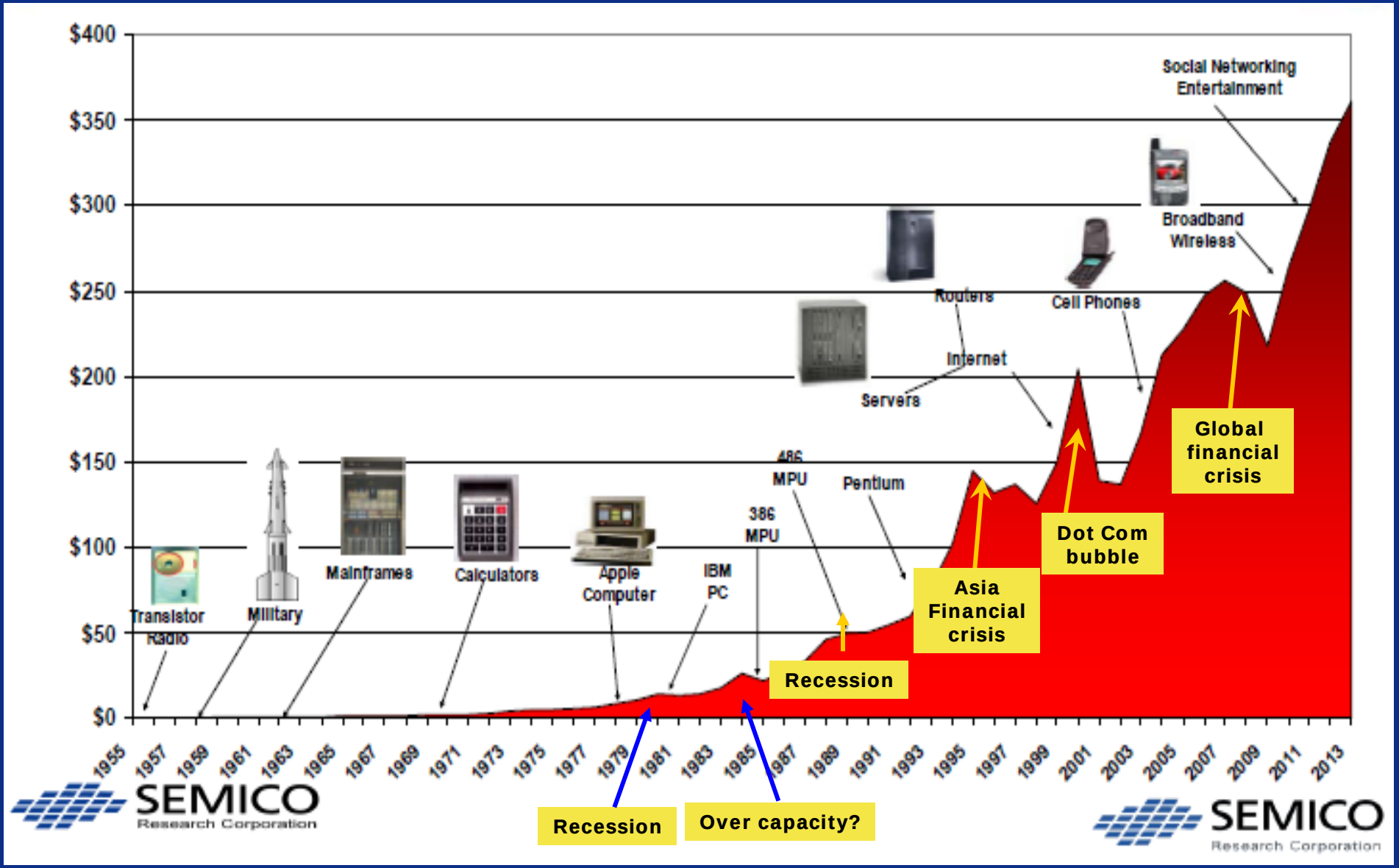
Paolo Gargini

Chairman ITRS
Chairman IEUVI
IEEE Fellow
Intel Fellow

Agenda

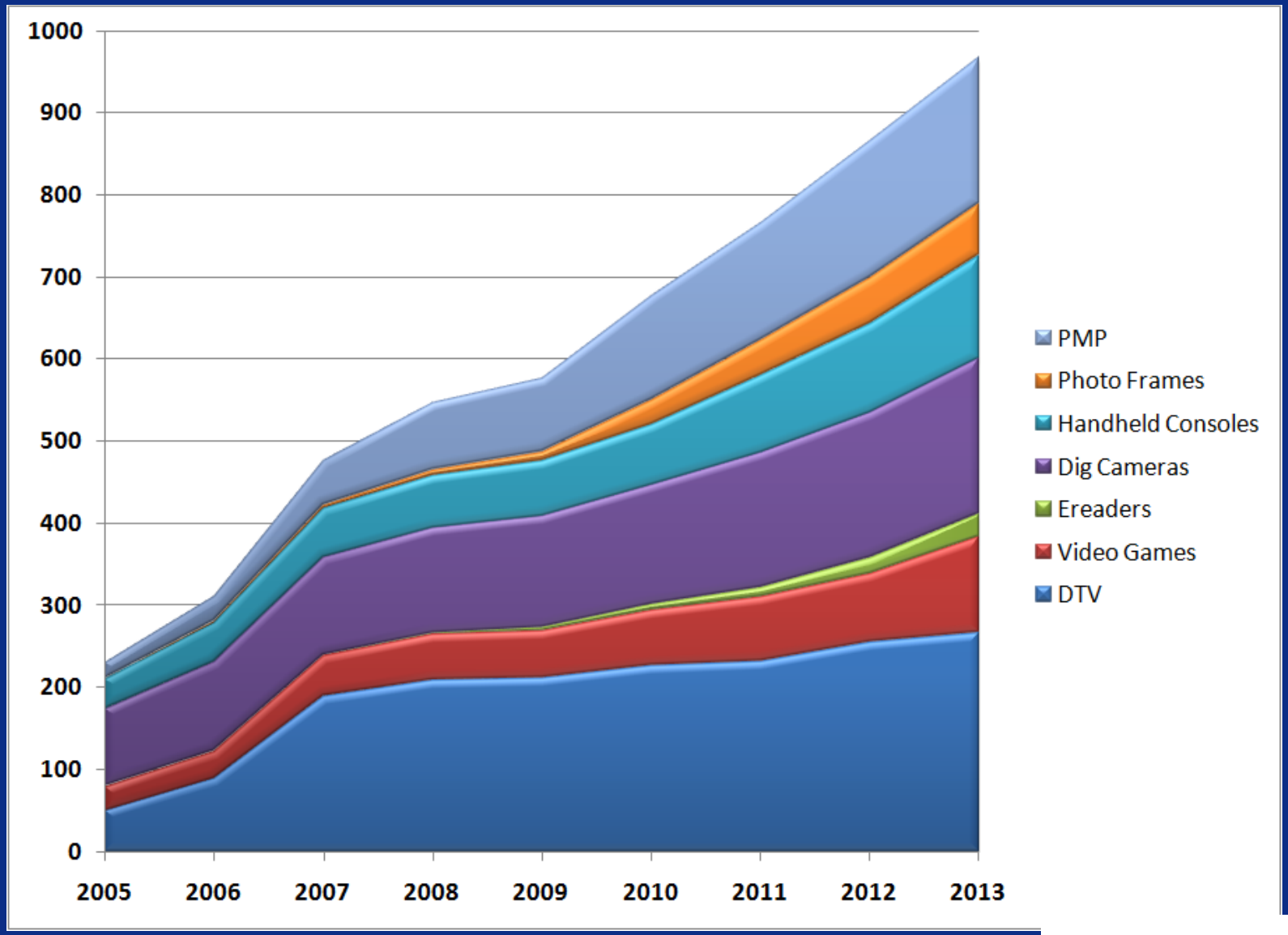
1. Why?
2. What?
3. How?
4. When?
5. Conclusions

End Application Drivers ($B)

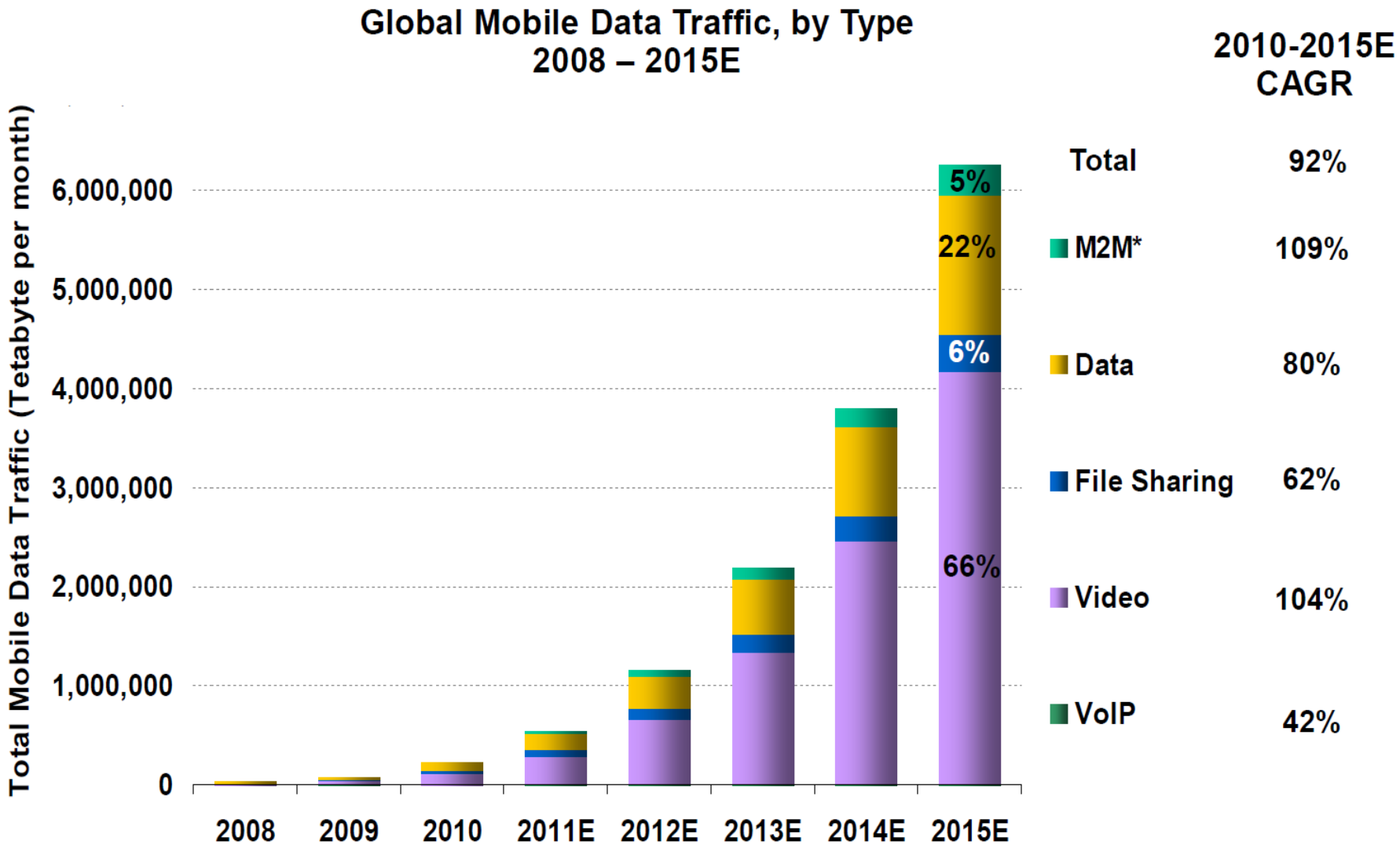


Top Consumer Electronics

Millions of Units

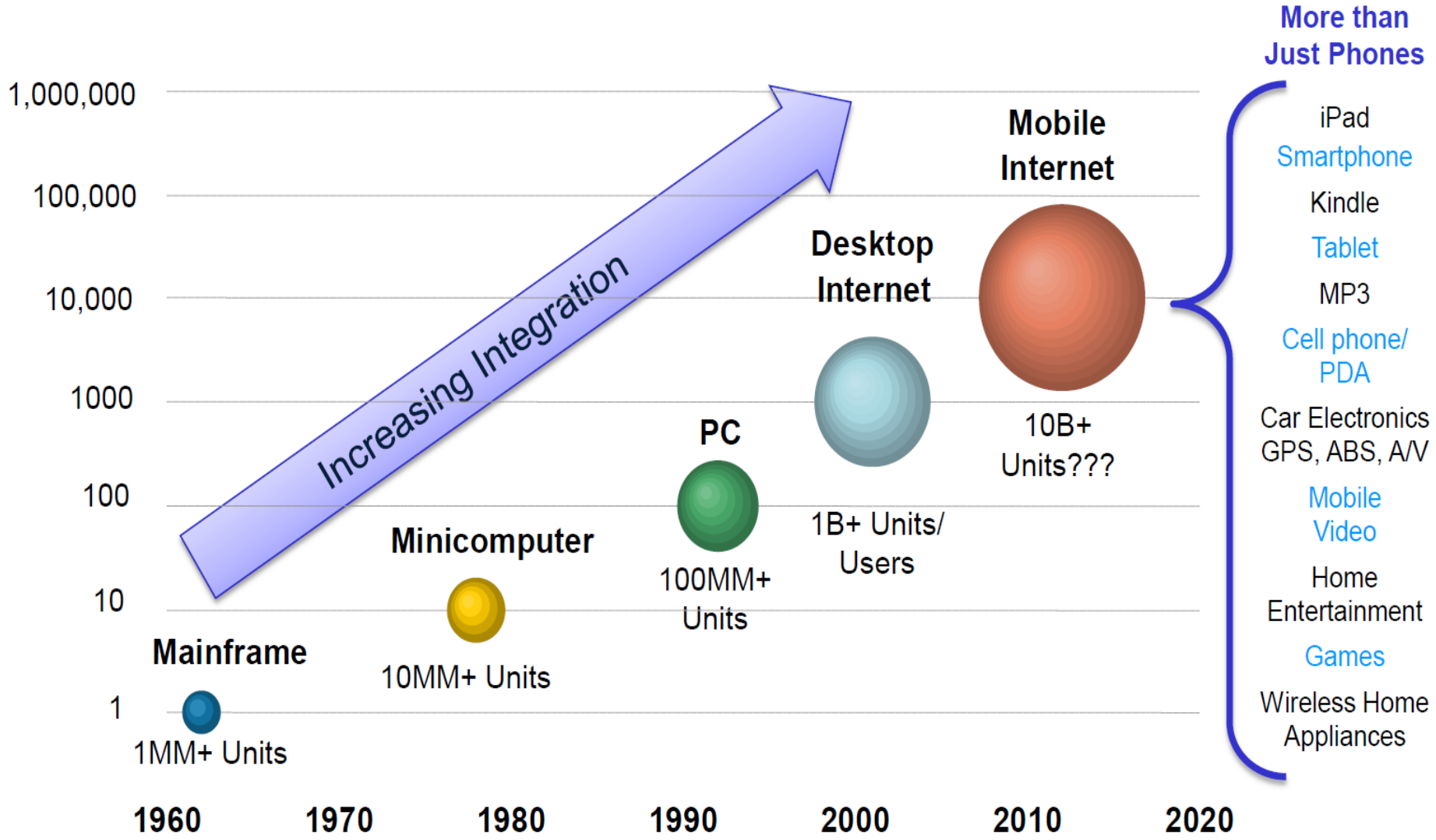


SEMICO Research Corporation



Source: Cisco Visual Networking Index (VNI) Global Data Traffic Forecast, 2010-2015

Computing Growth Drivers Over Time, 1960-2020E



Note: PC installed base reached 100MM in 1993, cellphone/Internet users reached 1B in 2002/2005 respectively;
Source: ITU, Mark Lipacis, Morgan Stanley Research.

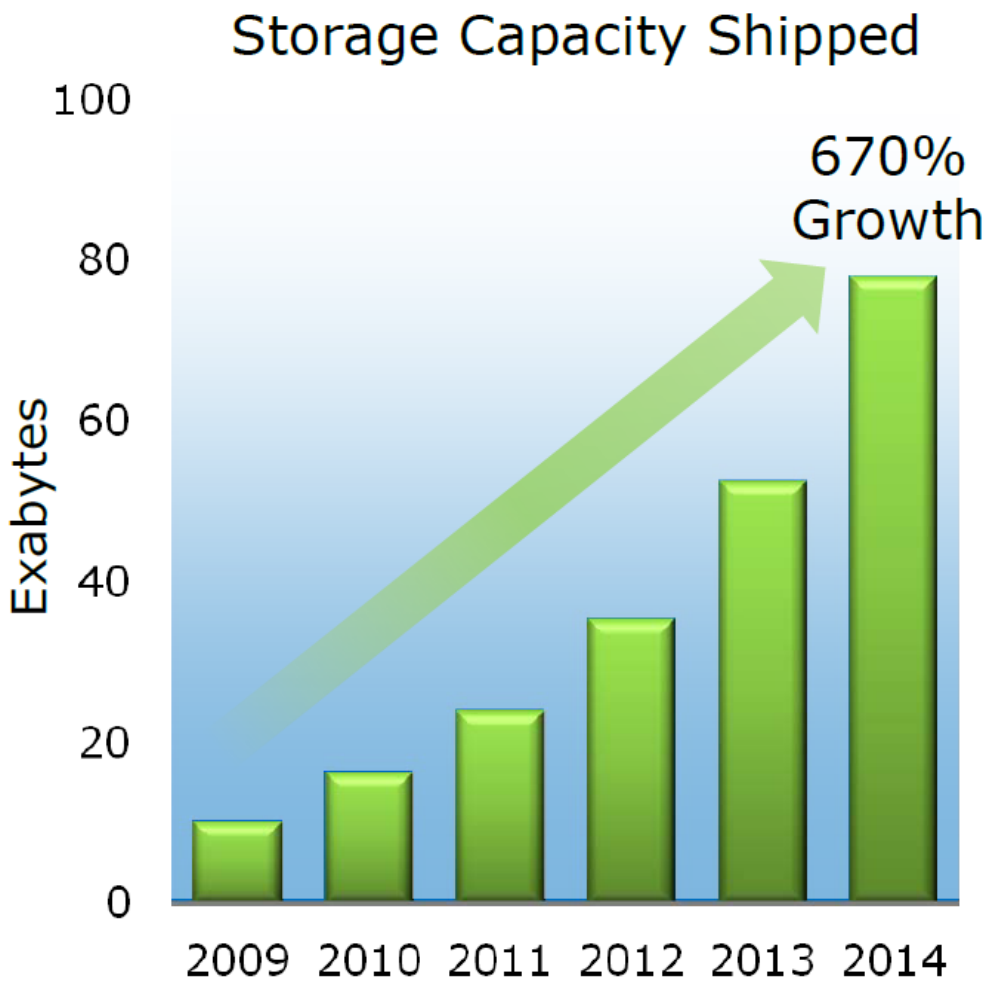
Surge in Storage

"More video uploaded to YouTube in the past 2 months than if ABC, CBS and NBC had been airing new content 24/365 since 1948."

— Gartner

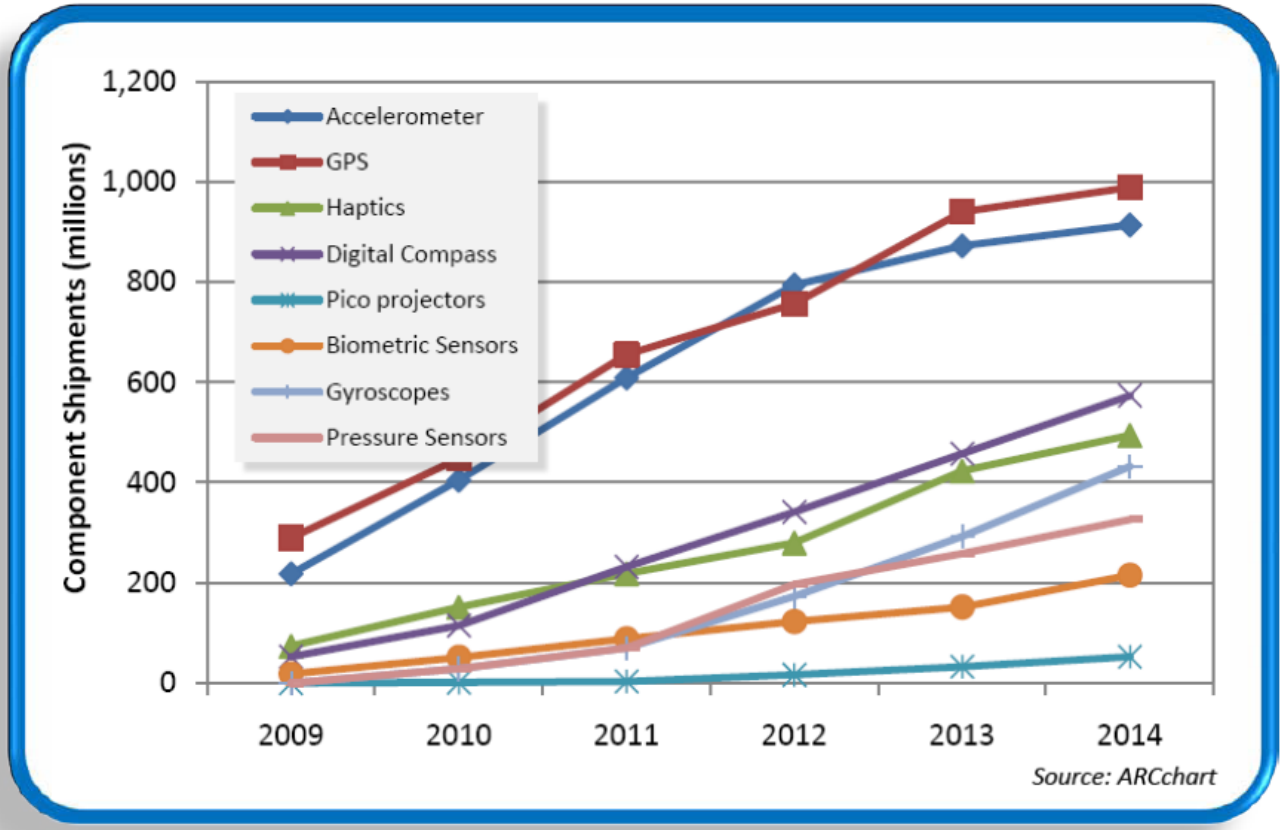
"Big Data last 5 years: 800% growth; 80% unstructured → effective tiering needed."

— Gartner



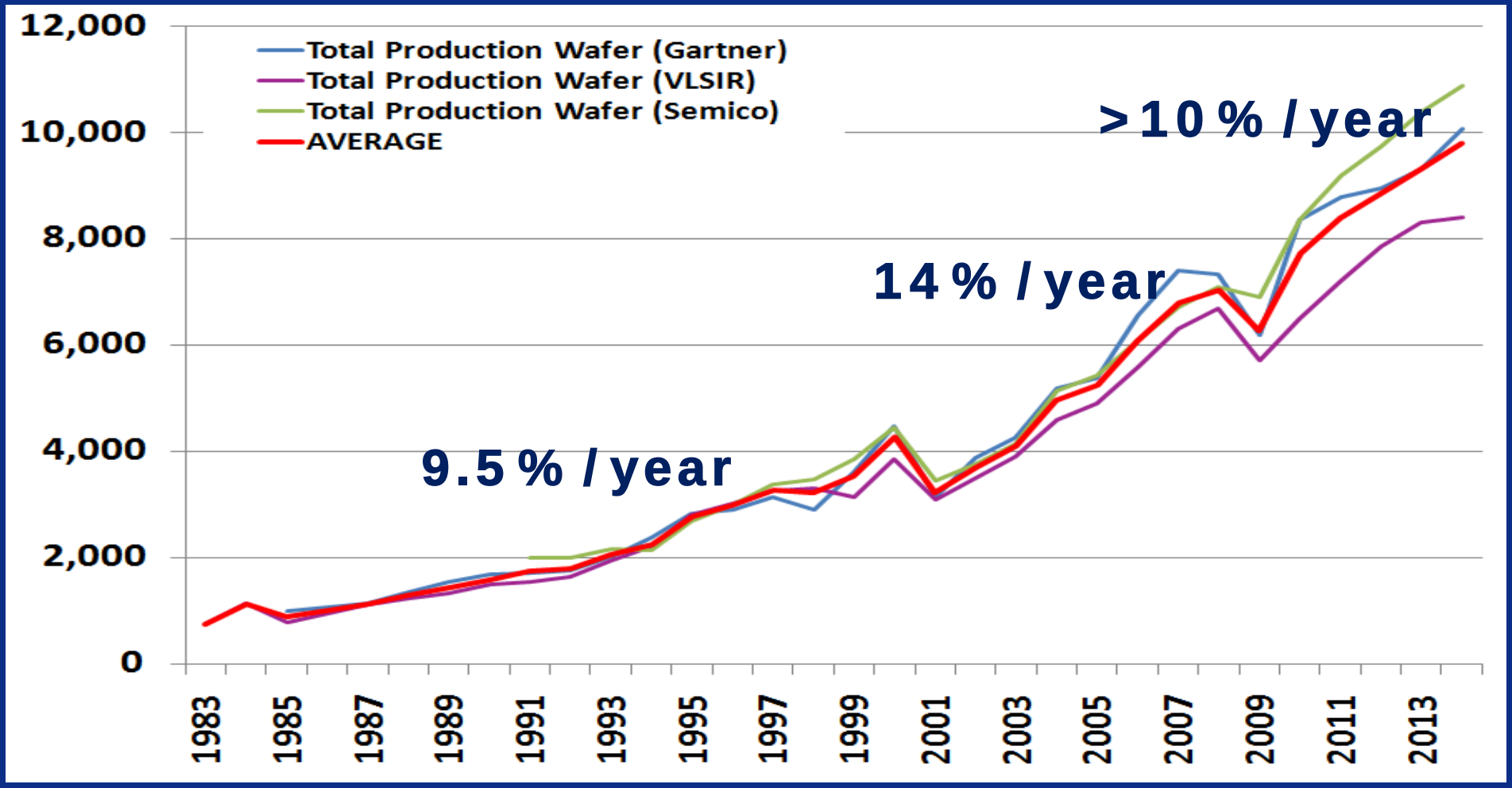
Surge in Sensors

- Downloaded Apps Require Sensors
- ~1B GPS, ~900M Accel, ~600M Compass, ~450M Gyros by 2014



Worldwide Silicon Demand

(in Millions of Square inches)



Wafer demand continues to increase

Wafer Size Conversion History

200mm/1990 300mm/2001 450mm/2012

38/94

Semicon West, July 12, 2004 P. Gargini

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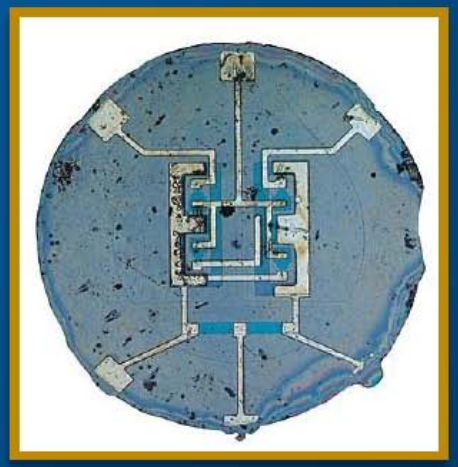
A Half Century of Integration

Silicon

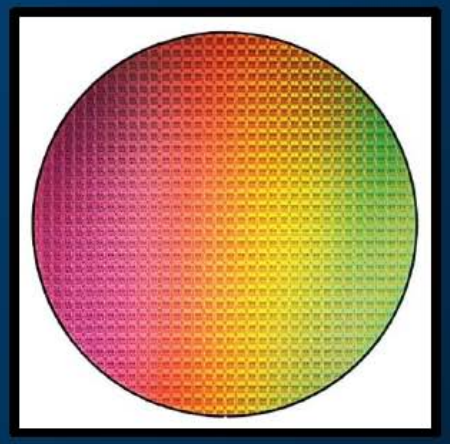
1959



First Silicon IC (Noyce and Kilby)

~50 years

Today

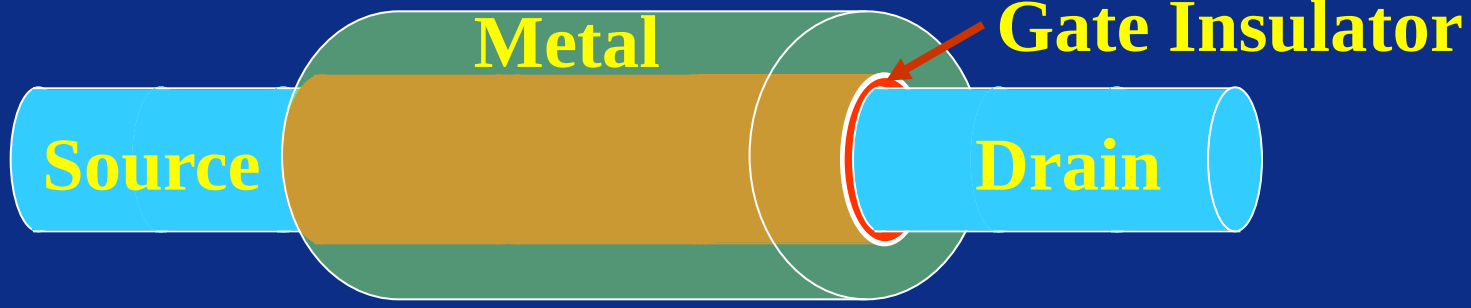


Billions of Transistors

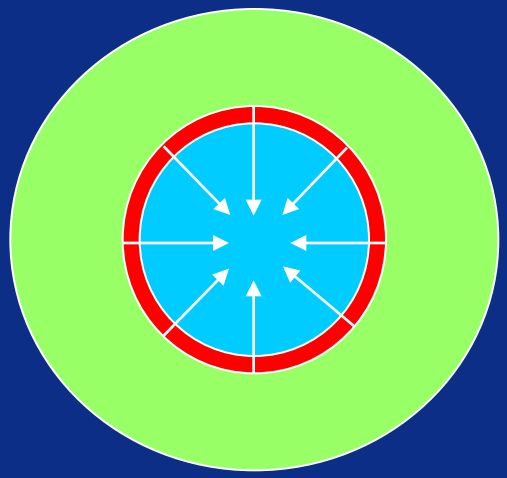
We have gone from 2 transistors to 2 billion

Silicon Technology has made this all possible

The Ideal MOS Transistor



Fully Surrounding Metal Electrode



Fully Enclosed, Depleted Semiconductor

High-K Gate Insulator

Band Engineered Semiconductor

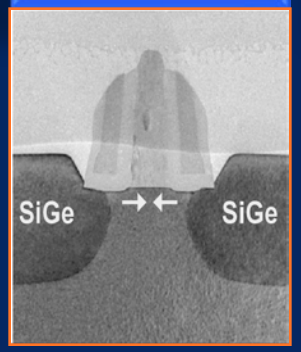
Low Resistance Source/Drain

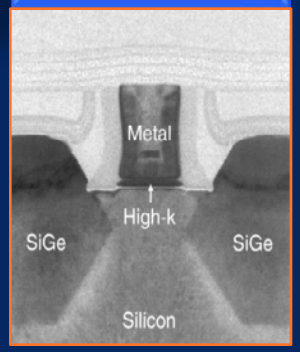
ITRS 1998

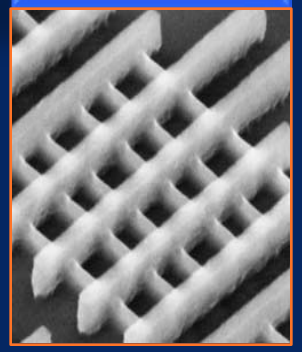
From My Files

Transistor Innovations Enable Technology Cadence

2003	2005	2007	2009	2011
90 nm	65 nm	45 nm	32 nm	22 nm







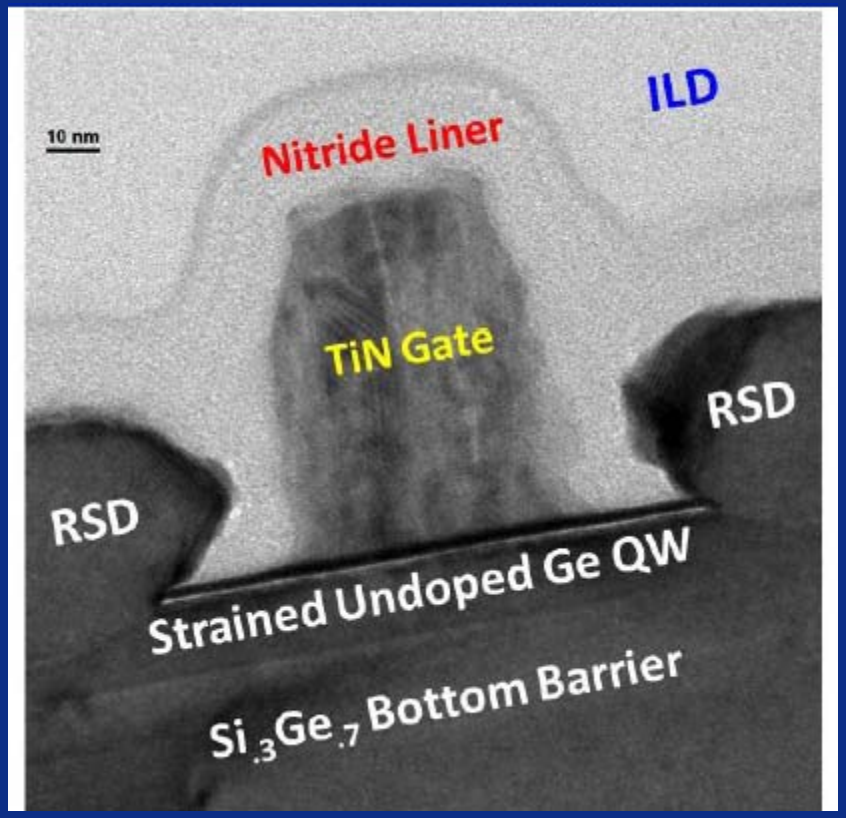
Invented SiGe Strained Silicon	2nd Gen. SiGe Strained Silicon	Invented Gate-Last High-k Metal Gate	2nd Gen. Gate-Last High-k Metal Gate	First to Implement Tri-Gate

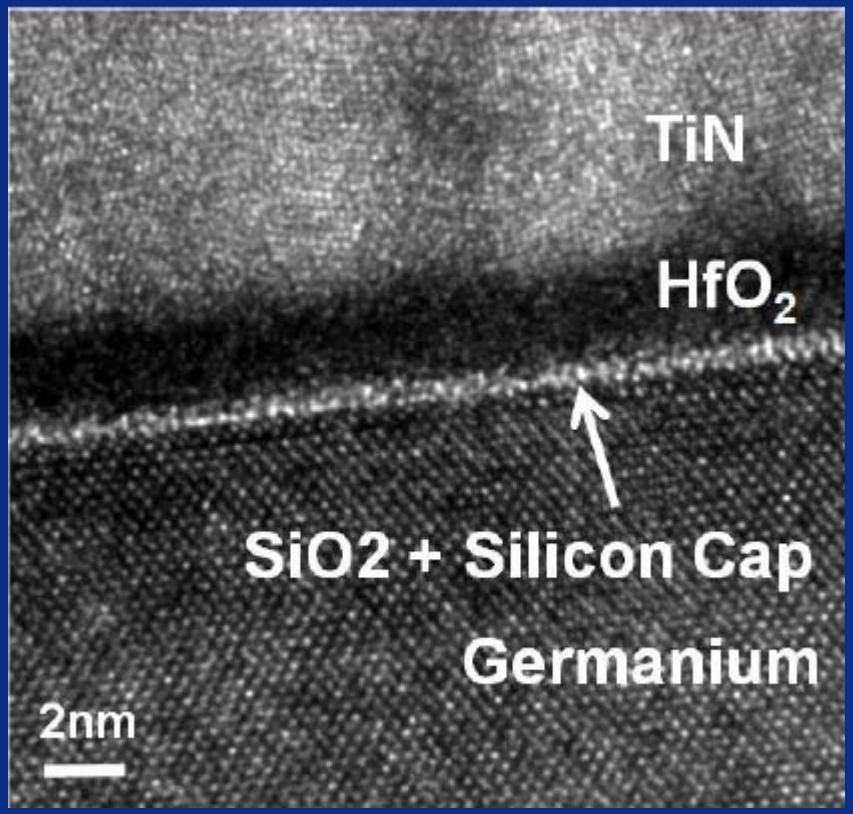
Strained Silicon

High k Metal gate

Tri-Gate

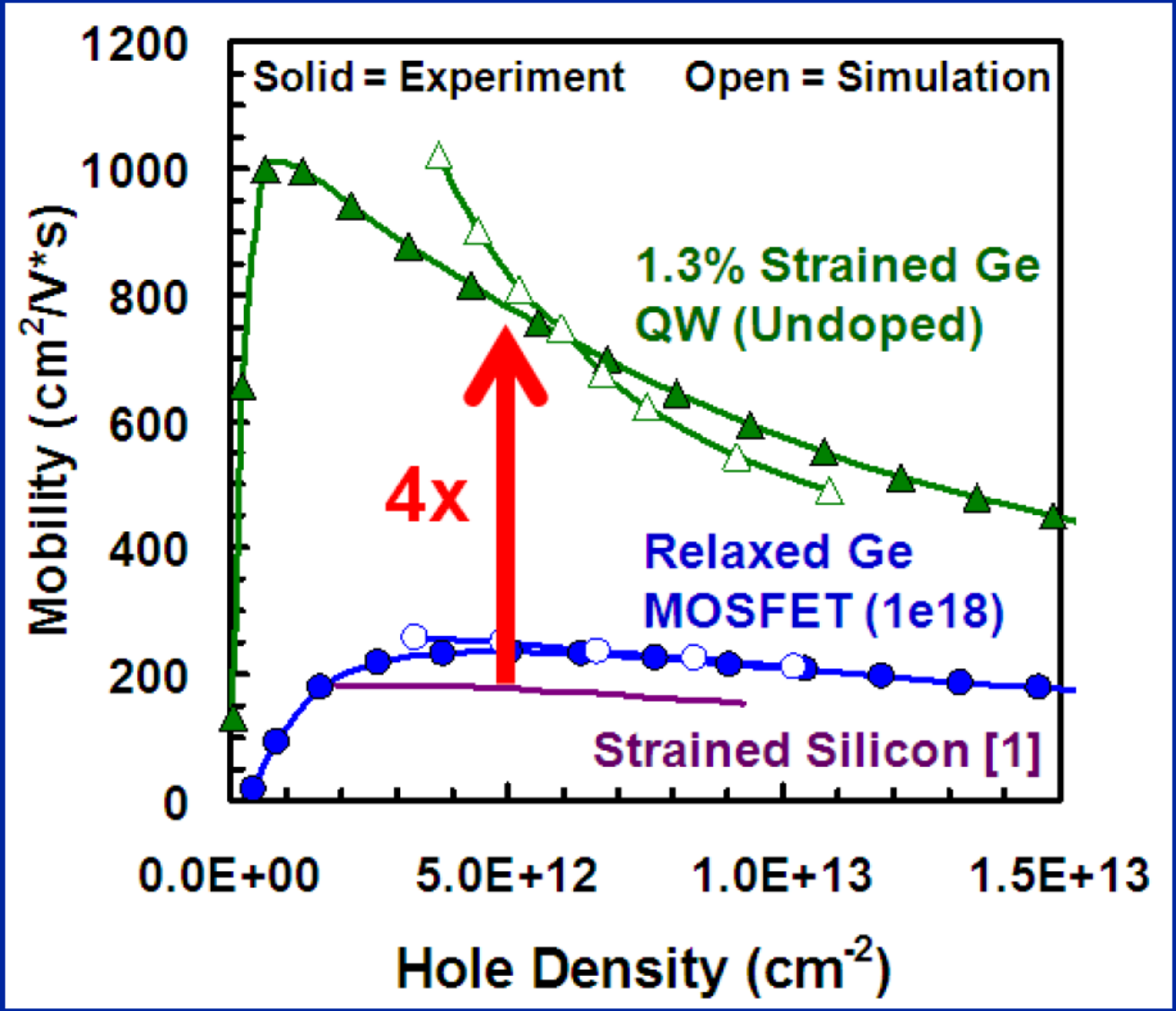
Ge P-Channel QWFET with HKMG





Intel, IEDM 2010

Ge QWFET Achieves 4x Gain in Mobility Compared to Strained Silicon

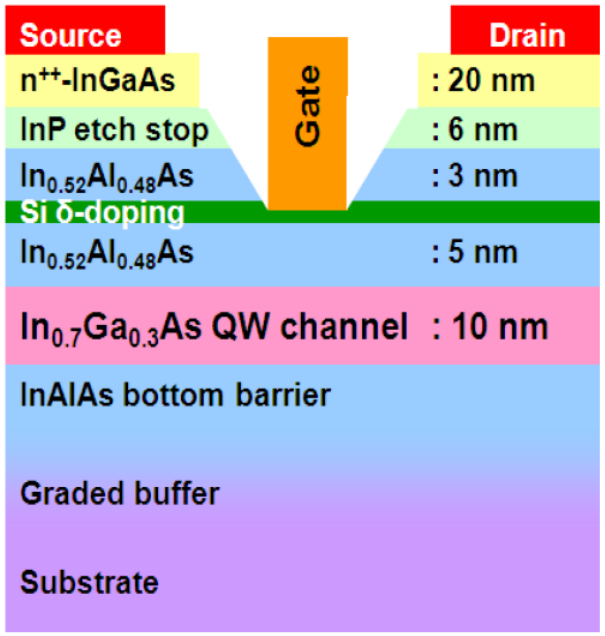


Intel, IEDM 2010

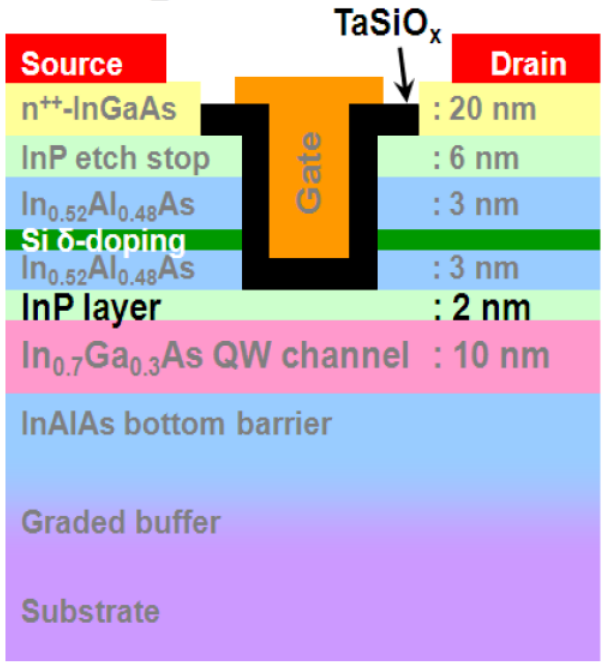
[1] P. Packan et al., *IEDM* (2008)

Evolution of InGaAs QWFETs

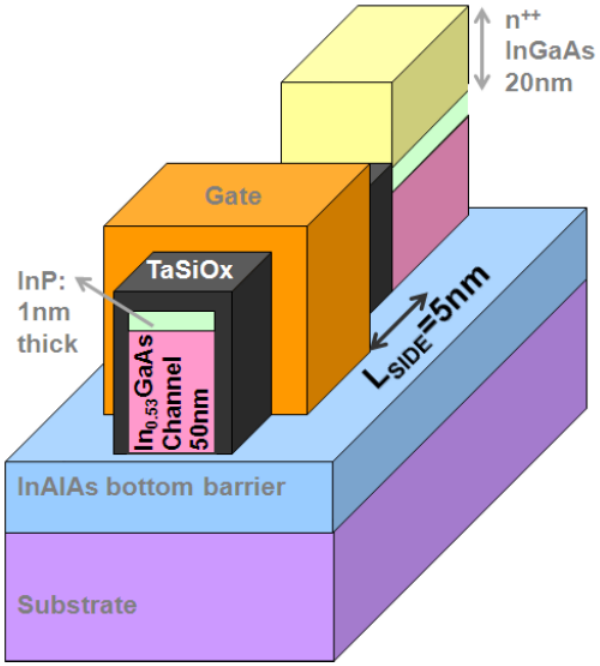
Planar Schottky-gate QWFET



Planar High-K/Metal gate QWFET



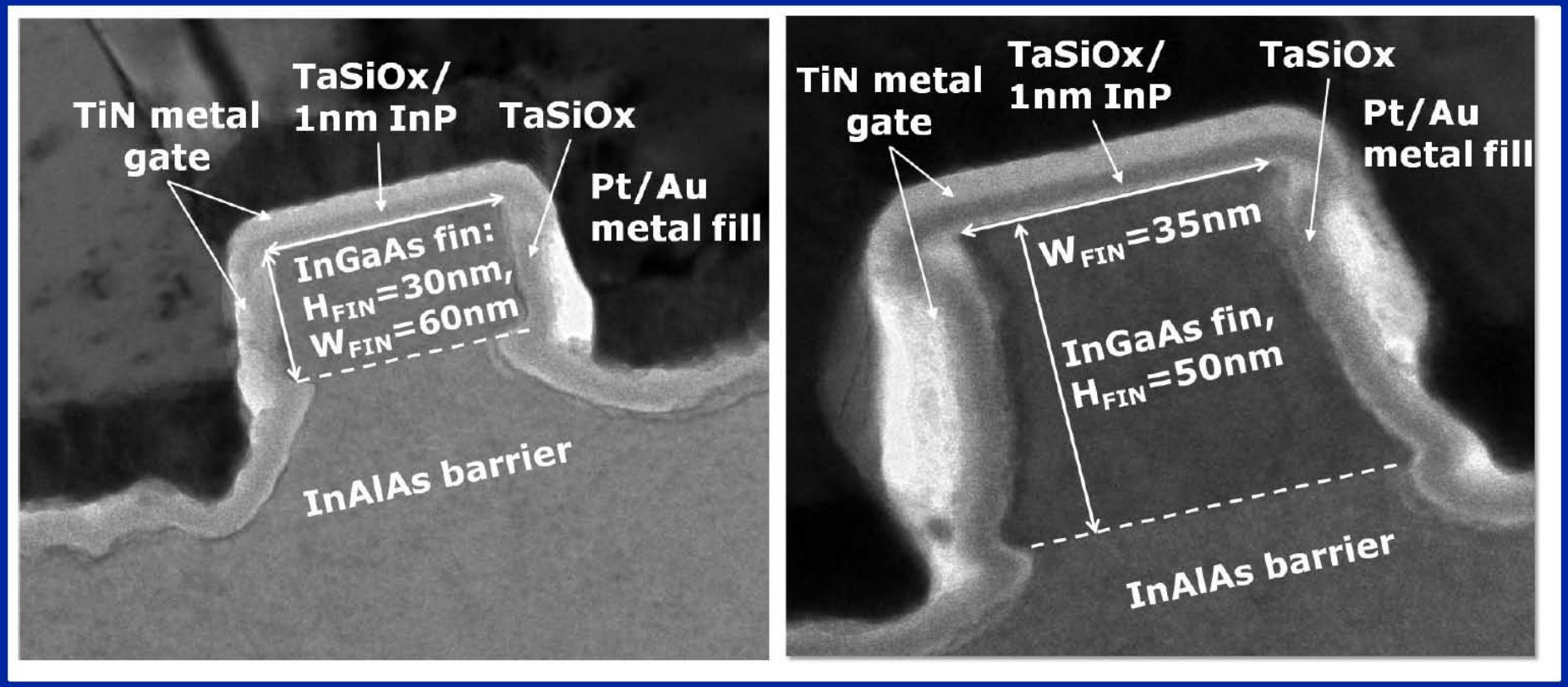
Non-planar, multi-gate QWFET



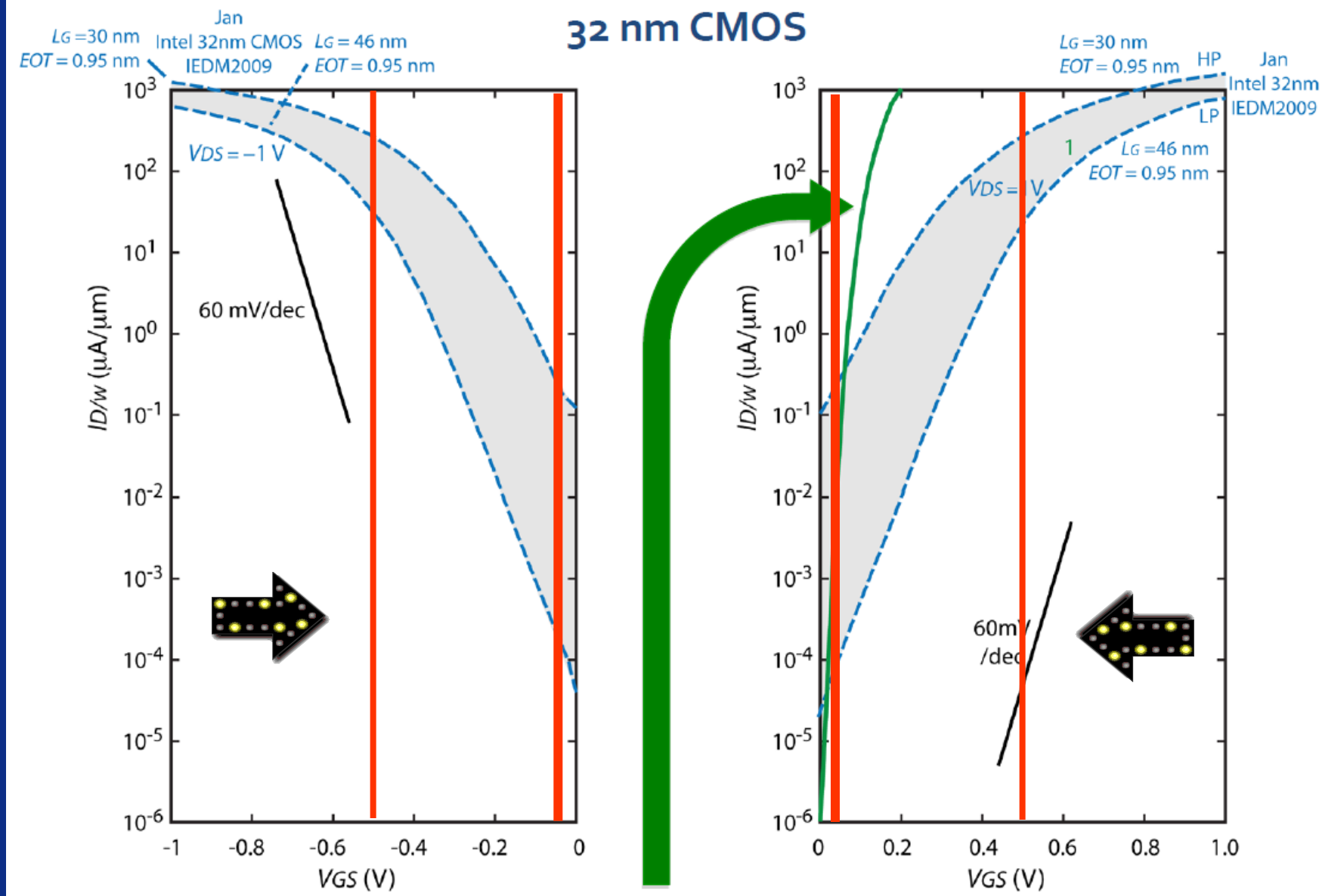
- Improved gate leakage and EOT/L_G scalability via High-K/Metal Gate
- Improved L_G scalability in non-planar, multi-gate architecture

Marko Radosavljevic, IEDM 2010

Completed Fabrication of Non-Planar, Multi-Gate InGaAs QWFETs

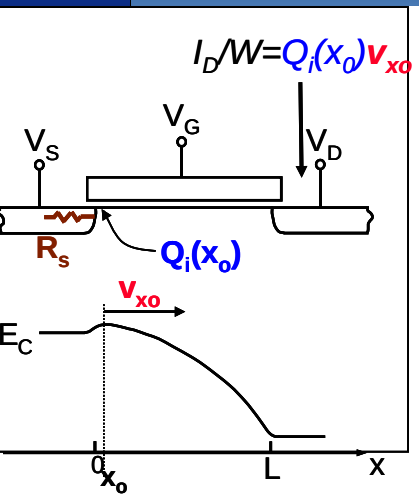


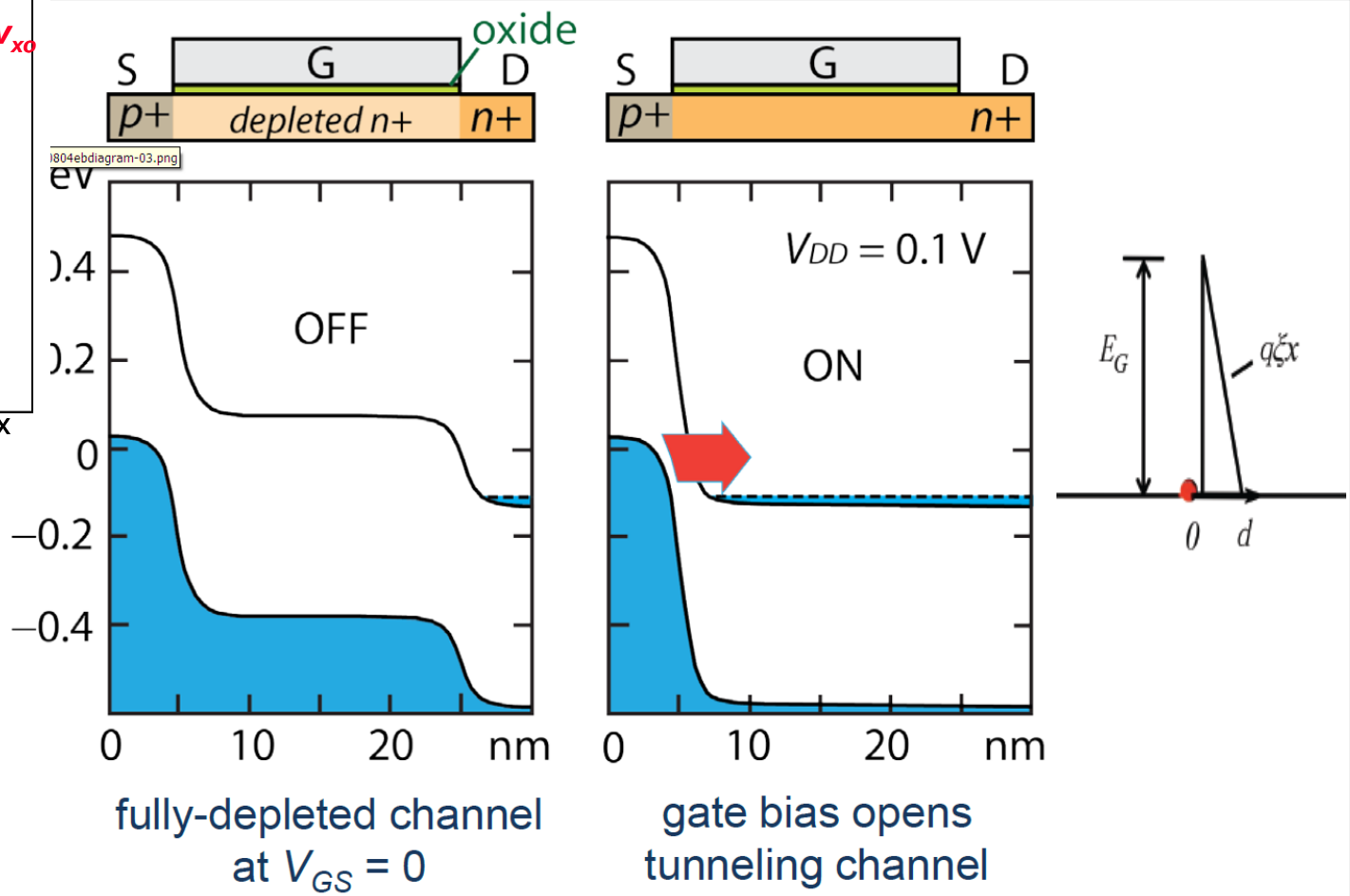
32 nm CMOS



Is this device possible?

Tunnel FET – physics of operation

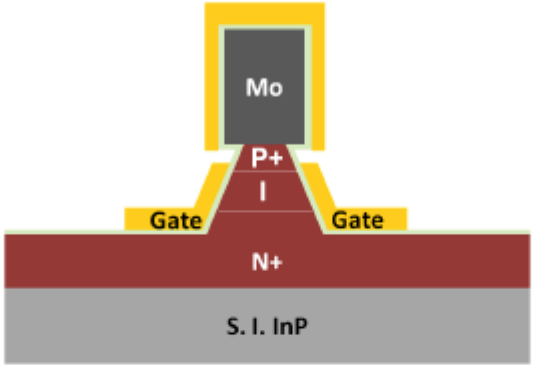




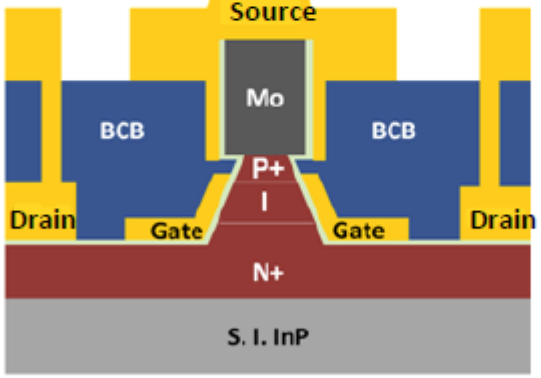
Attributes: (1) normally-off, (2) saturated I_{ON}, (3) low I_{OFF}, (4) low V_{DD}, (5) subthreshold swing <60 mV/decade, and (6) complementary

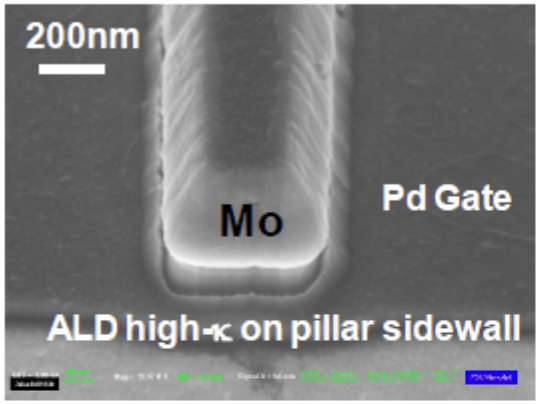
Vertical Nano-pillar TFET Process

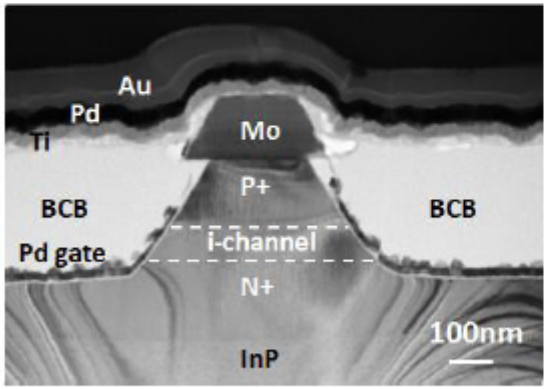
Self-aligned Gate and Drain separation



Planarization







Cross-section TEM of vertical nanopillar TFET

Key-steps

1. Define Cr/Ti Etch Mask
2. Dry etch Mo and $In_xGa_{1-x}As$
3. Wet etch undercut
4. Deposit high-k and self aligned vertical gate
5. Bottom contact
6. BCB planarization
7. Etch back
8. Top contact

Gate processing self aligned to top contact separation facilitates pillar thickness scaling
Mesa thickness scaled from 20um *(Mookerjea et al., IEDM 2009)* to 150nm (*Mohata et al., DRC 2011*)

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IEUVI Organization

IEUVI Board

Chair: Paolo Gargini ITRS
Organizer: Yumiko Takamori Intel
Member Organizations: Kurt Ronse, IMEC (EU), Stefan Wurm, Bryan Rice, SEMATECH (US), Ichiro Mori, Iwao Nishiyama, EIDEC (JP), Serge Tedesco, CEA / LETI (EU), Masashi Ogawa, EUVA (JP), CATRENE, ENIAC, AENEAS (EU)

IEUVI Technical Working Groups (TWG)

Source TWG

Chair: Dominic Ashworth (US) SEMATECH
Co-Chair:
Warren Montgomery (US) CNSE

Resist TWG

Chair: Karen Petrillo (US) SEMATECH / IBM
Co-Chairs:
Serge Tedesco (EU) CEA / LETI
Patrick Naulleau (US) LBNL

Mask Infrastructure & Manufacturing TWG

Chair: David Chan (US) SEMATECH
Co-Chairs:
Long He (US) SEMATECH / Intel
Markus Bender (EU) AMTC
Kazuya Ota (JP) Nikon
John Zimmerman (US) ASML
George KC Huang (TW) UMC

iEUVi Mask ITWG Update

October 2011

David Chan, Long He, Abbas Rastegar,

Frank Goodwin, Harry Kwon, Michael Goldstein

Mask TWG: Mission & Objective

Mission:

Ensure EUV Mask Infrastructure Readiness for:

- Pilot Line Production 2011 – 2012
- High Volume Manufacturing 2013 - 2016

Objectives:

- Identify Required Standards
- Coordinate industry-wide conversions
- Identify any gaps between current industry efforts and projected future needs
- Highlight gaps to member organizations and IEUVI Board for action

EUV Mask Standard Status

E152 EUV-pod standard revision is immediately needed.

- Among nearly ten updates, the two most important are additions of reticle purge ports, and safeguard features for positive identification of carrier or mask (RFID, info pad configuration).
- The yellow ballot was open for voting from 9/12 to 10/12.
- Review / adjudication will be on 10/26 in SEMI Fall Standard Meeting, Santa Clara, CA

P37 blank standard TF activity is low, but no urgent need.

(P38 was merged to P37 in last revision.)

- *Integrated mask reflectivity* is proposed, vs. reflectivity at mask level as currently defined.
- No consensus has been reached to move forward.

P48 fiducial mark standard implementation is at works between users and blank suppliers.

EUV Reticle Carrier Essential

EUV reticle carrier uses a *pod-in-pod* structure.

Masks transfer to vacuum with inner pod on

When outside of tools, masks are protected in complete sets of EUV carrier, not just inner pods.

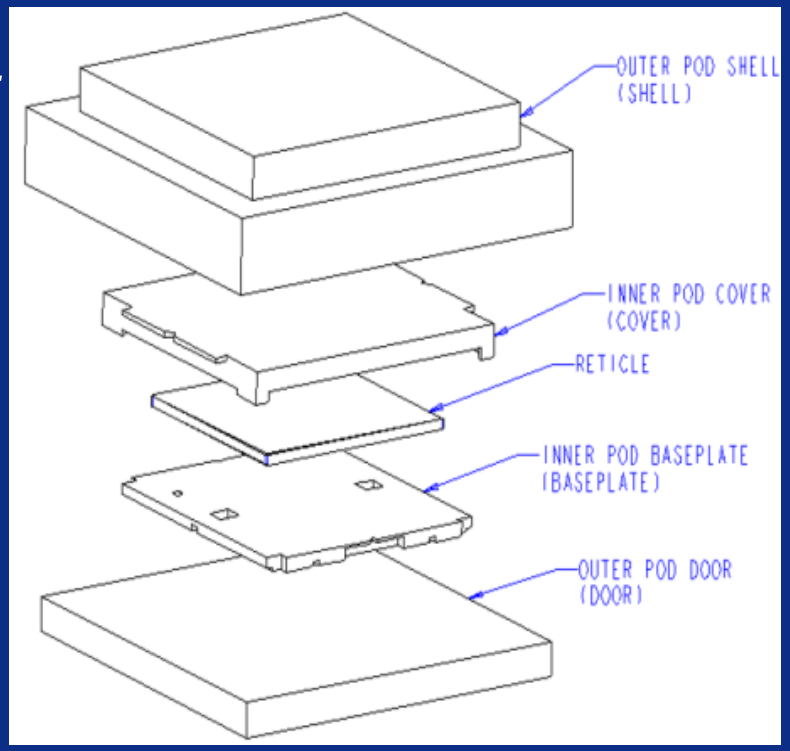
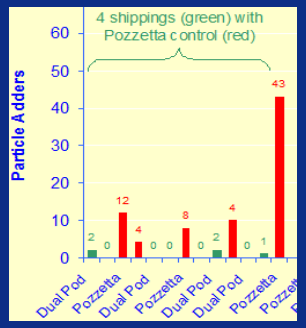
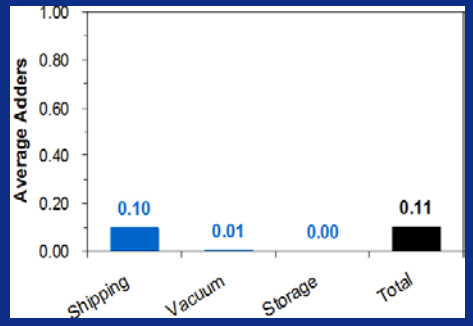
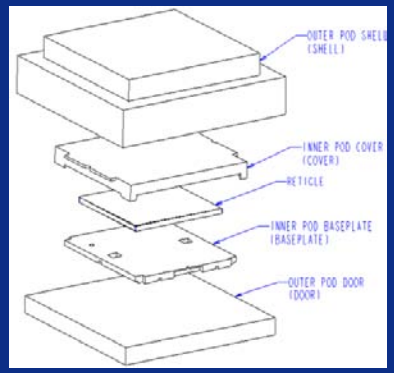


Figure 1. Concept of EUV reticle carrier

EUV Reticle Carrier Progress







There are still significant challenges!

Dual-pod concept demonstrated

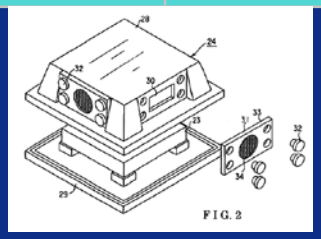
Performance capability demonstrated with sPod

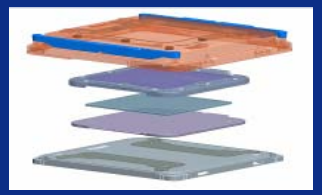
E152 EUV-pod standard established

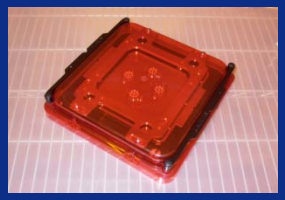
Implementation start

200?

2007		2008		2009		2010		2011	
H1	H2	H1	H2	H1	H2	H1	H2	H1	H2



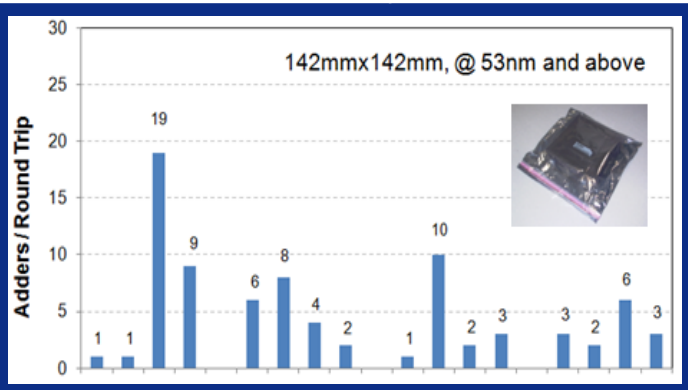




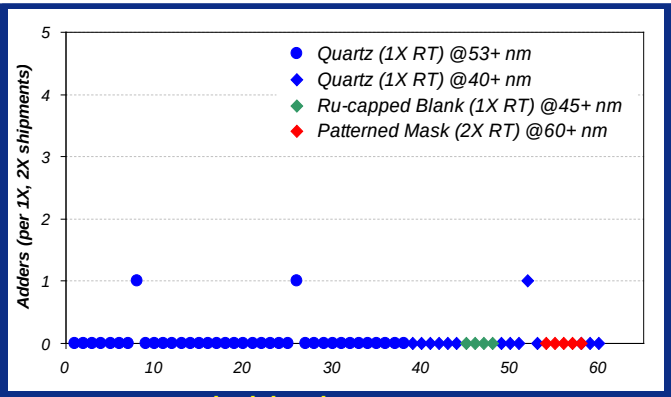
SEMATECH / Entegris outer-pod JDA for commercial availability of a-, n-, c-, and s-Pod.

Reticle Carrier Assessment: No Single Carrier Solution Exists Today from blank shops, mask shops to wafer Fabs.

Need	Carrier Type	SMT Assess. Risk	Comment
NXE3100 tools	aPod		Need more data to assess
Non-exposure tools (clean, inspection, etc.)	aPod, sPod	*L*	Require full tool compliance with E152 standards
Shipping	aPod	*M/H*	Palletized packaging, no data
	sPod	*L*	Require a *particle-free* transfer
	Clamp shell boxes	*M/H*	Require clean at wafer fab arrival
In-fab storage	aPod, sPod	*L/M*	Need data

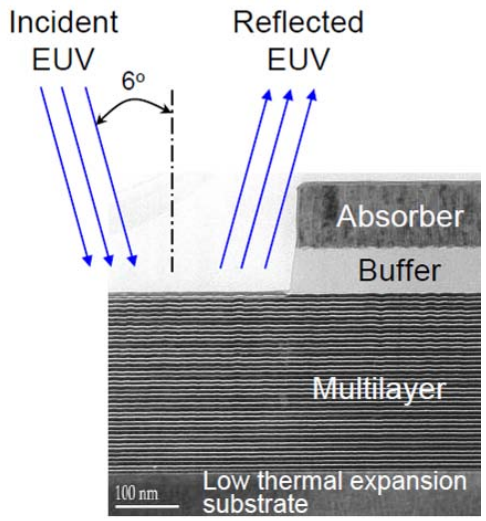


Typical shipping results with clamp shell compacts

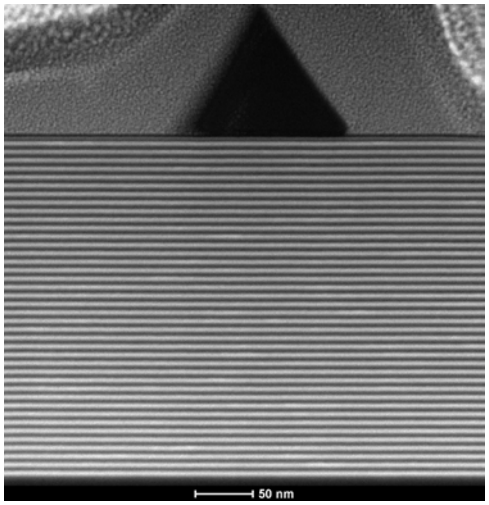


sPod shipping summary,

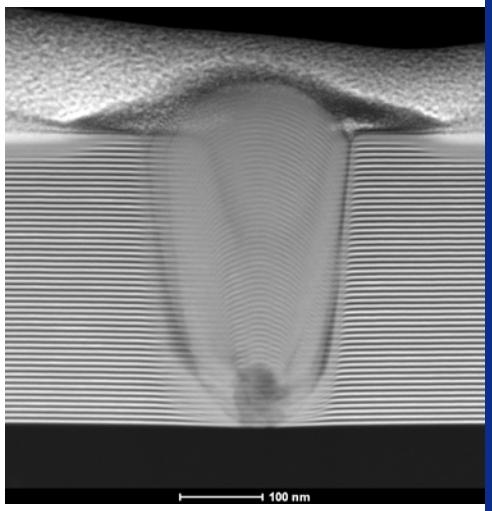
EUV Mask Blank Defect Types



TEM Courtesy: K. Nguyen, AMD



Amplitude defect



Phase defect

EUV masks are vulnerable to different types of defects

- Amplitude defects:
  - Surface particles/pits that generate contrast changes at the wafer
- Phase defects:
  - Bumps/pits at the substrate which become buried in or below the multilayer
  - Results in a phase change of the reflected wave.
  - Phase defects as small as 1 nm in height or depth can result in printable defect

EUV Mask Blank Defects @ 50+nm

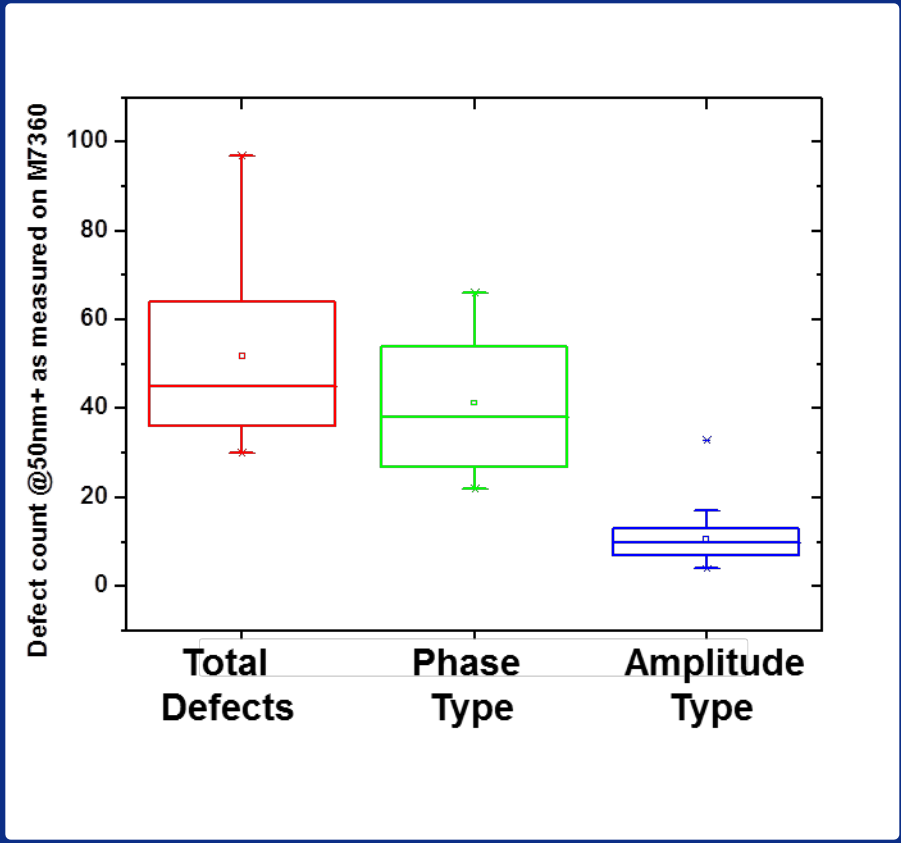
At 50nm inspection sensitivity

Phase type defects

- Substrate and handling
- Account for 70-80% of total defects in a mask blank

Amplitude defects

- ML Deposition
- Typically in single digits



Defect Density Trends

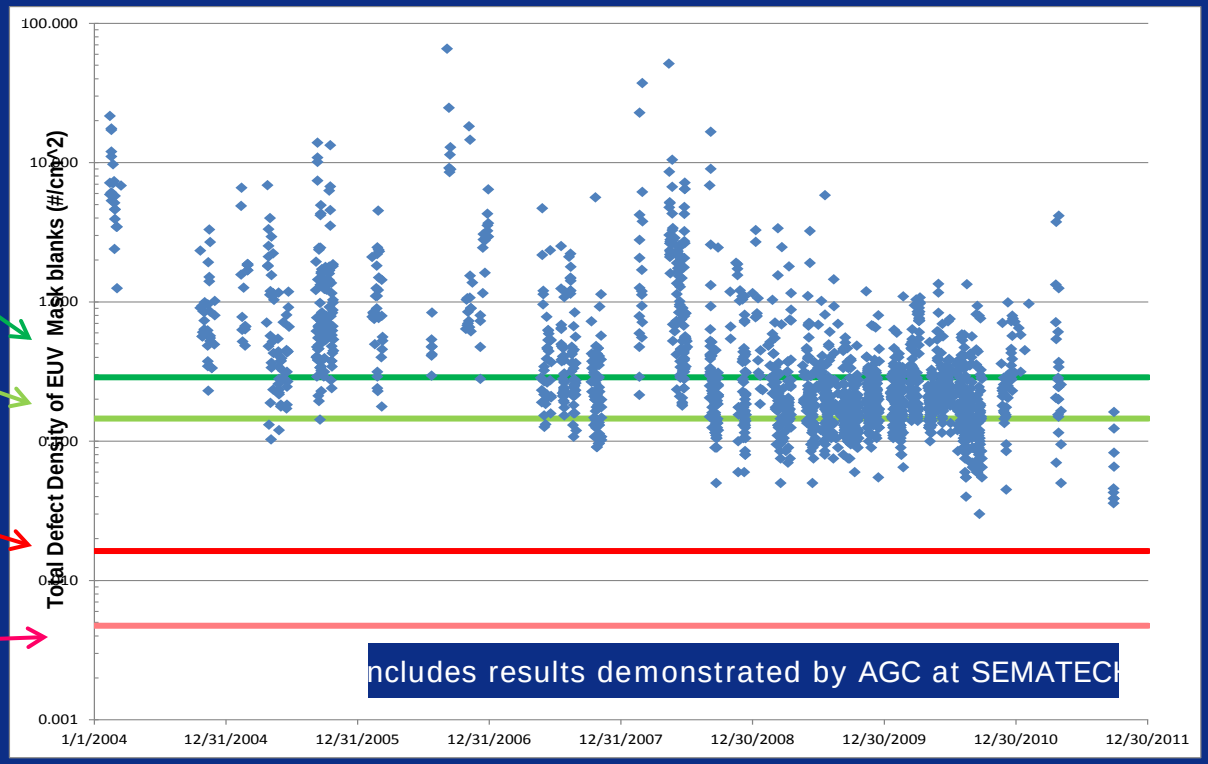
AGC

2013 Memory Need

2014 Memory Need

2013 Logic Need

2014 Logic Need



- Memory requirements
  - Overall defect counts are meeting requirements
  - However, large size “Killer” defects still present and remain a concern for mask yield
- Logic requirements for 2013 not being met
  - Current trend over the last 2 years looks positive to achieving these defect levels

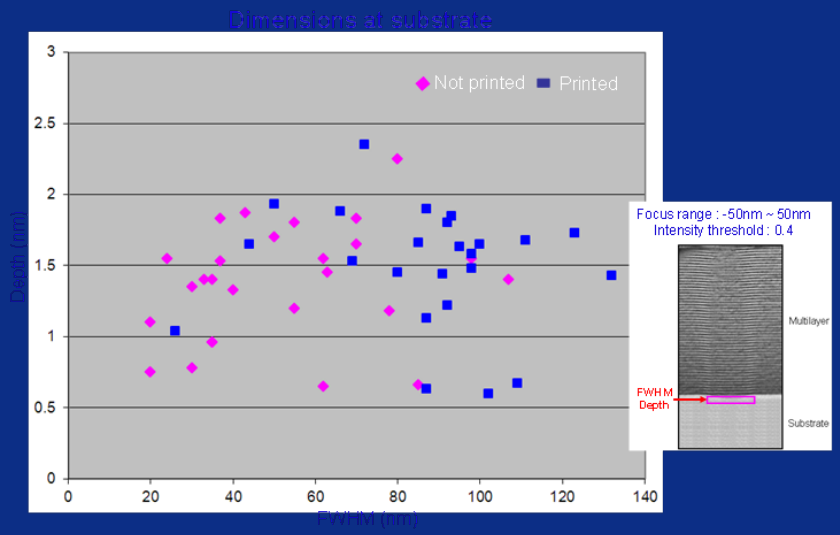
Pit Defect Printability

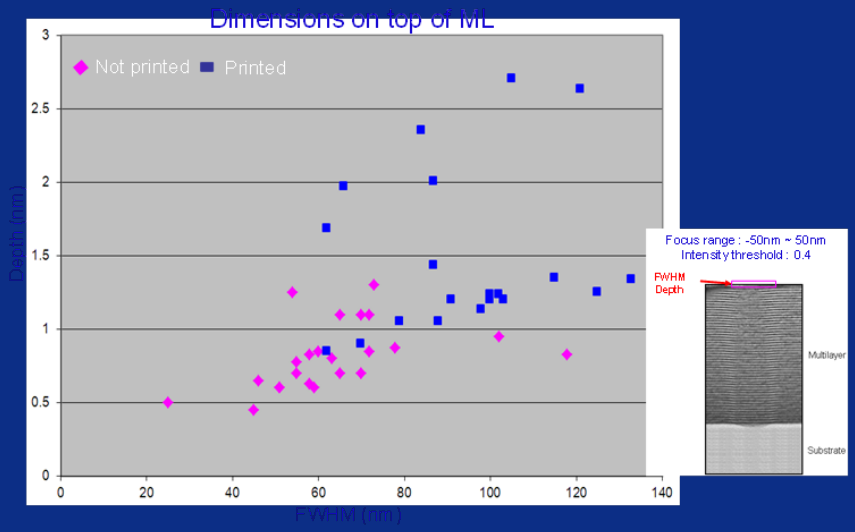
Programed Defect Mask Results

- Defects located at the substrate
  - Most defects with < 70 nm FWHM and < 1.5 nm depth will not print
- Defects measured at top of ML
  - Most defects with < 60 nm FWHM and < 0.8 nm depth will not print

Physical dimension is not the sole indicator of printability

- Neither data set provides a clear partitioning of what type of defect will print





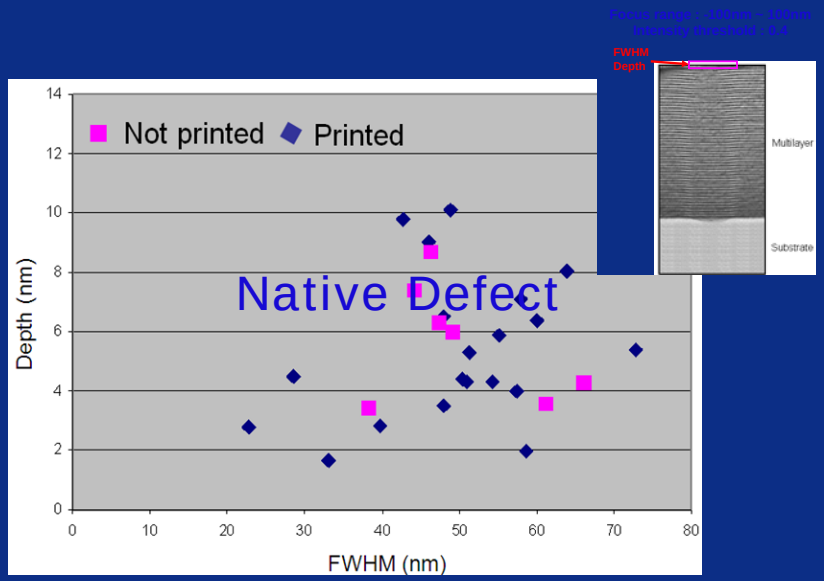
Native Defect vs. Program Defect

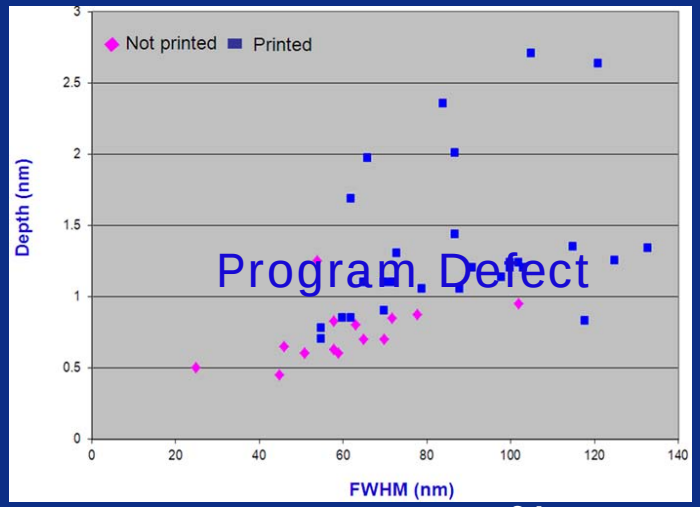
The printability of native and program pit-type defects are different

- Program defects are more likely to print than native defects.
- Native defect data shows that some larger defect will not print

Difference most likely due to how the defects are decorated during ML coating

- Film growth over programed defects does not mimic growth over native defects





EUV Mask Cleaning Progress

Damage free LTEM substrate cleaning processes were developed with PRE of 98% for particles >=40 nm (SiO_2 Equivalent)

Improved the lifetime of EUV mask blanks by improving their durability to the cleaning processes up to 50 cleaning cycles

- Determined interaction between VUV (λ=172 nm) and Ru cap and sulfuric acid is the main mechanism of EUV reflectivity loss
- Improved cleaning processes to reduce EUV reflectivity loss and megasonic damage

EUV mask cleaning at 16nm HP and beyond requires innovative cleaning technologies.

- SEMATECH initiated innovative cleaning technology development programs
  - Gigasonic cleaning
  - Laser nozzle technology
  - Liquid filtration and membrane technology

Mask Metrology Tool Update

October 2011

Michael Goldstein,

David Chan

Infrastructure Enablement

EMI Projects and Activities

- AIMS: SEMATECH / Zeiss program running. First tool 2014
- Blank Inspection:
  - Mid-2011: KLA 630
  - 2013: EIDEC/Lasertec actinic tool
- Actinic Patterned Mask Inspection: KT 7xx in 2015
- eBeam Patterned Mask Inspection: multiple efforts with tools in 2013-2014
- High brightness metrology source is in process
- Additional programs are in planning stage

Advanced mask metrology project

- The AIT*5 at LBNL for SEMATECH research and member access
  - *Actinic Inspection Tool

High Brightness Metrology Source

Impact of a brighter metrology light source

- ROI scales with ~ throughput x availability/cost.
- Throughput increases with brightness.
- Focus on improving the availability/cost ratio.

Light source should be applicable to AIMS and inspection tools.

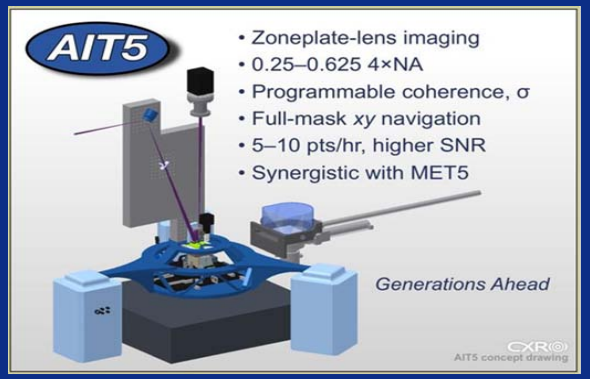
EMI / iEUVi metrology source activities in process

- Completed Request for Information (RFI) and site visits.
- Consolidated metrology source spec is being developed
- EMI project path is being reviewed.

SEMATECH High-NA Actinic Reticle Review Project (SHARP) at LBNL

Next generation AIMS

- Kenneth A. Goldberg, et. al., "Developing a New State of the Art EUV Mask Imaging Research Tool at Berkeley"



Improved optics and illumination.

- Wintz, et al., SPIE 7636, 76362L-1, (2010).

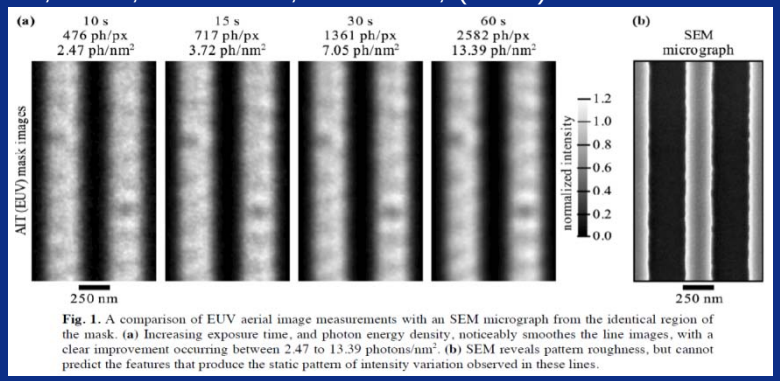
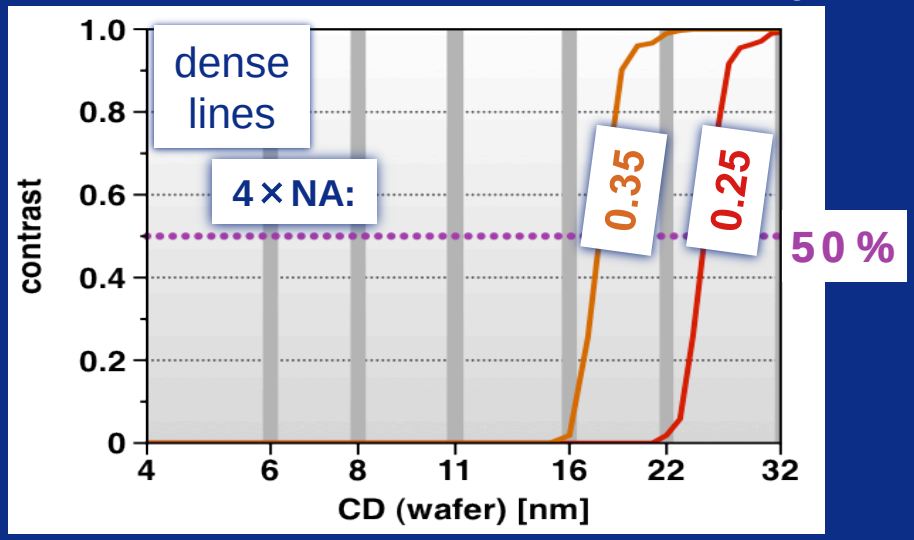
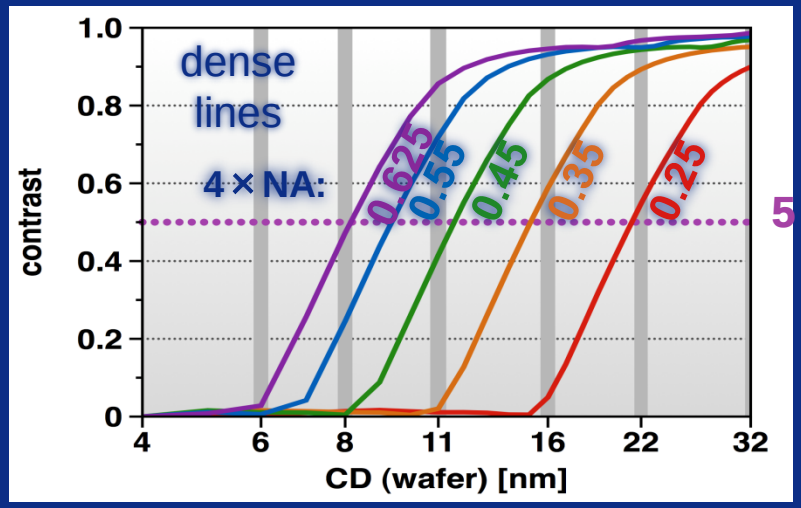


Fig. 1. A comparison of EUV aerial image measurements with an SEM micrograph from the identical region of the mask. **(a)** Increasing exposure time, and photon energy density, noticeably smoothes the line images, with a clear improvement occurring between 2.47 to 13.39 photons/nm². **(b)** SEM reveals pattern roughness, but cannot predict the features that produce the static pattern of intensity variation observed in these lines.

- Kenneth A. Goldberg, et al. SPIE Photomask, 2011





At σ ≈ 0.2, Currently AIT sees ≥ 16nm

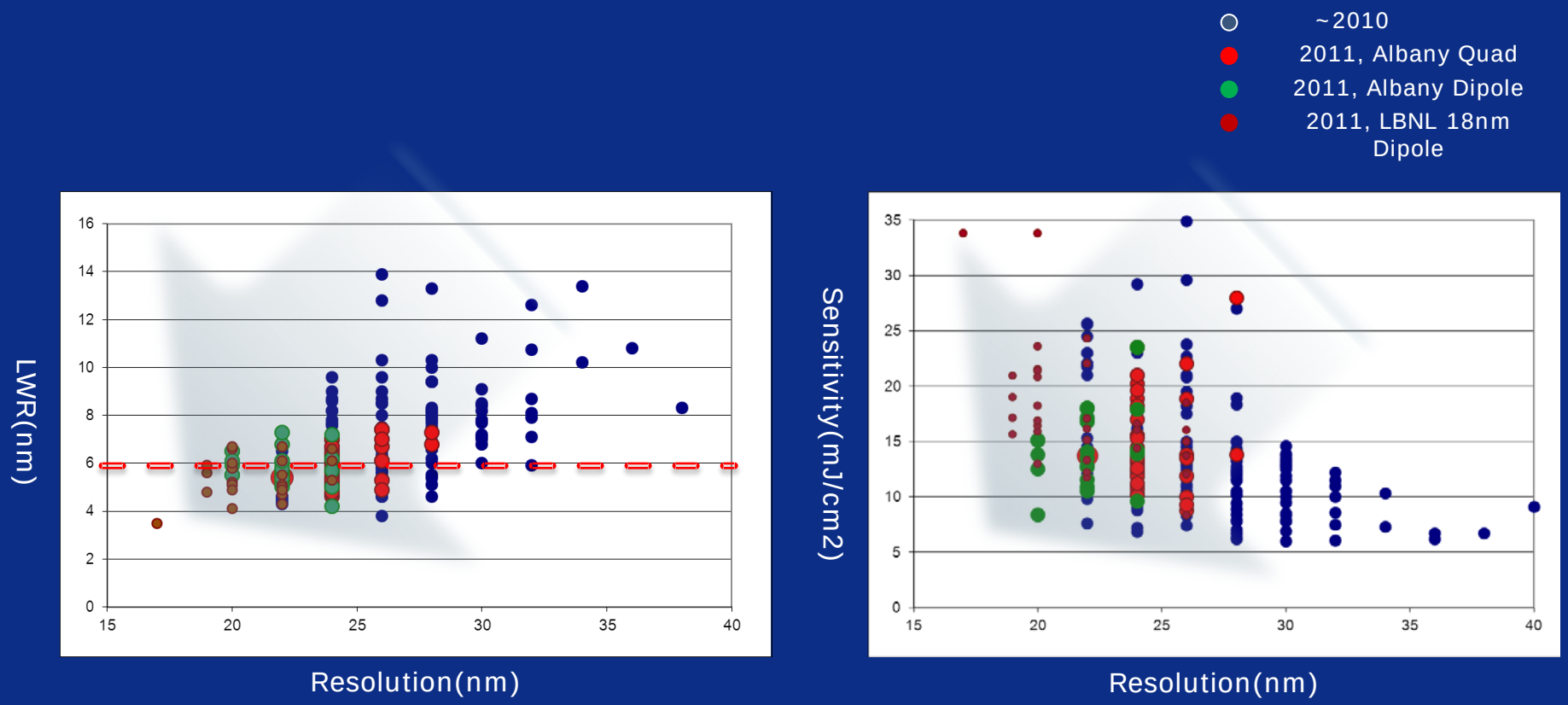
At σ = 0.8, SHARP will see > 6 nm

Progress in Resist Technology

Karen Petrillo

Resist ITWG Chair

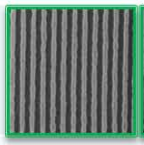
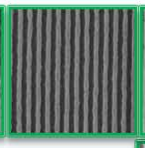
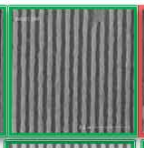
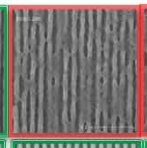
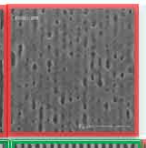
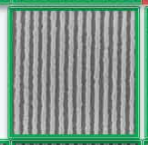
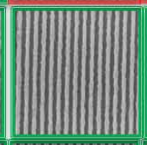
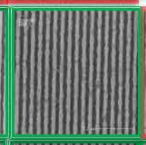
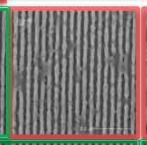
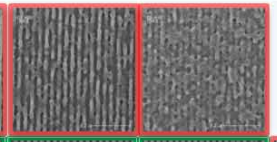
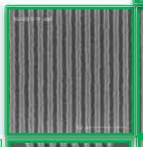
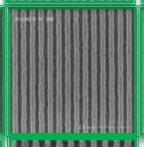
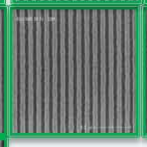
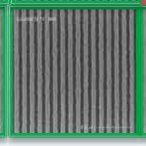
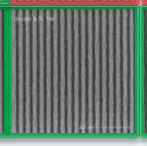
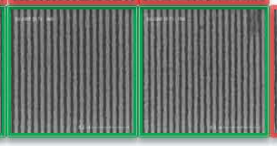
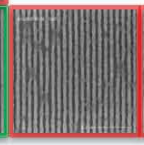
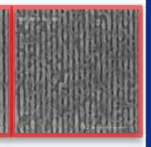
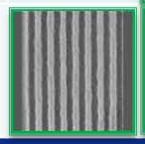
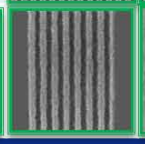
Current performance status



Resolution, LWR and sensitivity are improved but slowly.

Current performance status

- Best materials

Exposure Tool	Resist RLS	28nm	26nm	24nm	22nm	20nm	19nm	18nm	17nm	16nm	15nm
Quad @Albany MET	B1 R 24nm L 5.0nm S 10.3mJ/cm2										
Dipole @Albany MET	D1 R 20nm L 5.5nm S 12.5mJ/cm2										
18nm dipole @LBNL	D2 R 17nm L 3.5nm S 33.8mJ/cm2									
AD1 @Albany	B2 R 25nm L 4.9nm S 28.3mJ/cm2										

Resist Outgas Testing

CNSE ROX outgas testing tool has been ASML certified for NXE 3100 and 3300 tool platforms

- The tool is able to test ~40 samples per quarter now and with a dedicated XPS will be able to do ~120 samples per quarter starting Q2/2012

SEMATECH is installing a high volume outgassing tool in Q1/12

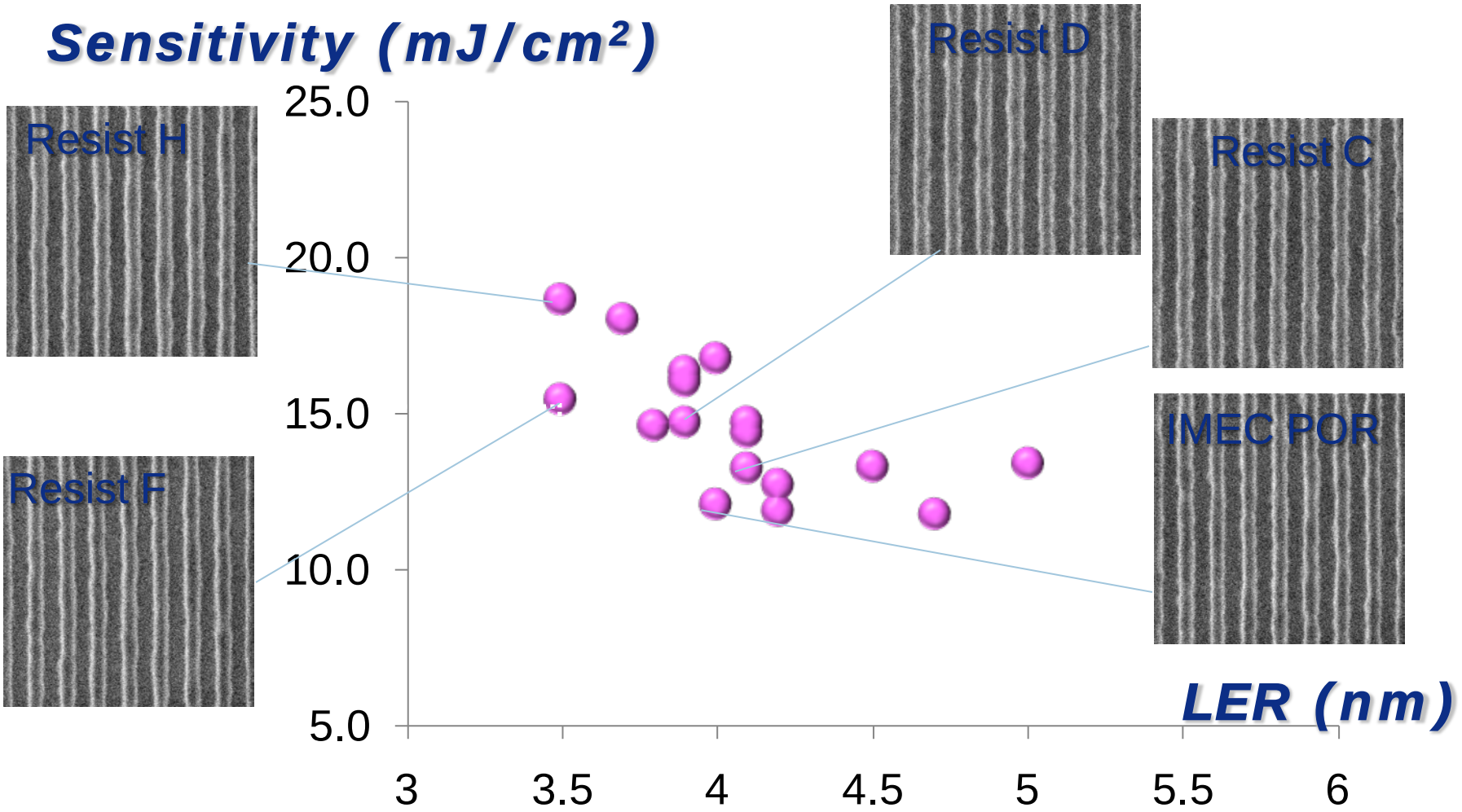
- This will provide an additional resist material certification capability mid-2012 of ~1000 samples per year
- The will meet the industry outgassing need for EUV pilot line introduction and HVM ramp-up

ASPIRE
INVENT
ACHIEVE

imec

EUV resist performance

EUV resist performance on ADT 28nm LS , NA=0.25, σ=0.5



Meeting the LER target is challenging

EUV resist Performance @ ADT

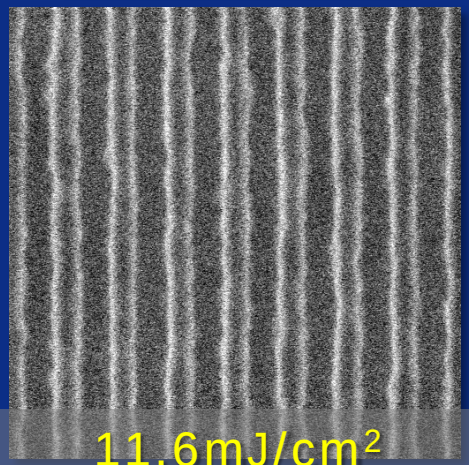
imec POR resist, 50nm thickness on std uL

28nm L/S

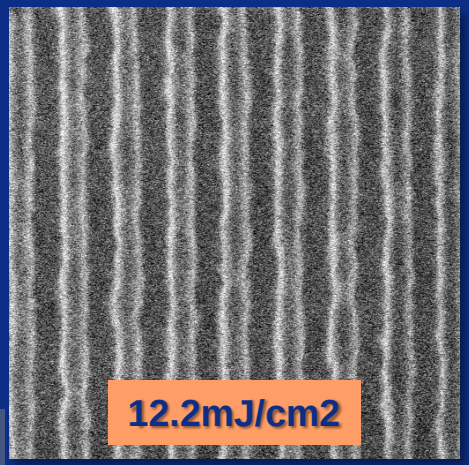
27nm L/S

26nm L/S

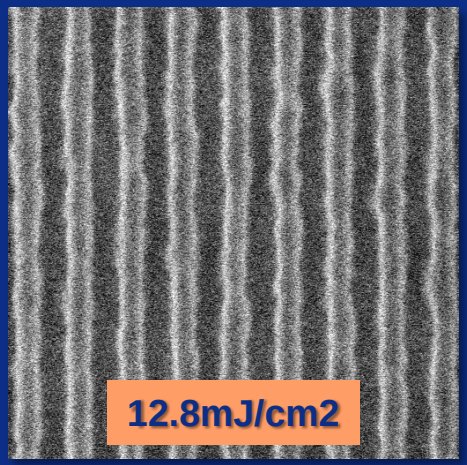
25nm L/S



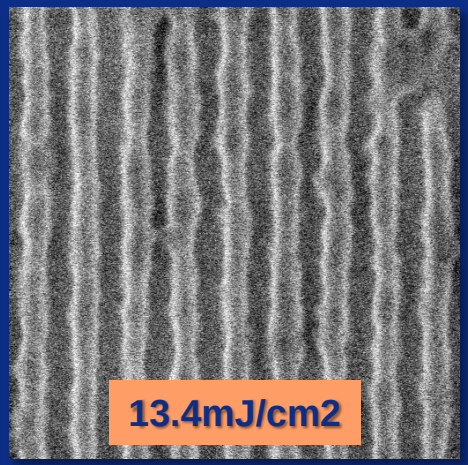
11.6mJ/cm^2
LER = 4.0nm (3σ)



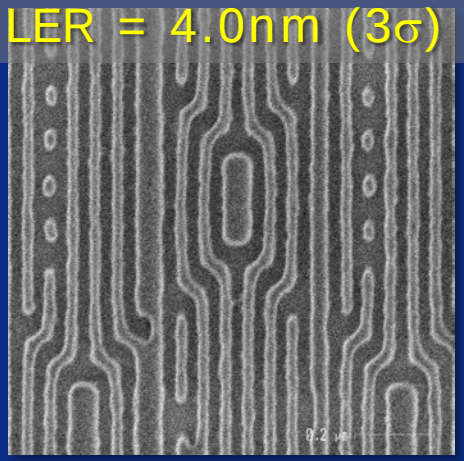
12.2mJ/cm2



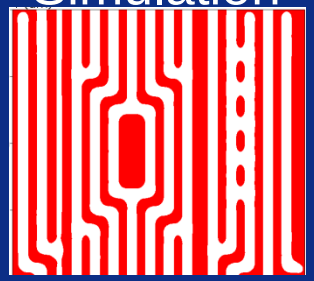
12.8mJ/cm2



13.4mJ/cm2

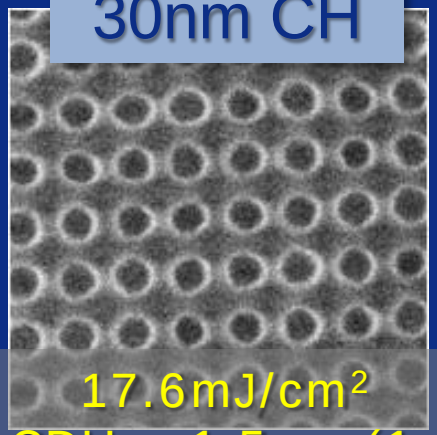


Simulation



0.25NA, 0.5sigma

30nm CH

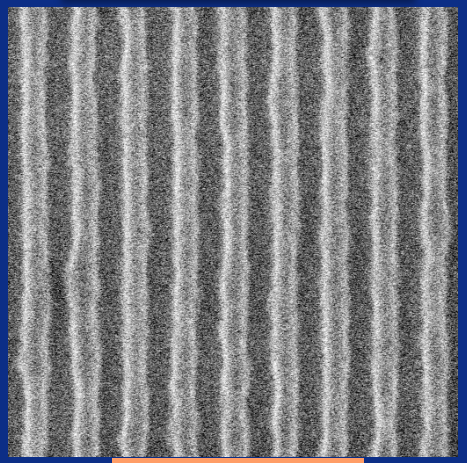


17.6mJ/cm^2
LCDU = 1.5nm (1σ)

EUV resist performance on NXE3100

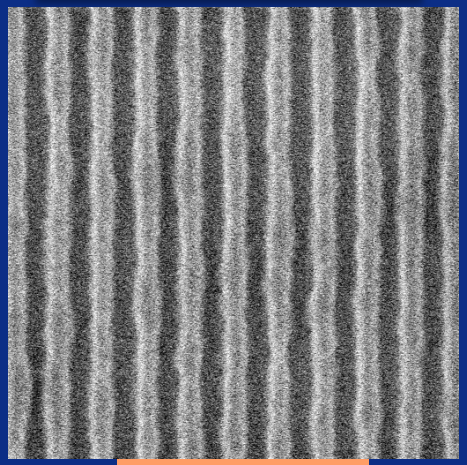
dipole illumination, 40nm imec POR Resist on uL

25nm LS



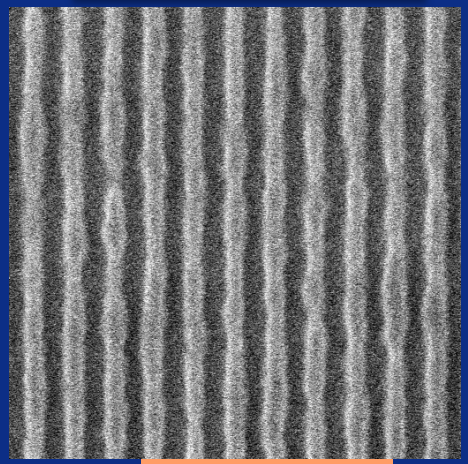
12.5mJ/cm2
4.0nm LER

22nm LS



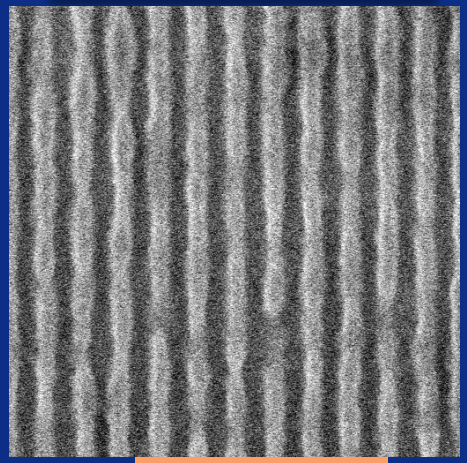
13.4mJ/cm2
4.7nm LER

20nm LS

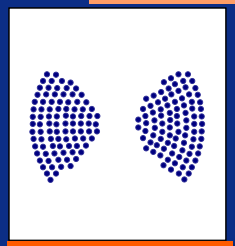


14.6mJ/cm2

19nm LS



15.2mJ/cm2



60°Dipole
σ0.81/0.43

0.25NA

Sub-22nm resolution demonstrated by the using dipole illumination

ASML

EIDEC

Hiroki Miyai

T.Yamane

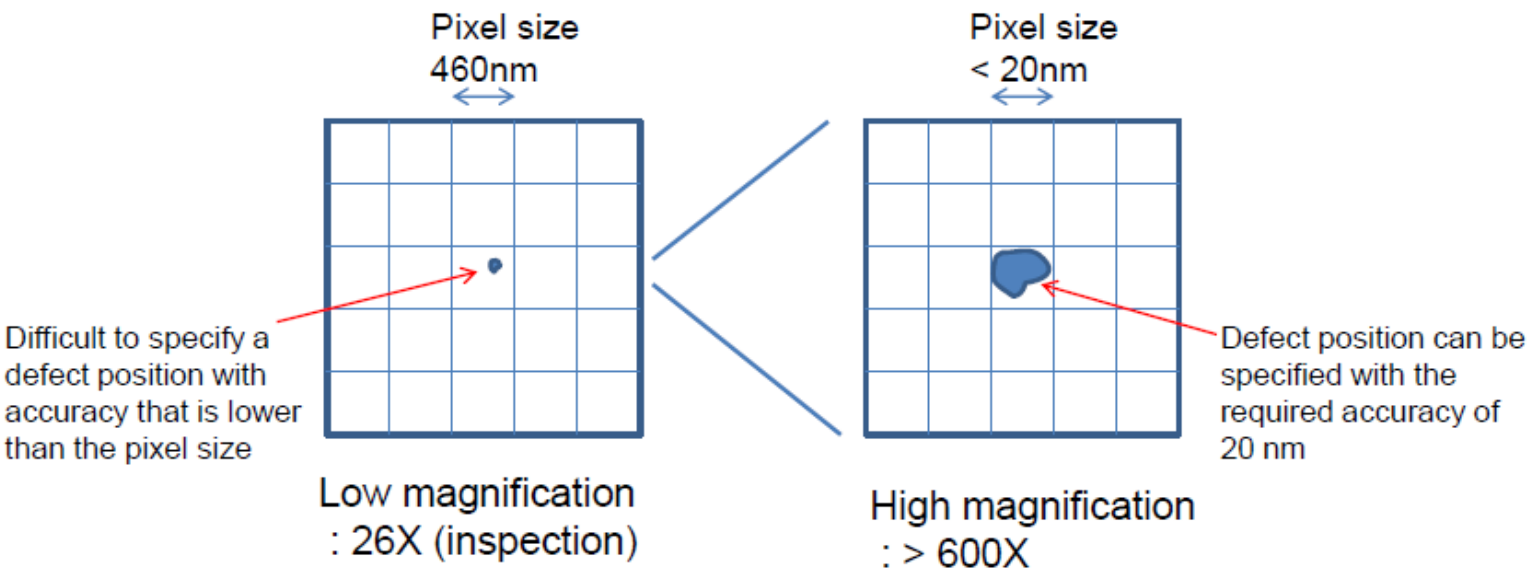
Lasertec

Development of Lasertec tool

Specification of the defect coordinate accuracy

- The ABI tool requires the defect coordinate accuracy of 20 nm for the defect mitigation of blanks.

  → The resolution limit needs to be smaller than the pixel size.

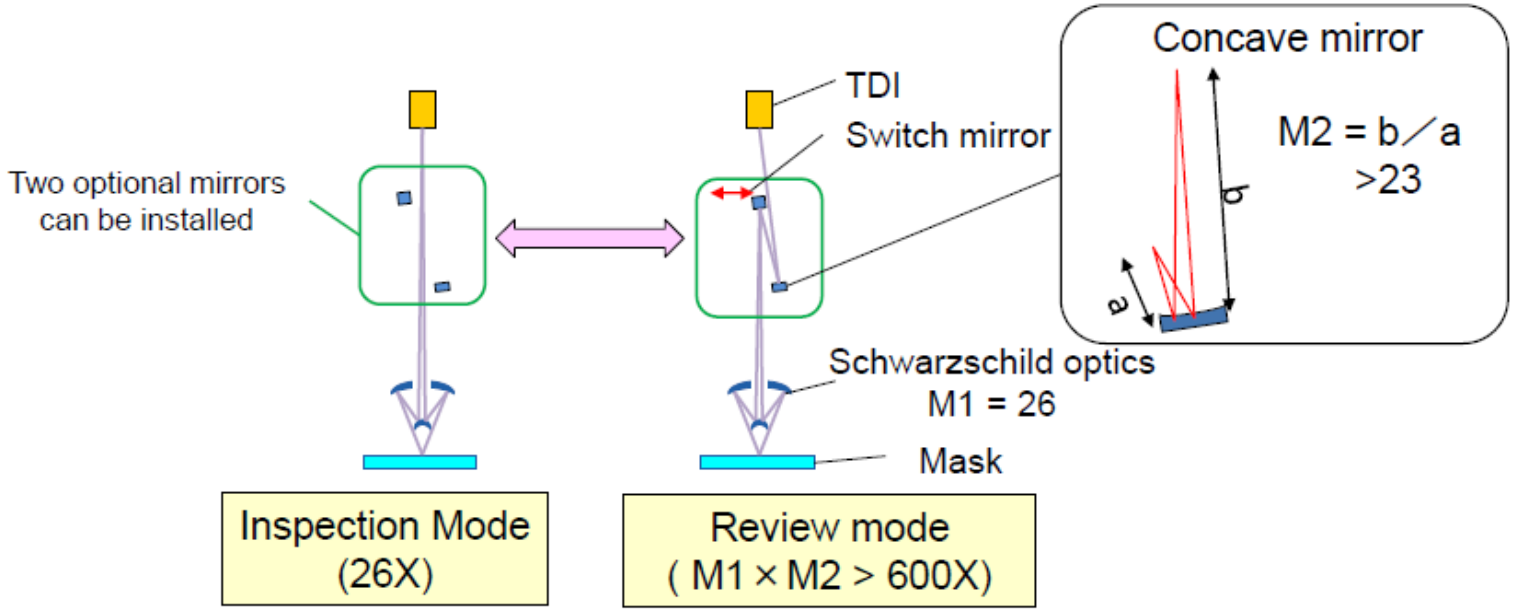


The relationship between the pixel size and the defect size

Development of Lasertec tool

High magnification review optics

- The ABI tool will perform defect position measurement of 20 nm.
  - -- For inspection, the 26X Schwarzschild optics is used prioritizing the throughput.
  - -- For review, a switch mirror is inserted into the optical path and observation is performed under the high magnification of > 600X.
  - -- Defect position is accurately measured by referencing the fiducial mark.



Improvement of MIRAI tool performance

Modifying the noise reduction algorithm, the detection probability for 1.2 nm-high and 40 nm-wide programmed defect increased from 95% to 99%

Top	Height	1.6	1.6	1.6	1.6	1.4	1.4	1.3	1.2	**1.2**	**1.0**
	Width	200	150	120	100	82	75	64	56	**40**	**36**
Bottom	Height	1.6	1.6	1.6	1.6	1.6	1.4	1.4	1.6	**1.4**	**1.4**
	Width	200	150	120	100	80	78	63	64	**50**	**41**

Defect size [nm]

- ◆Mask blank scan speed is 3 mm/s
- ◆Threshold for no false detection at full area of mask

T. Yamane et al., Oct. 19, 2011 EUVL symposium

Submissions to International Conferences

2011 International Symposium on Extreme Ultraviolet Lithography,
Oct. 17-19, 2011 (Miami, USA)

T. Amano et al., "Phase defect detection and analysis using actinic blank inspection tool and TEM", (poster)

T. Yamane et al., "Defect sensitivity improvement of actinic blank inspection", (oral)

H. Miyai et al., "EUV Actinic Blank Inspection tool development", (oral), (Collaborative work with Lasertec)

T. Amano et al., "EUV mask pattern inspection using EB projection optics" (poster)

J. J. Santillan et al., "In situ dissolution analysis of EUV resists: Ultrathin resists", (poster)

MNC 2011, 24th International Microprocesses and Nanotechnology Conference,
Oct. 24-27, 2011 (Kyoto, Japan)

T. Harada et al., "Micro Coherent EUV Scatterometry Microscope for a Defect Characterization on an EUV Mask" (poster) (Collaborative work with University of Hyogo.)

J. J. Santillan et al., "In situ Dissolution Analysis of Ultrathin EUV resists" (oral)

Joint IEUVI and EMI Source Technical Working Group (TWG)

Michael Goldstein,

David Chan

SEMATECH

Introduction

Light source improvements are needed for all EUV metrology tools.

- AIMS™ EUV tools.
- Actinic mask blank inspection tools.
- Actinic pattern mask inspection tools.

A first draft consensus specification has been created for metrology light sources with input from

- KLA Tencor,
- Lasertec, and
- Zeiss.

If funded in Q1'2012, it is possible to develop a prototype metrology light source in time for supplier evaluations.

Brightness Impact (in light limited conditions)

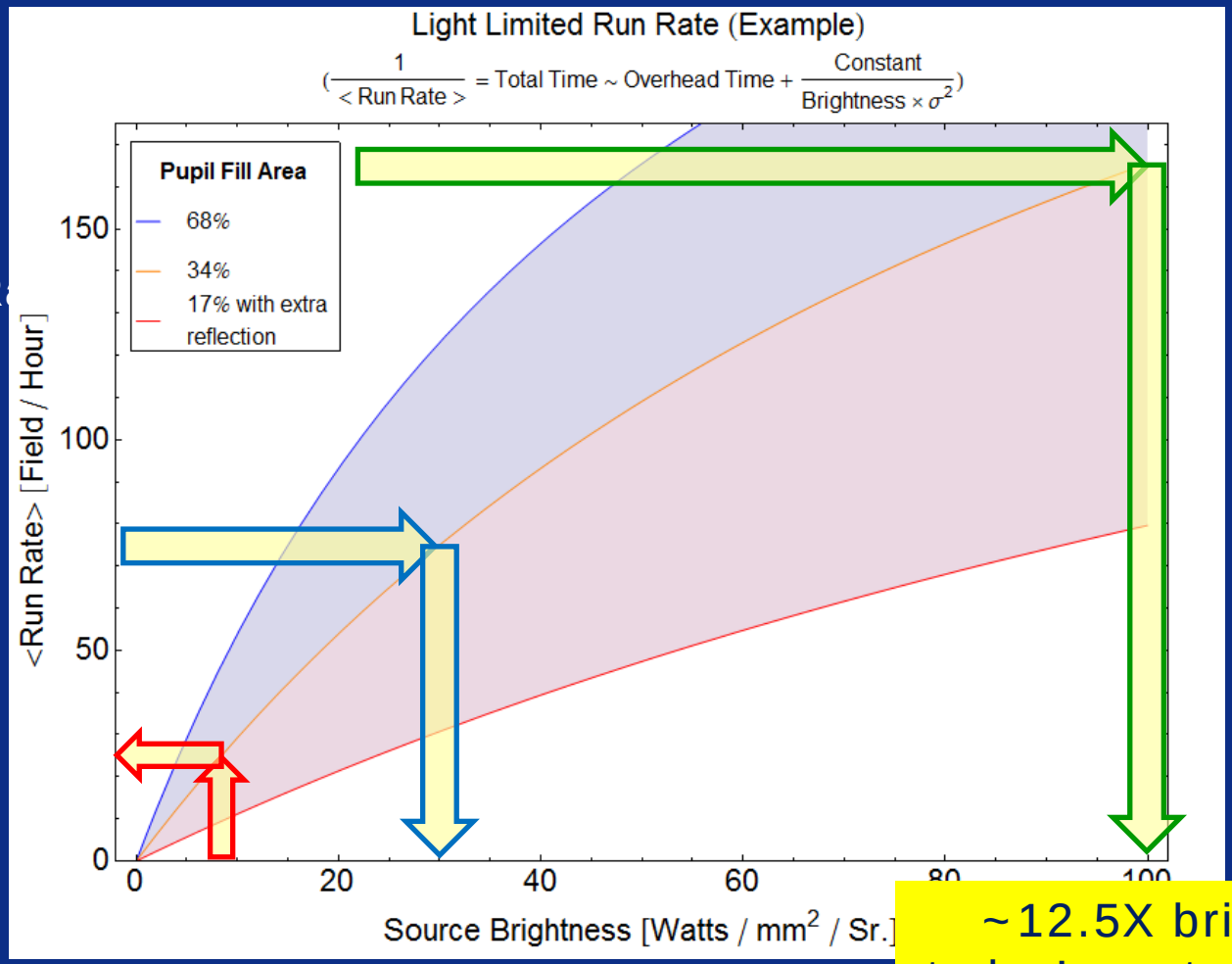
Why metrology source brightness counts in light limited run rate:

This is what we want. ⇨

<Run R

This is the abs. min need. ⇨

This is where we are today!



~12.5X brighter than today's metrology source.

Brightness

First Draft Consensus Specification

Key Specifications

- Schedule: Q3'2014
- Brightness: 40 → 100
- Etendue: By tool type.
- Pos./Size Instability: ≤3%
- Cleanliness: 100%

Some specs are still in review, in some trade-offs might be possible.

- Inhomogeneity
- Temporal Instability
- …

!	Specification	Requirement	Status
	HVM Prototype Available	Q3'2014	Consensus
	Wavelength [nm]	13.5	Consensus
	Repetition Rate [KHz]	≥ 10	Consensus
	Pulse Duration [nS, FWHM]	≥ 10	Consensus
	Continuous Operation, $\tau \geq 100$hrs	100%	In review
!	In-Band Brightness [W/mm^2/Sr] Pre-SPF 0.5 Sec. AVG B_1 B_2 B_3	≥ 100 @E_1 ≥ 40 @E_2 ≥ 80 @E_3	Consensus
!	Etendue [mm^2 Sr] (Max and min size TBD) E_1 E_2 E_3	5×10^{-4} 1.5×10^{-2} 4×10^{-3}	Consensus
	Power, ±1%BW [mW]	No Spec. For info only.	Consensus
	Inhomogeneity [%, within used Etendue]	≤ 5% spec ≤ 1% may be needed.	In review
!	Position Instability [%, $3\sigma_{center}$/FWHM] Avg over τ seconds. $3\sigma_{center}$/FWHM over 1 hour	≤ 3% Pos. ≤ 1.2% Size τ = TBD (10 to 300mS).	In review
	Temporal Energy Instability [%] 3σ, Avg 10mS windows. 3σ from 1 hour of data.	≤ 3%	In review. Target.
	Pulse timing error (Jitter)	≤ 1 μS Jitter	Target
	SEMI E10 Availability [%]	≥95%, 2015 Roadmap TBD	Consensus
!	Cleanliness (Source supplier to propose concept)	100%	Consensus
	Footprint [L ×W×H, meters]	≤ 3×3×2	In Review
	Control, minimum on period.	≤ 100 mS	Consensus

! = Must have spec. Tradeoffs possible in other specs.

Source TWG Conclusion

Good turnout. 25+ companies represented at the meeting.

Source improvements are needed for all EUV metrology tools (AIMS™ , blank and pattern mask inspection).

A consensus specification for metrology light sources was created with input from KLA, Lasertec, and Zeiss.

Metrology source requirements are very different from scanner sources! Much lower power, much lower Etendue, but very high brightness and stability.

Source suppliers are working closely with SEMATECH EMI and tool vendors to understand the project requirements.

Main Round Table Results

Source supplier presentations.

- The source suppliers presented very different approaches.
- Some time to digest the consolidate spec is needed.
- Specifications are easier than expected but nobody has a proven solution today.

Metro tool companies

- All metrology tool companies agree that a solution will not be available when needed without investment, but picking a winner today is difficult.

EMI & EIDEC Members:

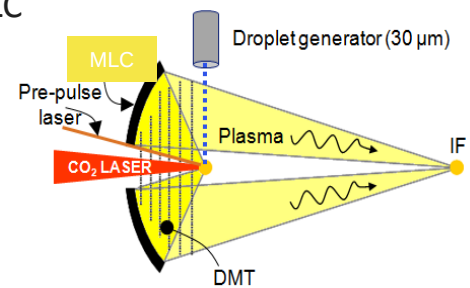
- We need to decide among different project strategies.
- Concept and feasibility data relative to specifications may be needed from a DPP and an LPP source before making a selection.
- A project Go/No-Go decision should be made soon or the Q3'2014 timeline will be at serious risk.

The greatest risk to EUVL adoption is the performance of the "front-end" – The Source Collector Module … if we are to solve this problem and accelerate adoption we may have to change the paradigm:

"OLD" EUVL Paradigm:

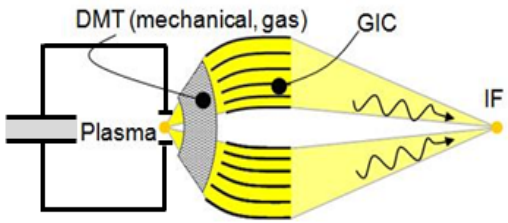
Two horse race: Which is the best system…?
LPP-MLC vs. DPP-GIC

LPP-MLC



VS.

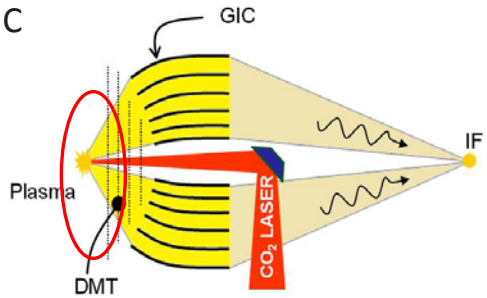
DPP-GIC



"NEW" EUVL Paradigm:

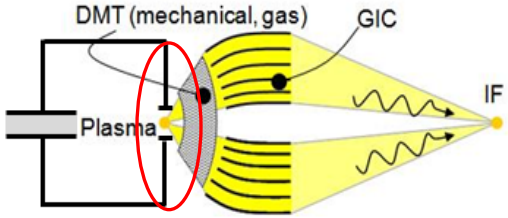
GIC is the only proven reliable collector for high power HVM.
Two horse race: Which is the best source…?
LPP vs. DPP

LPP-GIC



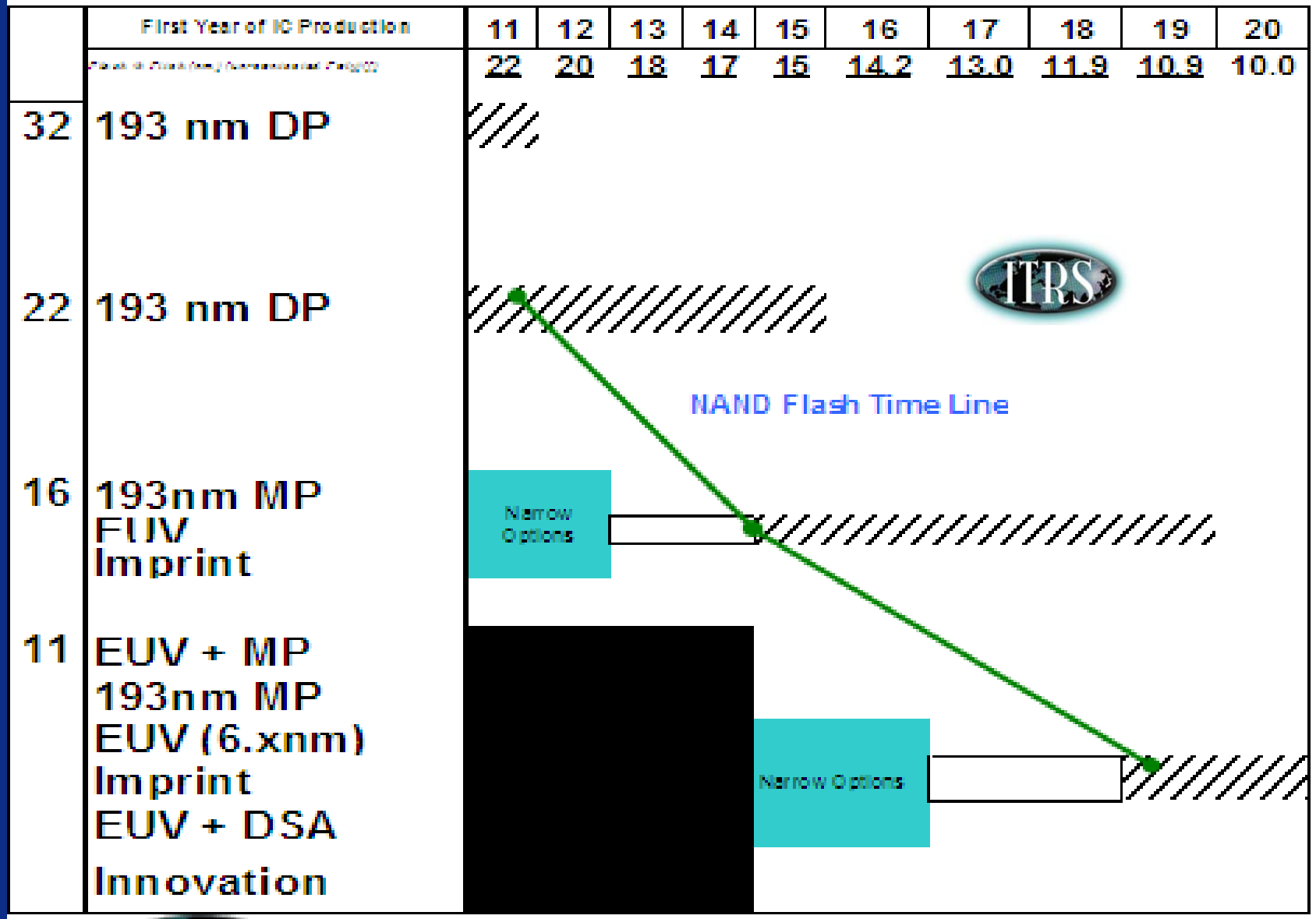
VS.

DPP-GIC



Agenda

1. Why?
2. What?
3. How?
4. When?
5. Conclusions


First Year of IC Production
11 12 13 14 15 16 17 18 19 20
22 20 18 17 15 14.2 13.0 11.9 10.9 10.0
32 193 nm DP
22 193 nm DP
16 193nm MP
FUV
Imprint
11 EUV + MP
193nm MP
EUV (6.xnm)
Imprint
EUV + DSA
Innovation
NAND Flash Time Line
Narrow Options
Narrow Options
ITRS
International Technology Roadmap for Semiconductors
Work in progress – Do not publish or distribute
5

EUV: Past, Present and Future

- 1985. First papers on EUV
- 1991. First demonstrations
- 1995. Why is this fab circular?
- 1996. The Nat Lab are shutting down EUVL!
- 2001. EUV LLC Demonstration.
  IEUVI Started (EUV LLC, ASET)
- 2002. First EUVL Symposium
- 2006. First 2 prototypes shipped
- 2010. First NXE shipped
- 2011. 32 IEUVI meeting held to date
- 2013. First HVM forecasted

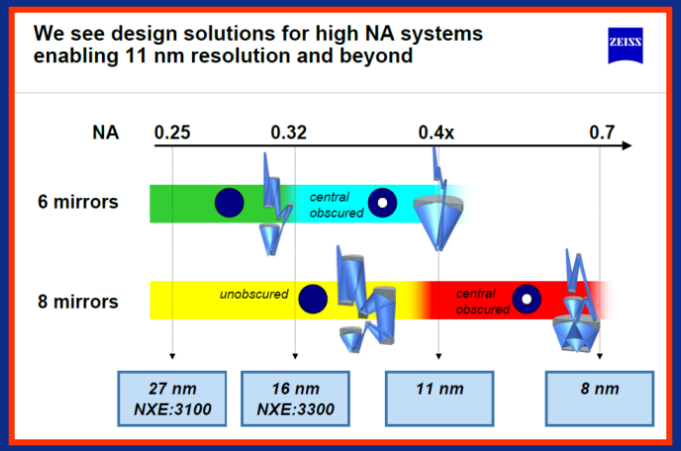
} 10 years

Short and Long Term Challenges

	Near Term Challenges (2011-2018) (16nm Logic/DRAM @ HVM; Flash 11nm @ optical narrowing with 16nm in HVM)
1	Defect "free" EUV masks availability, source power to meet throughput requirement; mask infrastructure availability; EUV mask in fab handling, storage, and requalification.
2	Multiple patterning - cost, throughput, complexity
3	Optical mask - complexity with SRAF, long write time,
4	Resist at 16nm and below that can meet sensitivity, resolution, LER requirements
5	Process control on key parameters such as overlay, CD control, LWR at 16nm HVM
6	Retooling requirements for 450mm transition
	Long Term Challenges (2019 - 2025) (11nm @HVM)
1	Higher source power, increase in NA, chief ray angle change on EUV; Mask material and thickness optimization
2	Defect free DSA processing
3	Metrology tool availability to key parameters such as CDU, thickness control, overlay, defect
4	Infrastructure for 6.Xnm Lithography or multiple patterning for EUVL 13.5nm
5	Early narrow and implement ~2 options with viable infrastructures support

Looking at Your Future

Multiple Passes with 13.5 nm



Build Infrastructure for 6.x nm

Agenda

1. Why?
2. What?
3. How?
4. When?
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CONCLUSIONS

- Semiconductor industry is experiencing a period of accelerated growth in number of units and in the amount of silicon area shipped
- This accelerated growth is driven by new exciting devices, by new applications and by new users
- New Devices will support the industry for the foreseable future (e.g., next 10 years)
- Lithography remains a fundamental enabler of miniaturization. Cooperation is a must!
- EUV (13.5nm) is finally approaching pre-manufacturing after 15 years of incubation but much still needs to be done!
- Which lithographic technology do you think will be used at 8nm and below?