# **EUV Defect Repair Strategy**







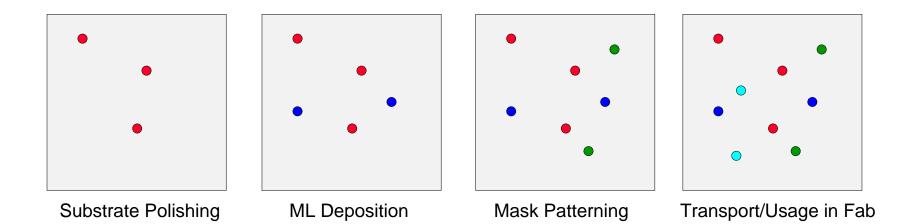
- 1 Blank and Mask Defects
- 2 Repair Strategy
- 3 AIMS EUV Status
- 4 Summary



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## "Defect Flow"



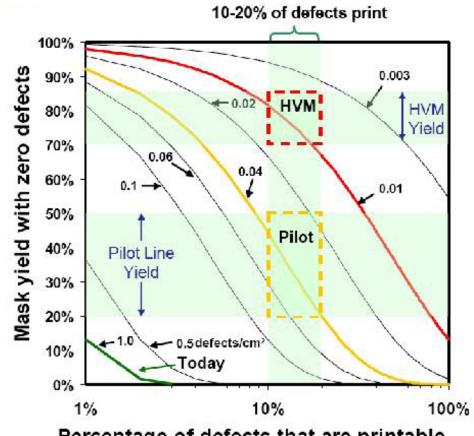


- Each manufacturing and handling step potentially adds defects (particle and/or pattern defects)
- Goal is to design a manufacturing flow that mitigates defects as much as possible or repairs defects that have been added in the preceding steps
- Target is zero printable defects

#### **Blank Defect Level**



- Large gap for "zero defect" blanks
   → low yield for production
- EUV blanks will still have defects when high volume manufacturing starts
- Challenge: take this fact into consideration for mask manufacturing



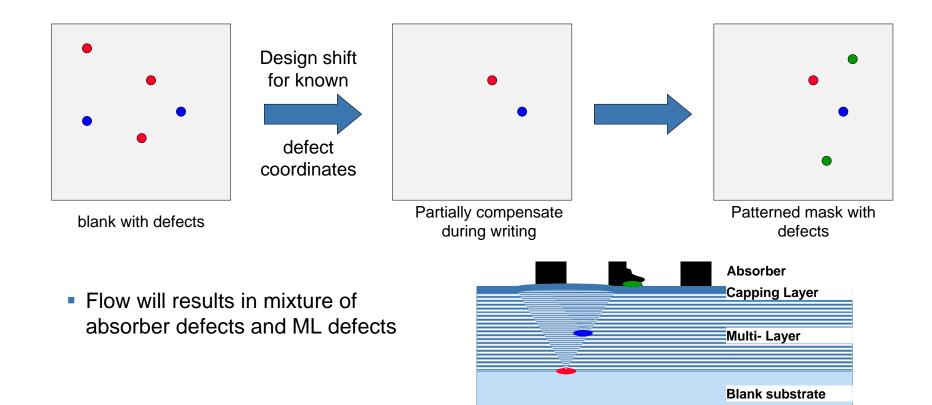
Percentage of defects that are printable

Source: SEMATECH

## **Mask Manufacturing Flow**



- Blank inspection tools need to deliver exact locations and sizes of defects
- Pattern will be placed in a way to hide majority of remaining defects
- Followed by standard mask manufacturing process

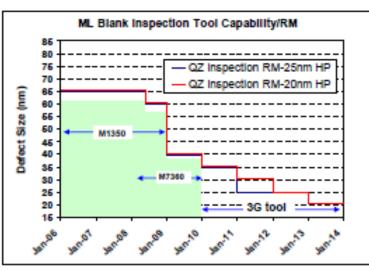


#### **Find and Review Defects**



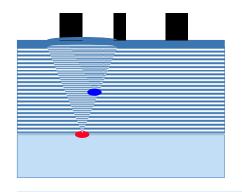
- There are infrastructure gaps to find and review defects with EUV light
- Joint industry effort to close the gaps led by SEMATECH
- One of the projects has started:
   AIMS™ EUV development to close defect actinic review gap





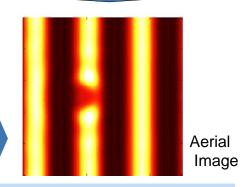
Source: Andy Ma (EUVL 2010 Kobe)

## Review defects



Blank defects convert Into phase defects

Phase defects cause printing defects although patterning was perfect



Solely actinic 13 nm mask qualifications by AIMS™ EUV can predict printing behavior of the defects in EUV mask manufacturing environment



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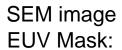
## **EUV** absorber and ML defect repair strategy

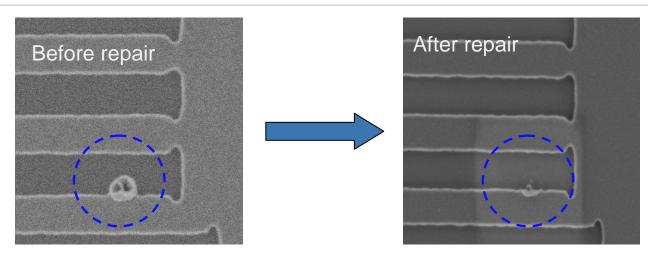


The MeRiT® can locate the exact position of defects with a surface topography With the ebeam (including BSE detector) With the in-situ AFM (optional feature) Classical absorber repair absorber repair Compensational repair

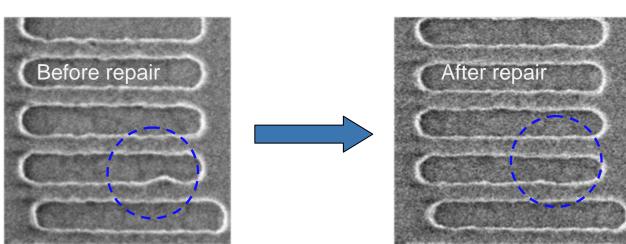
## Classical Absorber Repair with MeRiT® HR







SEM image Wafer print:

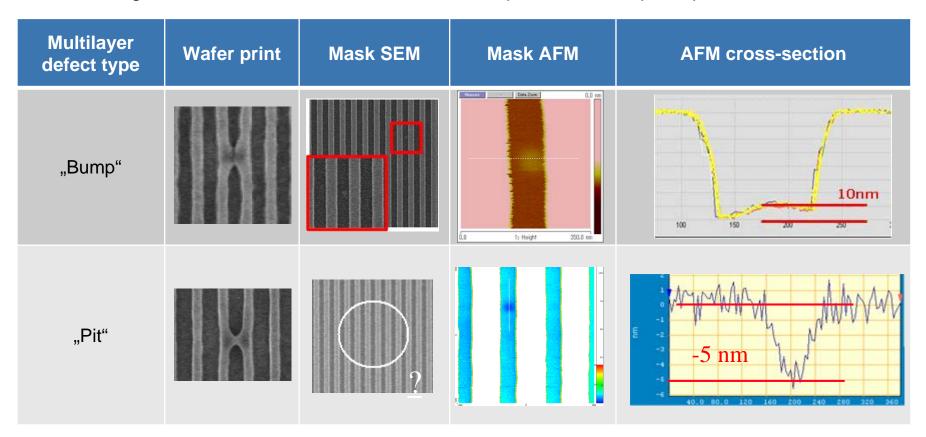


→ Defect was repaired successfully

## **EUV Defects and Compensational Repair**



- EUV-specific multilayer defects are often SEM-invisible → use AFM
- Printing defects can be +/- 3 nm shallow: Compensational repairs performed



## **Defect Repair with MeRiT® HR**

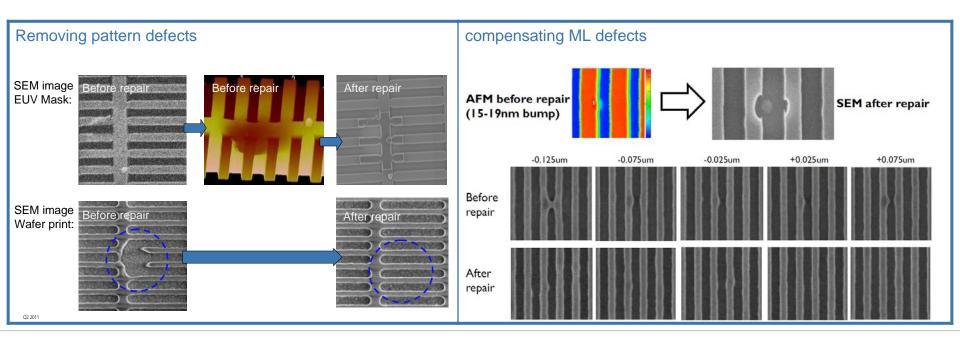


#### Removing pattern defects.

- EUV mask pattern repair possible already now with MeRiT® HR 32
- Further refinement with future platforms

#### Compensating effect of blank defects

- Mitigation of ML defects by compensational repair shown
- Making use of in-situ AFM feature of MeRiT® HR 32



## Repair Strategy using AIMS™ and MeRiT®



|      |  |                                 | AIMS™ EUV                   | MeRiT® HR  | AIMS™ EUV                 |
|------|--|---------------------------------|-----------------------------|--|---------------------------|
|      | Defect map   | Defect Type                     | Defect Review               | Repair Strategy  | Repair Review             |
| 193  | Defect Map<br>Pattern Inspection                           | Phase & Transmission_<br>Defect | ► <mark>AIMS™ Review</mark> | ≯Absorber Repair——   | AIMS™ Review              |
| EUVL | Defect Map Pattern Inspection  Defect Map Blank Inspection | Absorber Defect                 | - ►AIMS™ Review             | ≯Absorber Repair——   | —>AIMS™ Review            |
|      |  | Multi-Layer Defect              |                             | Compensational Absorber Repair  Compensational Pattern Placement | AIMS™ Review AIMS™ Review |

- AIMS<sup>TM</sup>EUV review needed for both defect types and repair strategies
- Number of processes requiring review increases in EUV compared to 193 increased



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## **AIMS™ EUV Project started**



# Industry-Leading Semiconductor Companies Join SEMATECH's EUVL Mask Infrastructure (EMI) Partnership at UAlbany NanoCollege

Carl Zeiss begins main development of AIMS™ System to target mask defects for 22 nm half-pitch node and below

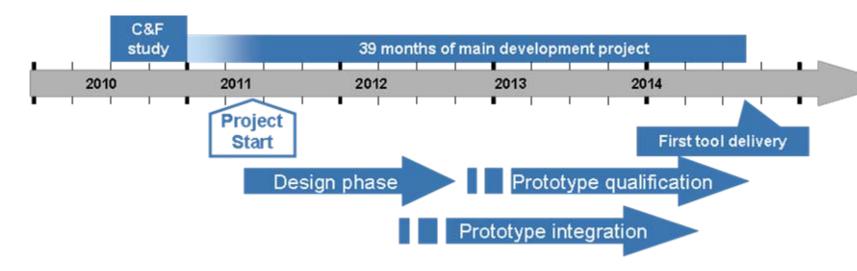
ALBANY, N.Y. and JENA, GERMANY – July 12, 2011 – SEMATECH announced today that Intel, GLOBALFOUNDRIES, Samsung Electronics Co., Ltd., and TSMC have joined SEMATECH's EMI Partnership to develop critical metrology tools for reviewing defects in advanced masks needed for extreme ultraviolet lithography (EUVL). In collaboration with SEMATECH, these leading semiconductor companies are pursuing an ambitious metrology program to enable defect-free EUVL masks for high-volume manufacturing.

→ see also Session 3, Monday, 17. Oct., Michael Goldstein "Update from the Sematech EUV Mask Infrastrutcure Initiative"

#### Defect Review with AIMS™ EUV

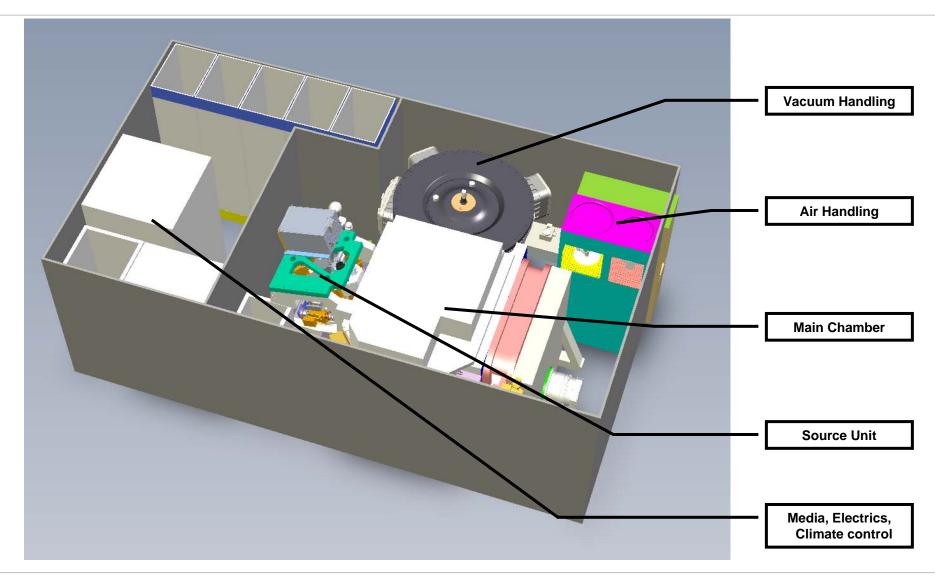


- Project started in June 2011
- 4 industrial partners
- Prototype ready by August 2014
- First customer tools ready by August 2014 then 1 tool every 4 months
- Currently project is within the design phase



# AIMS™ EUV Design Phase: Preliminary Layout of the AIMS™EUV







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## **Summary**



#### Essential to find and classify all defects

- Current blank and mask pattern inspection methods not sufficient
- Joint industry effort started to close gaps
- AIMS™ EUV needed for disposition or repair verification
- AIMS<sup>™</sup> EUV project started and on track

#### Repair or mitigate defects

- Blank defect mitigation concepts existing but need to be proven in process flow
- Pattern defects can be repaired as for standard 193nm masks
- ML defects cannot be repaired as of today
- ML defect however can be compensated by compensational repair methods

Zeiss provides critical tools and solutions for EUV mask manufacturing

Mask manufacturing tools will be ready in time for HVM

## **Acknowledgements**



#### Defect studies and repair

Tristan Bret, Thorsten Hofmann and the Zeiss SMS team in Rossdorf

#### AIMS™ EUV

- Sascha Perlitz and Markus Weiss and the Zeiss teams in Jena and Oberkochen
- Sematech and the members of the EMI Consortium for their great financial support

And thanks to you for your attention!



We make it visible.