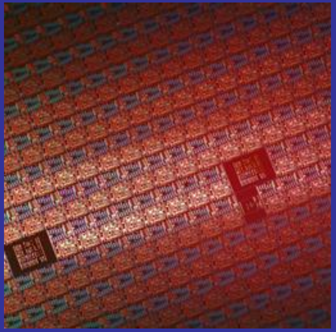
Accelerating the next technology revolution

SEMATECH's Perspective on EUV Mask Blank Status and Manufacturing Infrastructure

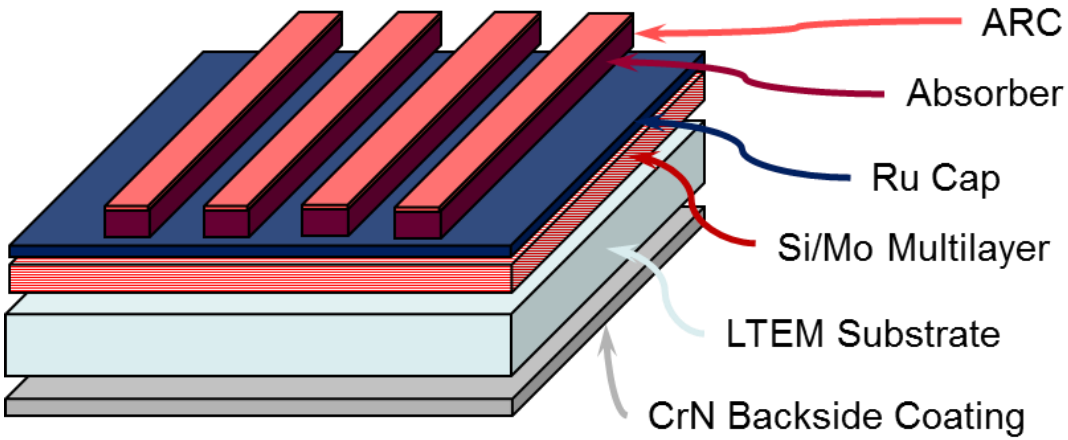
Frank Goodwin, Patrick Kearny



19Oct2011

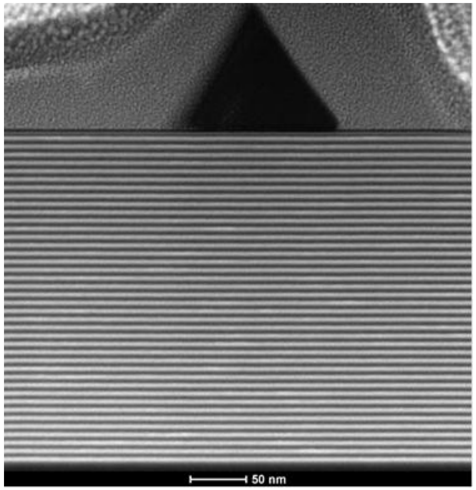
Challenges to Meeting EUV Mask Blank Requirements

- Absorber/ARC Stack
  - Optical Properties at EUV
  - Properties at Inspection Wavelengths
  - Defectivity
  - Etch Performance
- Ru Cap
  - Defectivity
  - Film Loss from Etch
  - Metrology
- Multilayer
  - Defectivity
  - Uniformity
  - Reflectivity and Centroid Wavelength
  - Metrology (Defect Detection)
- Substrate
  - Thermal Properties
  - Defectivity
  - Flatness and Surface Roughness
  - Metrology (Defect Detection)
- Backside Coating
  - Electrical Properties
  - Defectivity

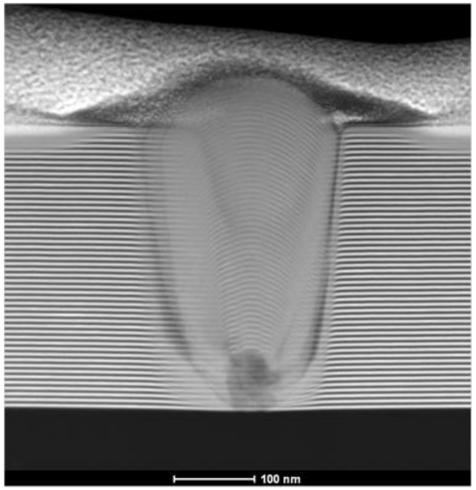


EUV Mask Blank Defect Types

- EUV mask blanks are vulnerable to basically two types of defects
  - Amplitude defects:
    - Surface particles/pits that generate contrast changes at the wafer
    - Potential for repair or mitigation
  - Phase defects:
    - Particles or pits at the substrate which become buried below the multilayer
    - Particles imbedded in the multilayer
    - Result in a phase change of the reflected wave
    - Phase defects as small as 1 nm in height or depth can result in printable defect
    - Not repairable



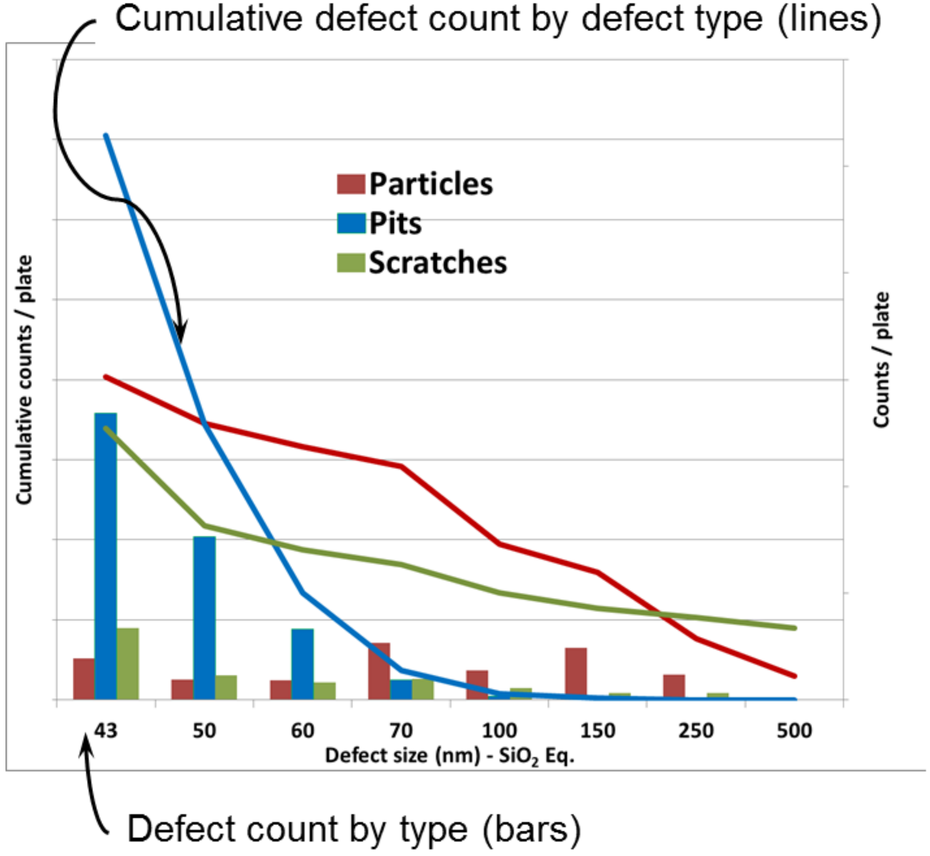
Amplitude defect



Phase defect

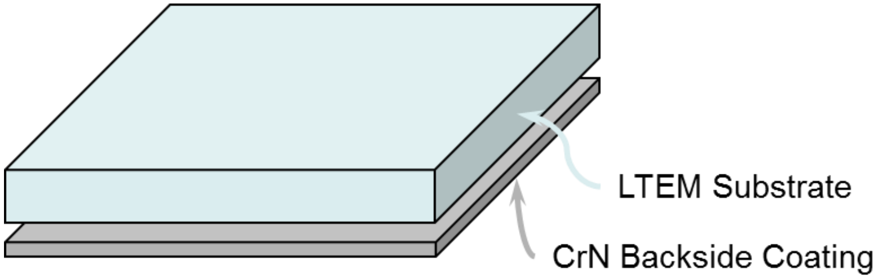
Trend of Mask Blank Defects

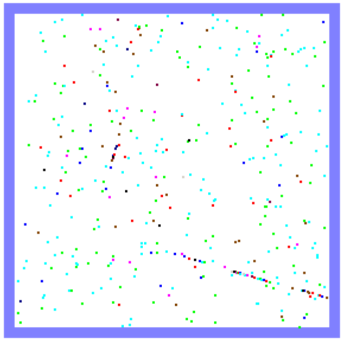
- Indication of defect trends
  - Cumulative plot of defect count against defect size
- Particle type defects have a linear trend
  - From deposition process and substrate
  - Particle defect counts do not scale by power law as size decreases
- Pit Type and Scratches
  - Originate at the substrate
  - Both defects signatures increase exponentially



Substrate Defects

- Substrate pits and scratches
  - Majority become visible after ML deposition through decoration
  - Affect substrate cleaning efficiency by trapping particles
- Not detection during substrate inspection
  - Decoration through ML deposition is of limited value
    - Adds to cycle time and reduces learning cycles
    - Adds complexity to data analysis
- Reduction of substrate defects is the most critical challenge to achieving defect free mask blanks
- Will require substrate inspection capability

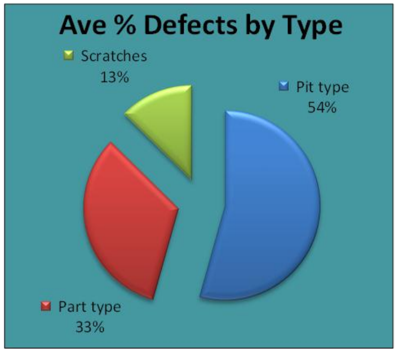




Pixel Histogram

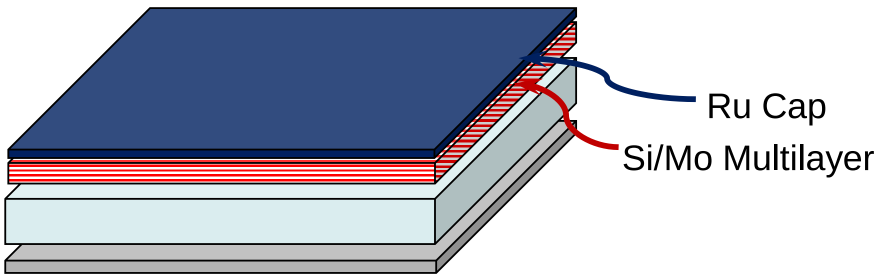
After ML deposition
- Pre-inspection
  - 1 Pit
  - 1 Scratch
  - 0 Particles
- Post Inspection
  - 33 Pits
  - 30 Scratches
  - 11 Particles

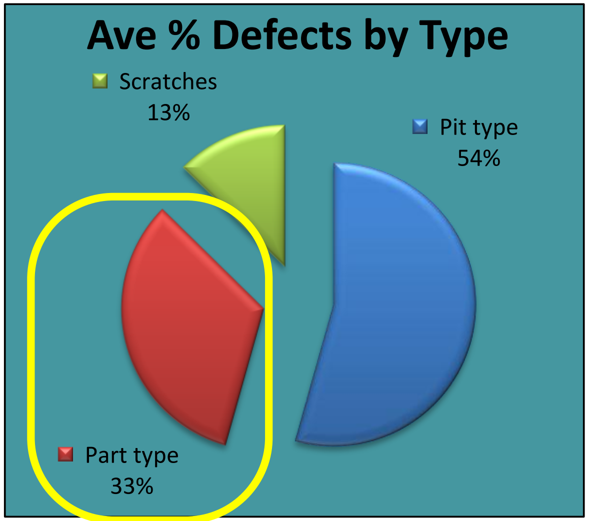
Mask Blank defectivity
- Particles – 33%
- Substrate Pits – 54%
- Substrate Scratches – 13%



ML and Ru Cap Defects

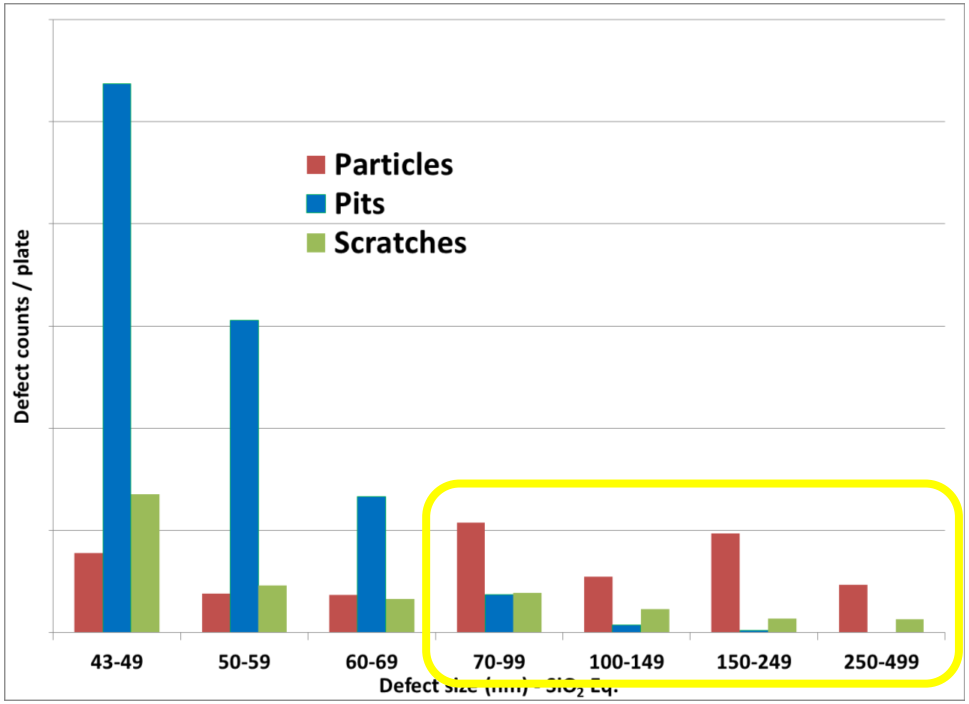
- Particle type defects
  - Substrate (CMP, Cleaning, Handling)
  - Si/Mo ML Deposition
  - Ru Cap Deposition
  - ~ 1/3 of total mask blank defects
- Particle type defects < 80nm in size (SiO_2 equiv)
  - Handling
  - Substrate
- Defects from deposition typically “larger in size”
  - 100 – 500 nm
  - Shield and Ru defects dominate





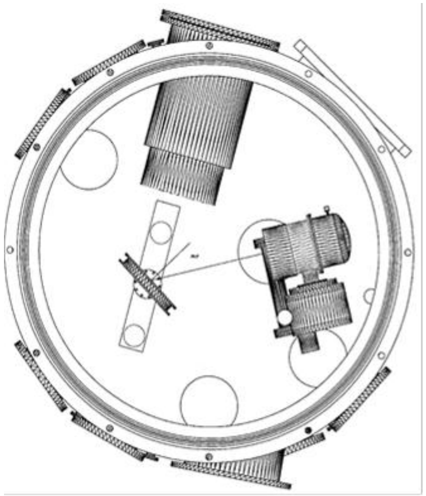
Particle Type Defects

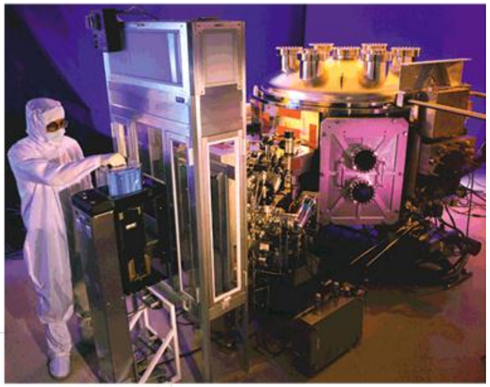
- Defect density for mask blanks have improved
- However the size distribution has not changed
  - Still large “killer” particles
- Potential for improvement is limited by tool design

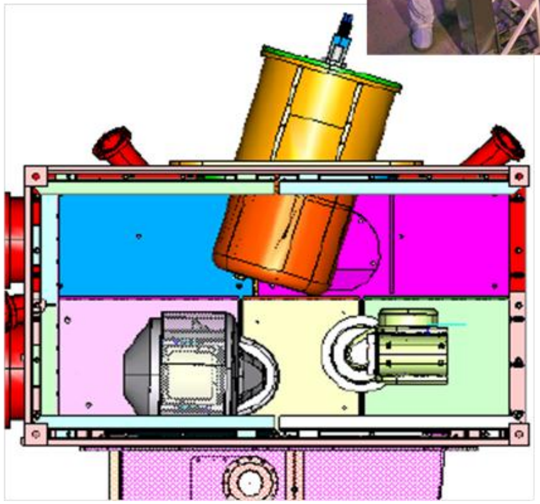


Veeco Nexus LDD IBD Tool

- Configuration of current tool
  - Source, target, and substrate locations identical to 1995 Lawrence Livermore design
  - Same ion source
    - Advanced RIM-210 Ion Source
- Modifications
  - Target Turret
    - Supports 4 water cooled targets
  - Removable stainless shields
    - Cover the chamber walls, target turret, and substrate fixture
  - Rectangular chamber design select by tool manufacturer
- Focused ion beam
  - Dished grids
  - Ideally etches a 3-inch erosion spot in center of target

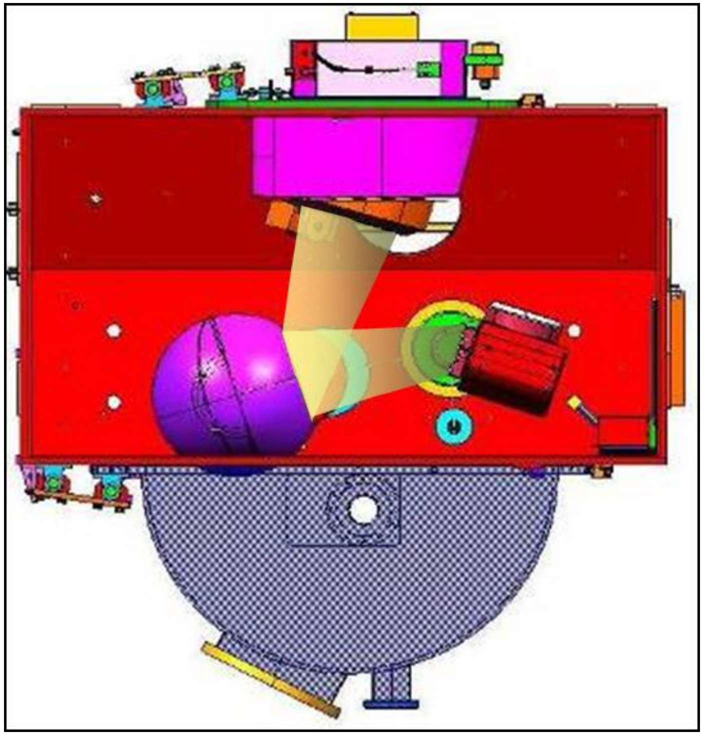




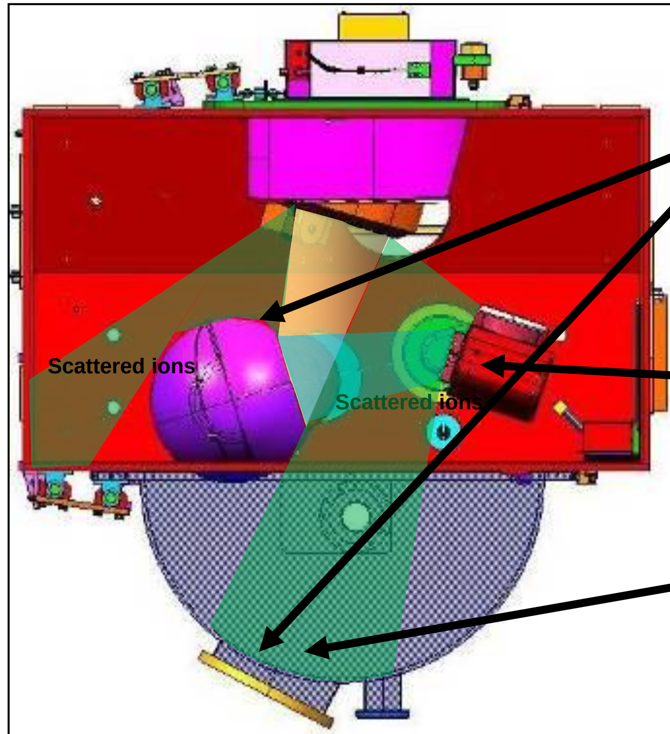


Overspray of Ion Source

Ideal Ion Beam Profile



Real Ion Beam Profile



Ions hitting shields

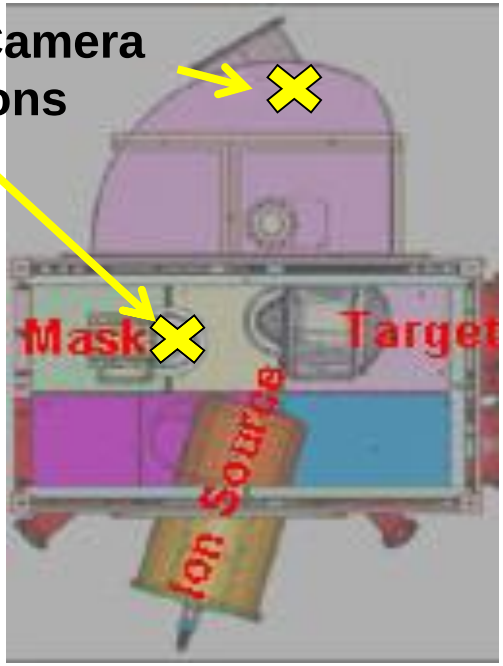
Ions hitting substrate

Etching of door shield

- Divergence of the ion beam result in ions hitting shields
- Was not predicted by modeling of ion source

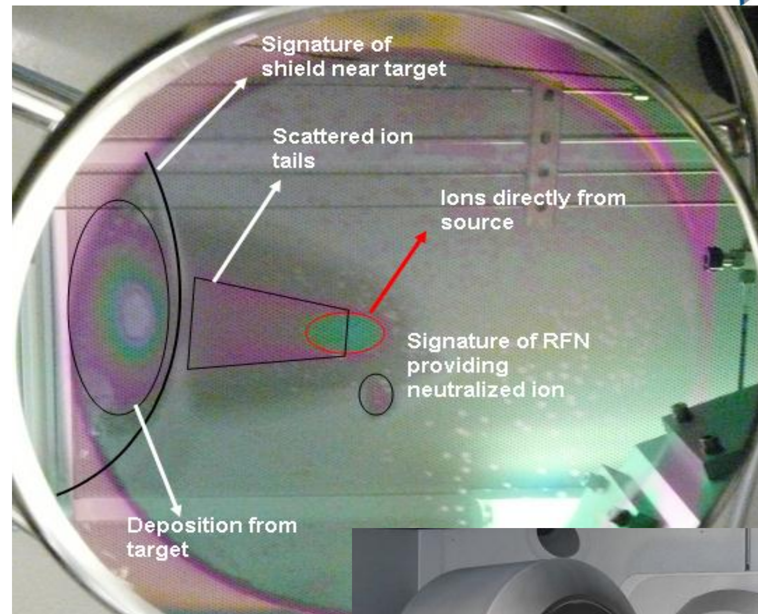
Imaging of the Ion Beam

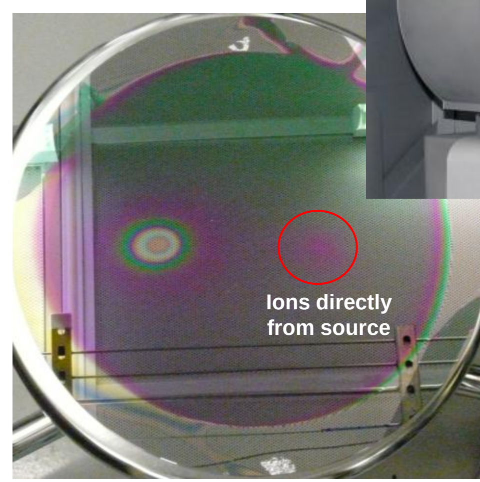
- Pinhole cameras were installed to image were the ions were going
  - One on the chamber door
  - One on the e-chuck of the substrate fixture
- Oxide wafers were used as image media
  - Etching of oxide shows were ions impact
  - Deposition will show path of atoms from target



Pinhole Camera Image

- Door camera provided a detailed image of the target, ion beam, and beam divergence
  - Target image shows erosion pattern, beam tails and target shield
  - Heavily etch area shows the ions coming directly from the source
  - Beam divergence is indicated by the lighter etched area
  - Ions are also coming from the neutralizer
- Substrate camera showed that the ions also hit the substrate
- To prevent sputtering of shields and substrate the divergence of the ion source must be controlled

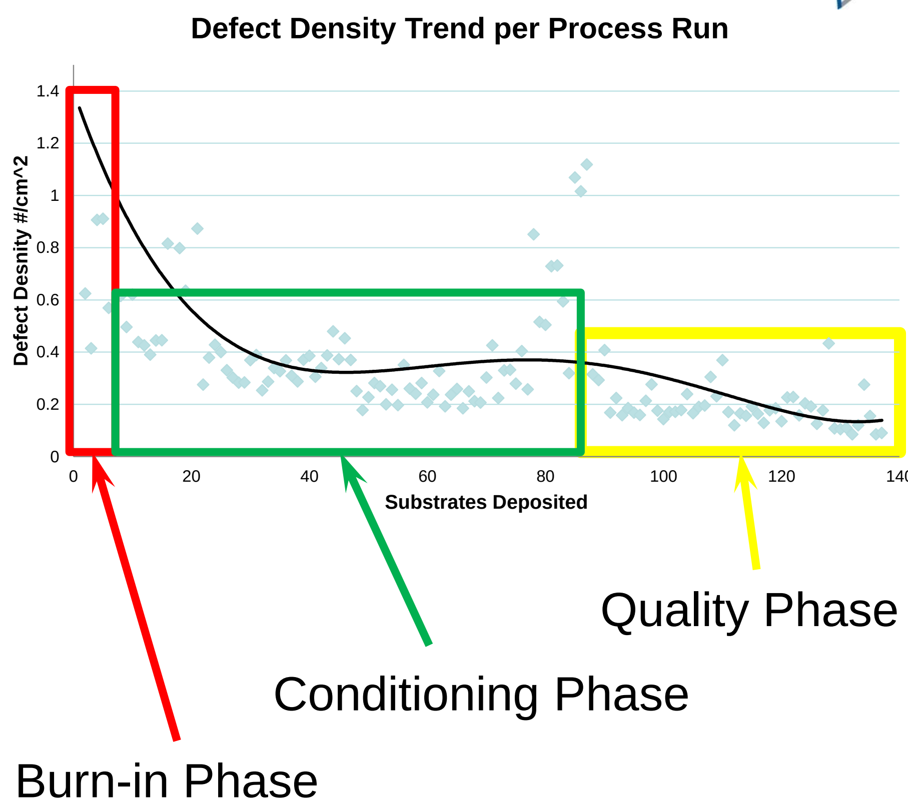




Process Yield: Quality Deposition Region

SEMATECH

- Typical defectivity trend
- Three phases of deposition
  - Burn-in phase
    - Target and Ion Source burn-in
    - Deposition defects
    - High defect counts
      - >200nm in size
  - Conditioning phase
    - Coating of shields
    - Moderate defect counts
    - Primarily from deposition and handling
  - Quality phase
    - External sources
      - Handling, Cleaning, Substrates
    - All champion data from this region



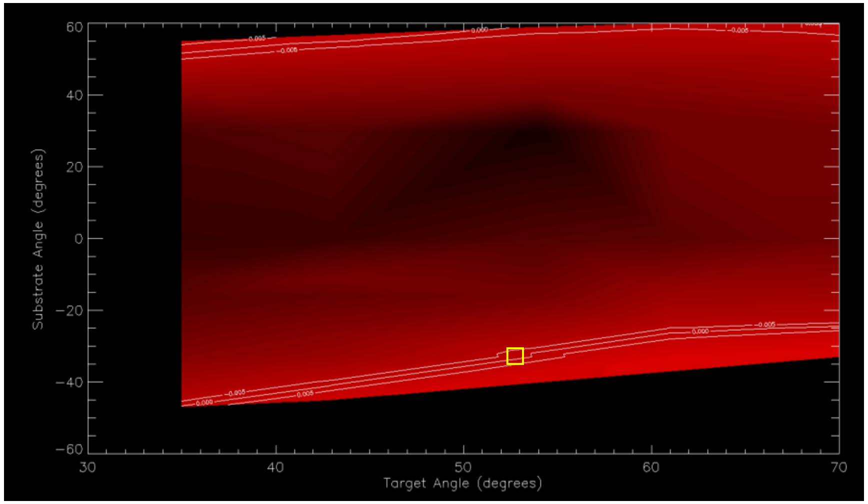
Good quality mask blanks

- ~ 30% of tail-end of deposition process run
- Only last 10% (10 to 15 mask blanks) reach a 0.1 defect density

Additional Limitation: Mask Blank Uniformity Process Window

- Reflectance uniformity requirement is ±0.5% over mask blank
- Meeting this requires a combination of substrate rotation and precise positioning of target and substrate
  - As target erodes the deposition plume shifts
  - Uniformity can not be maintained without adjustment to target and substrate angle
- Current process window:
  - Allowed target angle variance of 1°
  - Substrate angle variance of 4°

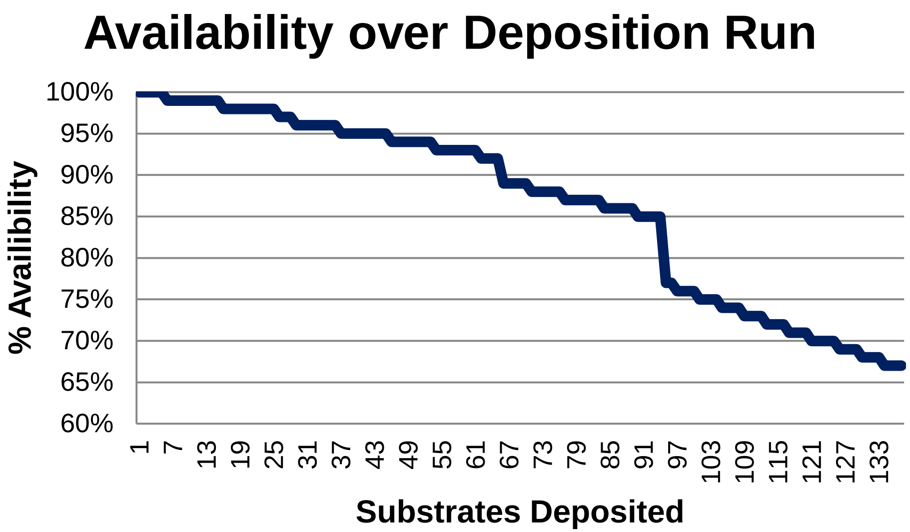
Map of uniformity over available substrate and target tilt angles



- Process window limited by:
  - Substrate location
  - Roughness of ML

Productivity Hit

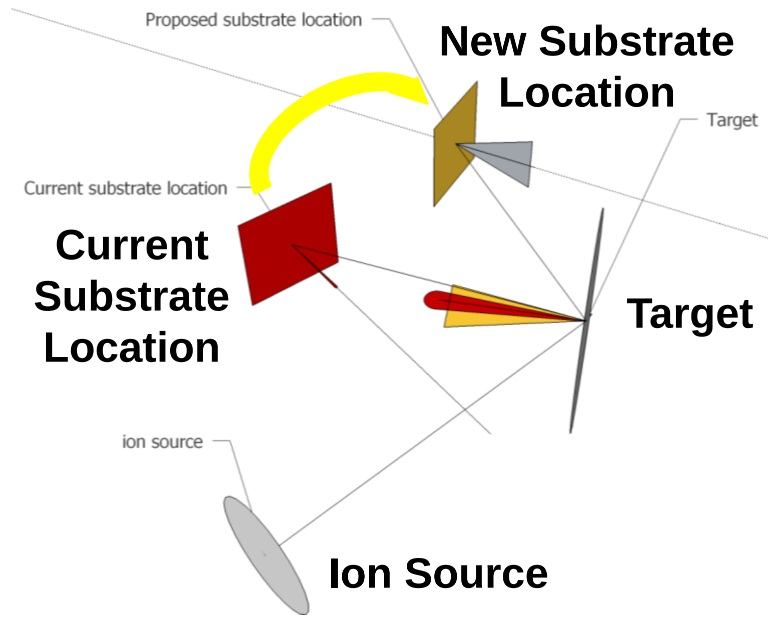
- Recovering uniformity requires adjustment of the substrate and target angles
  - Deposition is halted until a new operating point is determined
  - Requires EUV reflectivity measurements to confirm
- Tool availability impacted by the limit uniformity process window
  - 30 to 35% cumulative down time over course of a deposition run

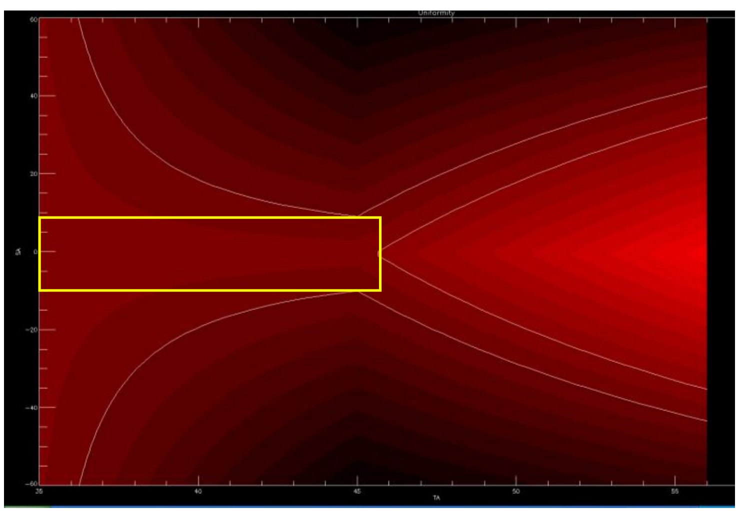


- Target and substrate angles go from requiring adjustment every 5 days to every 2 days

New Substrate Location

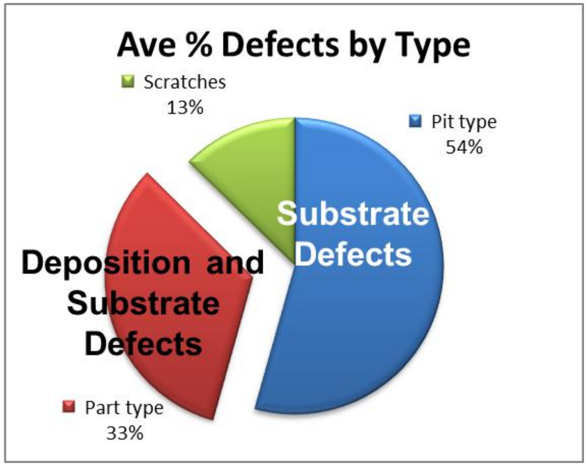
- Modeled process window at different substrate location
  - Target angle=11°
  - Substrate angle=18°
- Requires moving the substrate 15”and changing tilt
- Should enable a full deposition run without adjusting substrate and target angles





EUV Mask Status

- Challenges continue with substrate and multilayer deposition
- ML Deposition
  - Defects from deposition still an issue
  - Low process yield
  - Availability limited by substrate location
- Substrate Defects
  - Defects become visible after deposition
  - Increase exponentially as defect size decreases
  - Potential to be a showstopper
- Infrastructure
  - New generation of ML deposition tool is needed
  - Solution for substrate defects required
    - Metrology – Substrate Inspection



Acknowledgements

- SEMATECH
  - Members of SEMATECH's Defect Reduction Program, Failure Analysis Group, and Mask Blank Development Center
  - Ranganath Teki
  - Andy Ma (Intel Assignee)
- AGC
  - Junichi Kageyama

Thank You

Accelerating the next technology revolution

Research

Development

Manufacturing