FROM ASML **ALPHA DEMO TOOL** TO ASML **NXE:3100** AT IMEC

EUV LITHOGRAPHY HEADING TOWARDS PRE-PRODUCTION MODE

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imec

CONTENTS

EUV ADT & NXE:3100 installation

NXE:3100 vs. EUV ADT

- 27nm LS image formation
- Off-axis illumination
- Flare
- Overlay

Conclusions

ADT USE 2008-2011

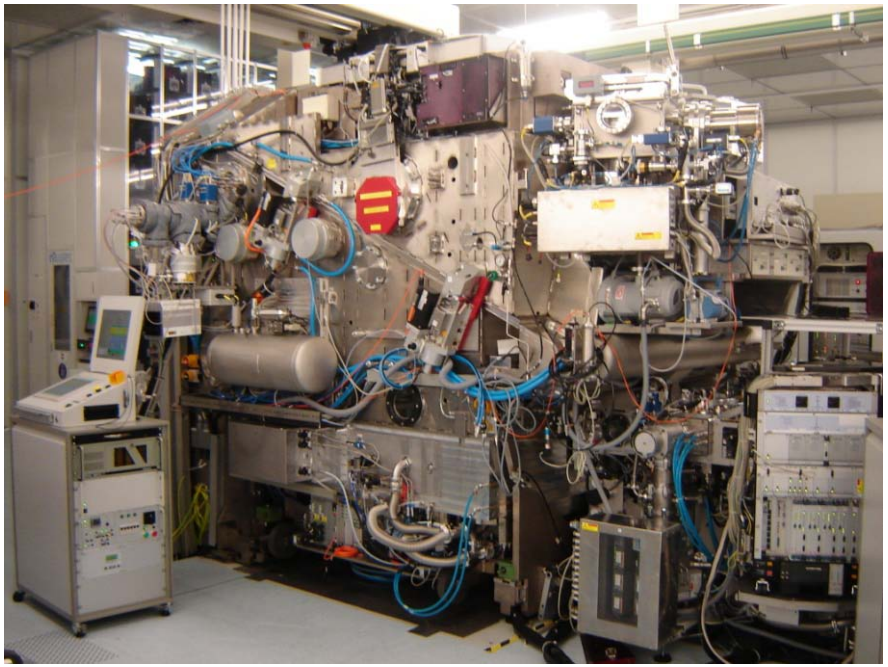
Main specifications

- Field size: 26x24mm^2
- NA=0.25 and σ=0.5
- Flare < 16%
- Wafer CDU 40nm LS < 4nm 3σ

Interfaced to TEL ACT12 track

Site acceptance on June, 2008

XTREME 170W/2π DPP source (July 2009)



More than 4000 wafers exposed since SAT 2010: 60% uptime – 42% productive time

EXTENSION OF 10,000m² CLEAN ROOM FOR EUV TOOLS

NXE:3100

Main specifications

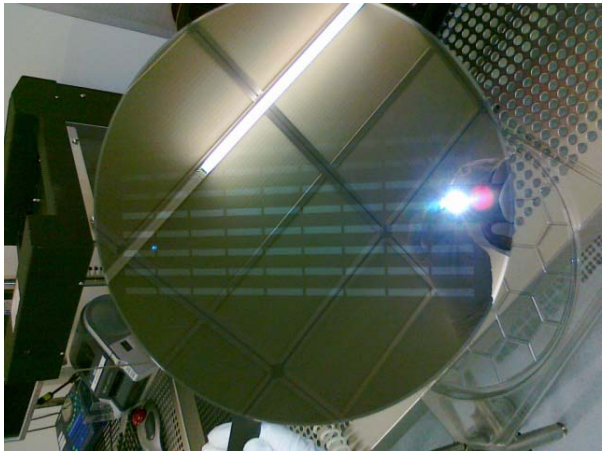
- Field size: 26x33mm^2
- NA=0.25 and σ=0.81
- 6 off-axis illumination conditions available
- Flare < 8%
- Wafer CDU 3s 27nm LS < 2.0 nm (corrected)

Interfaced to TEL Lithius Pro for EUV

XTREME Laser assisted DPP source

FAT in Feb 2011 (~7 Watt at IF shown)

First wafer at imec on May 2nd, 2011



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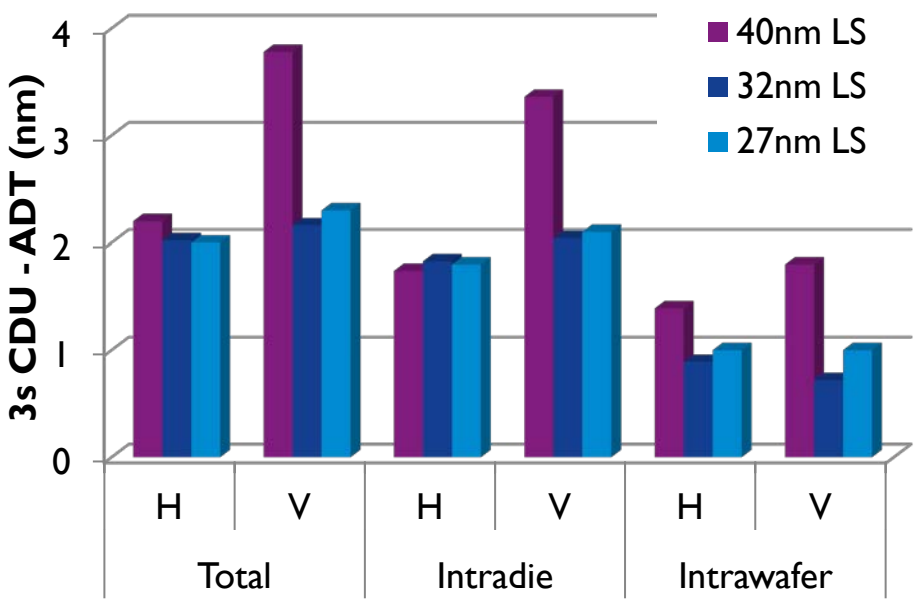
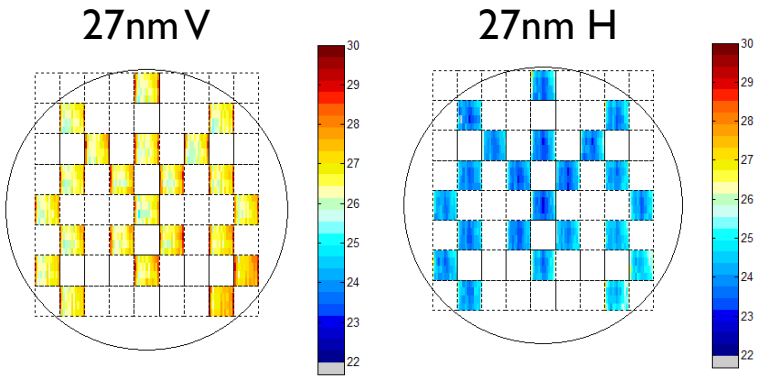
EVOLUTION OF WAFER CDU ON ADT



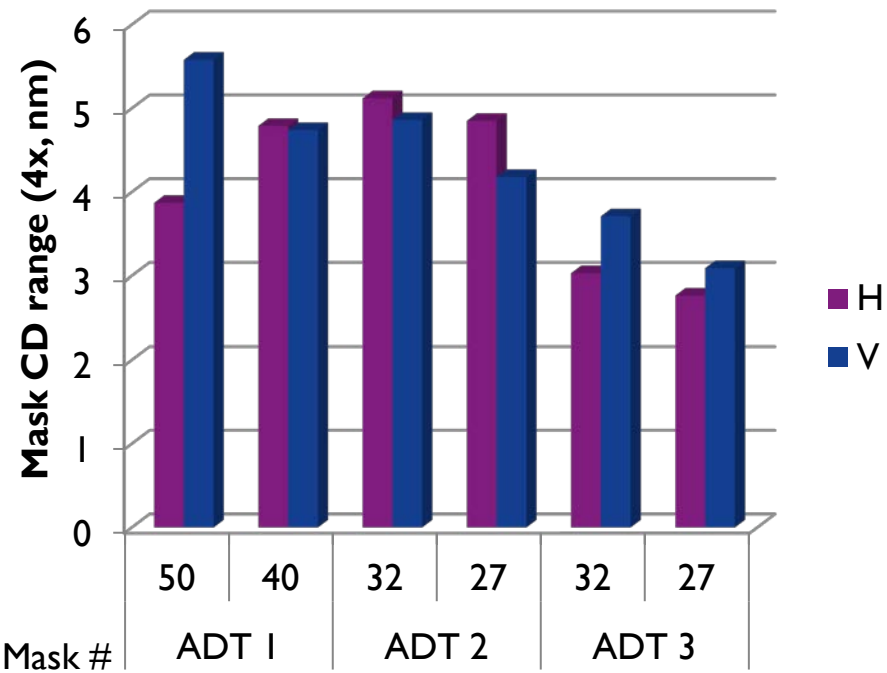
Feature	Year	Resist	Mask
40nm LS	2008	ADT1	ADT1
32nm LS	2009	ADT2	ADT2
27nm LS	2010	ADT3	ADT3

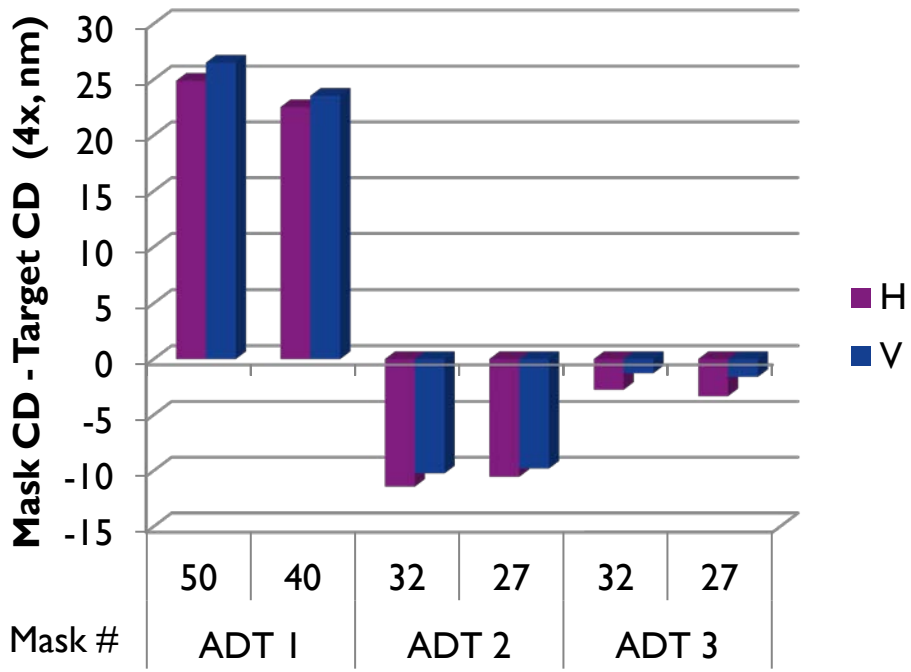


Across wafer CDU greatly improved over time
27nm LS feature size demonstrated in 2010

2010 EUVL Symposium, E. Hendrickx

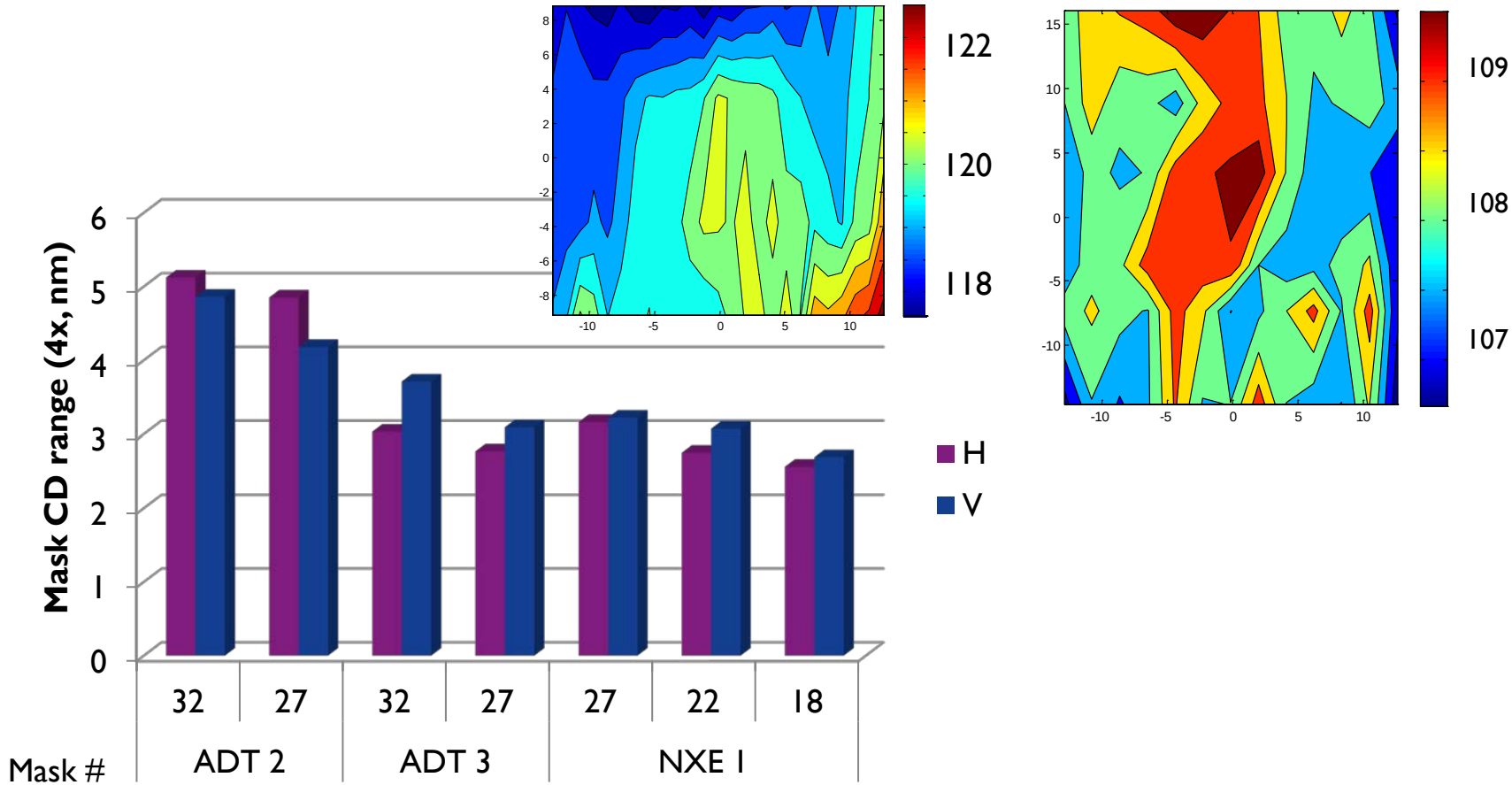
EVOLUTION OF CDU AND MTT ON ADT MASKS





Mask CD, mask CD uniformity, mask CD mean to target decrease over time for ADT monitor mask

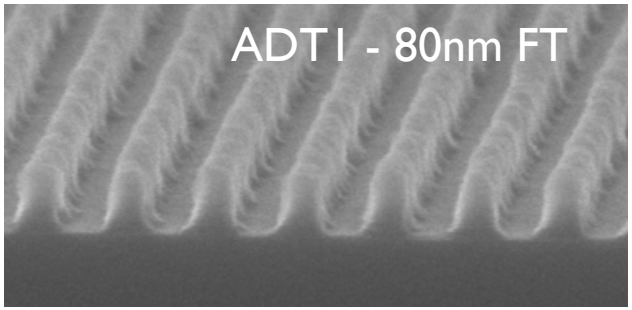
EVOLUTION OF CDU AND MTT ON NXE MASK



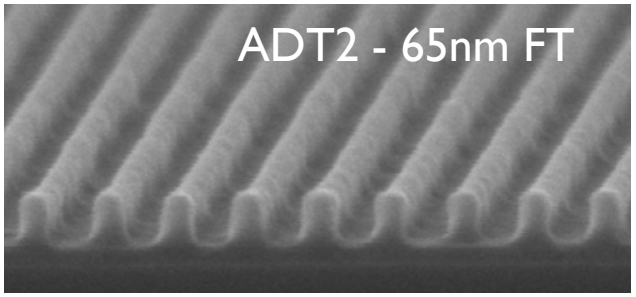
Good uniformity – but now for full 26 x 33mm image field and at 18nm LS

EVOLUTION OF EUV RESIST PERFORMANCE

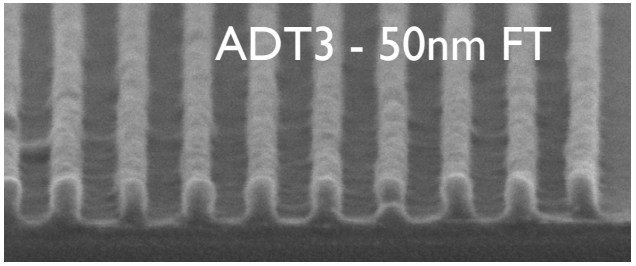
ADT



2008: 40nm LS

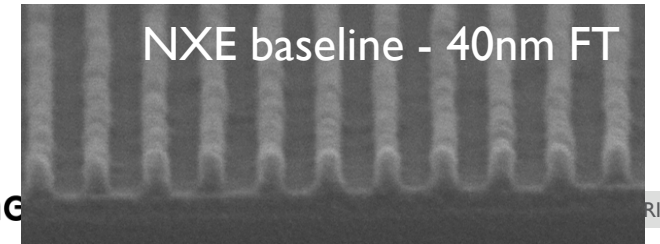


2009: 32nm LS



2010: 27nm LS

NXE

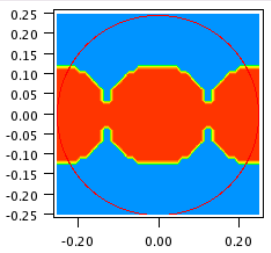
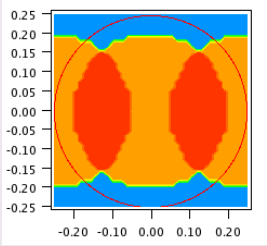


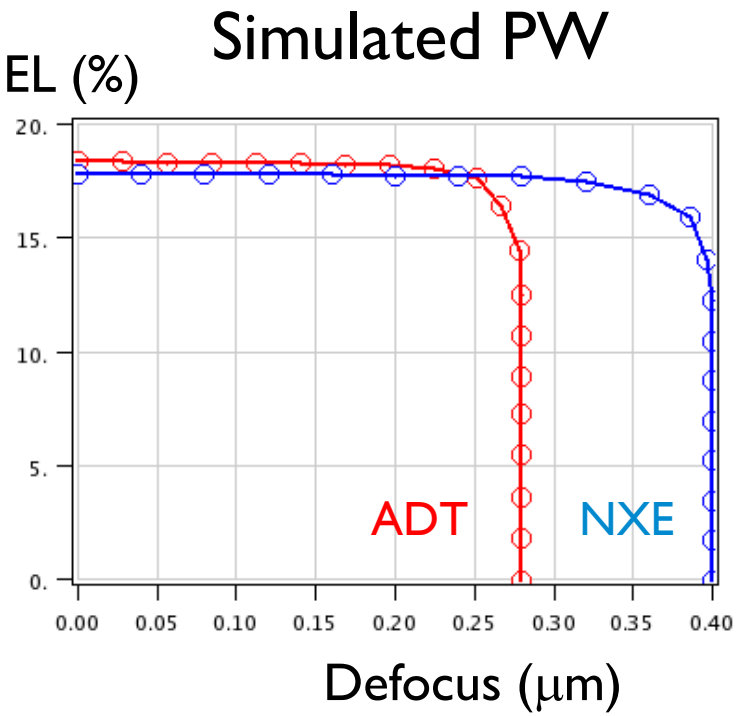
2011: 22nm LS

Ultimate resolution
80nm pitch to
44nm pitch

EUV resistscreening,
M. Goethals, session 4

EXPECTED IMAGING PERFORMANCE IMPROVEMENT ADT-NXE

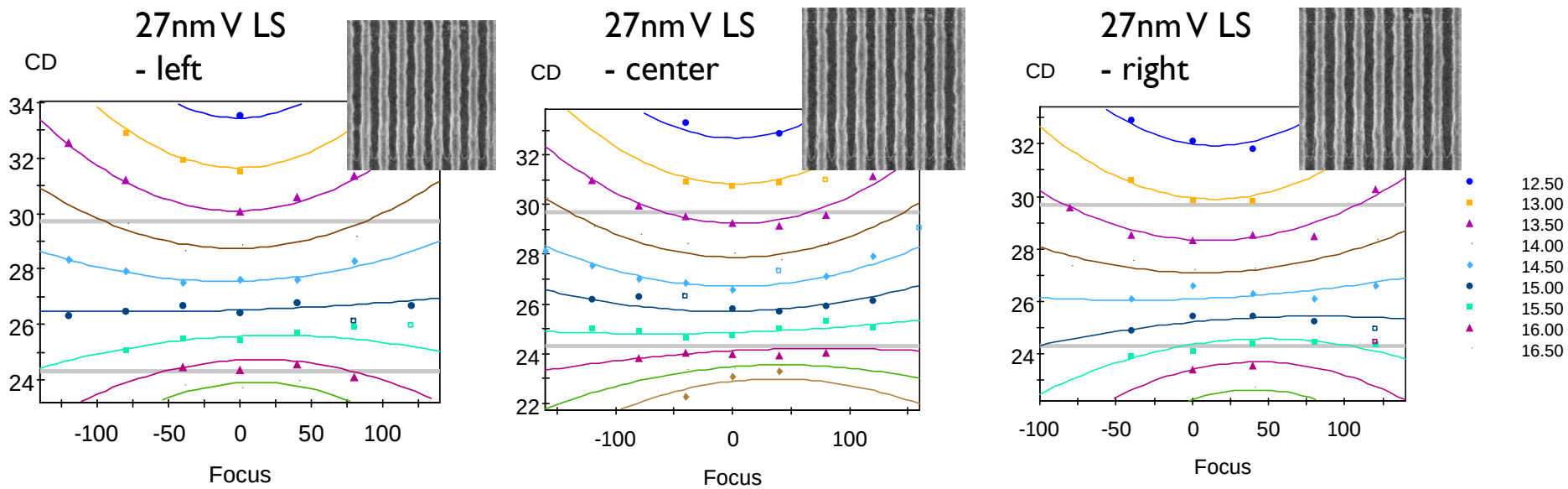
	ADT	NXE
NA	0.25	
λ (nm)	13.5	
σ	0.5	0.8
Pupil 27nm V LS		



Similar Exposure Latitude for 27nm V LS on ADT and NXE
NXE:3100 should have larger Depth of Focus

NXE:3100 PROCESS WINDOWS OF 27NM LS

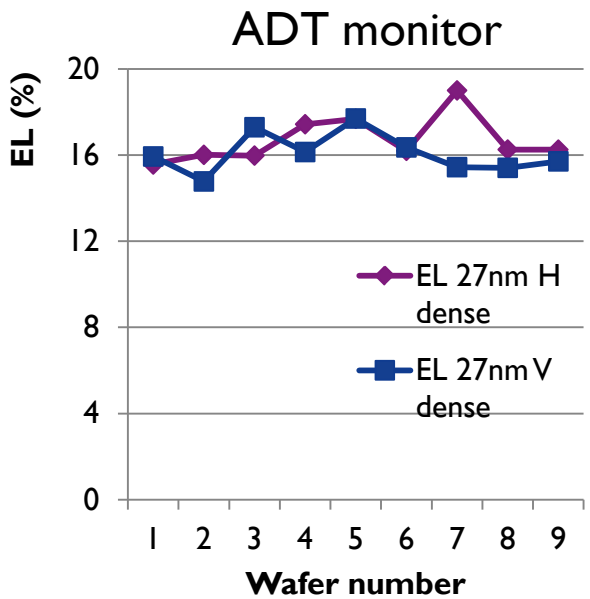
- Process window of 27nm LS across slit – baseline process



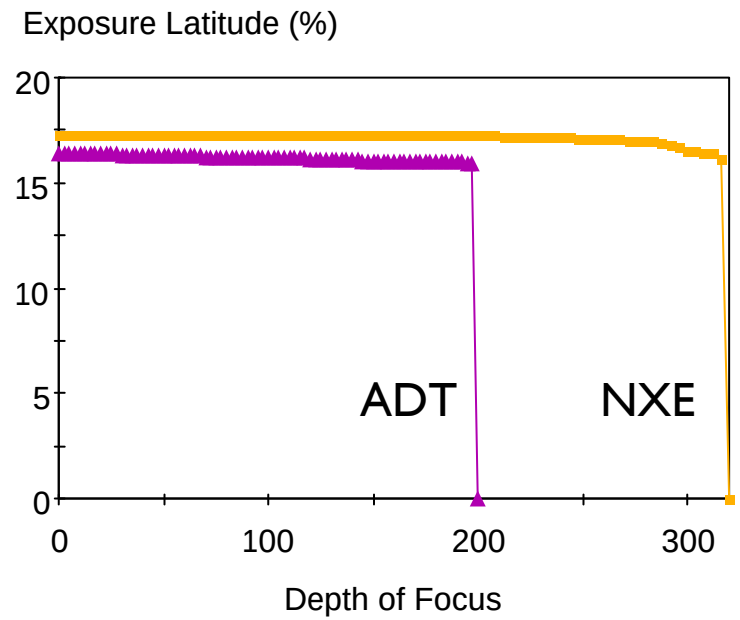
Maximal Exposure latitude V lines: 17%
Maximal Exposure latitude H lines: 17%

ADT – NXE COMPARISON OF EL FOR 27NM LS

- EL measured for 27nm LS on EUV ADT on weekly monitor wafer – same process



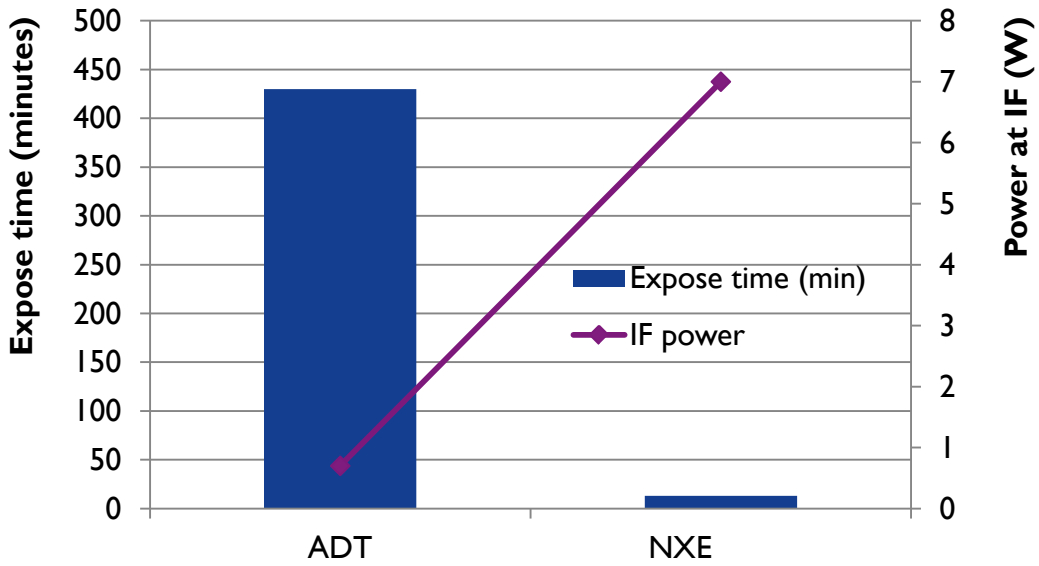
Average EL 16-17%



Experimental data confirm expected values for DOF and EL

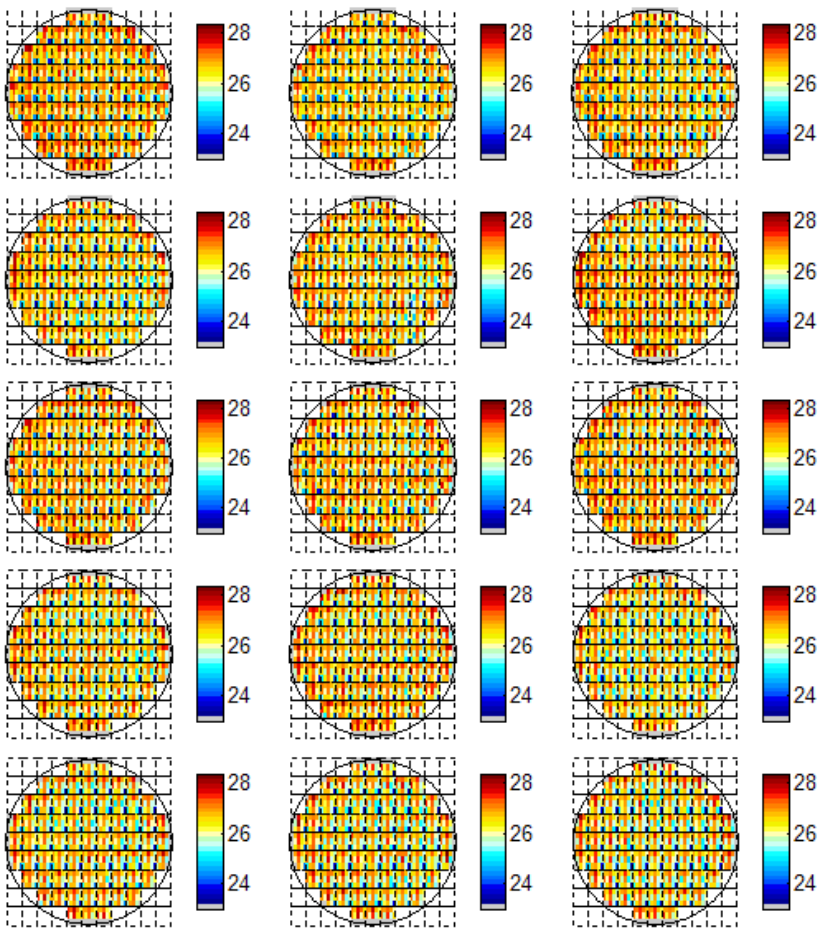
NXE:3100 TIME PER WAFER

- Compared to EUV ADT, NXE:3100 throughput at 7W IF is a factor of ~30 larger, which enables exposure of wafer batches
  - At 7W IF power, full wafer exposure at 27nm LS dose to size takes ~13 minutes when using both exposure chucks



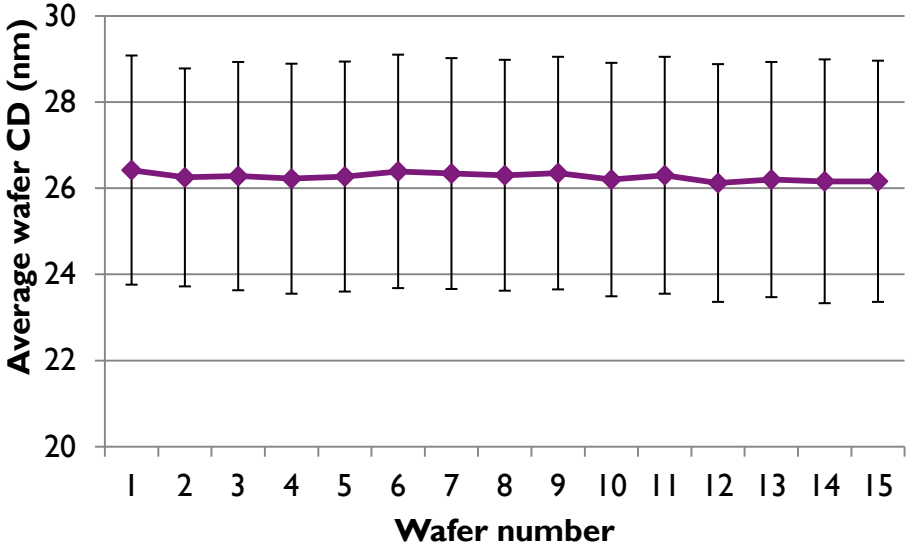
CD UNIFORMITY THROUGH WAFER BATCH FOR NXE:3100

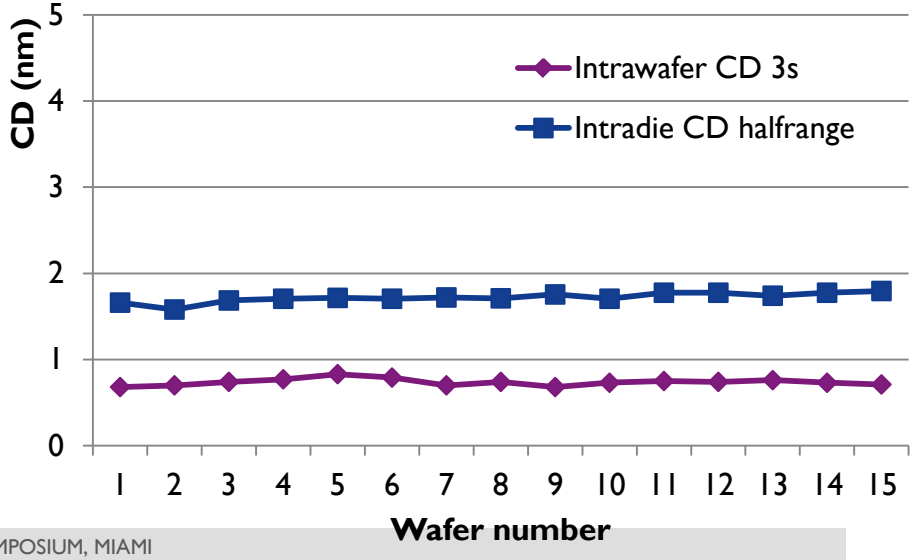
- CD data collected for **15-waferbatch** exposed in wk 35
  - Full field and wafer coverage
  - Dual chuck mode on NXE:3100
  - **Exposure time was 3hr. 10min.** for 15-wafer lot at dose to size of 27nm LS
  - 27nmV LS CD data collected on Hitachi CG4000 – 15 points per die covering the entire 26 x 33mm exposure field
  - <4 metrology flyers per wafer



CD UNIFORMITY THROUGH WAFER BATCH FOR NXE:3100

- Average CD per wafer is stable through batch
- Error bars are +- 3s values per wafer ~5nm 6s
- Split into intrawafer and intradie CD
  - Intradie CD is main contribution to CD fingerprint (<2nm halfrange, without correction)
  - Intrawafer CD 3s values are smaller (<1nm)



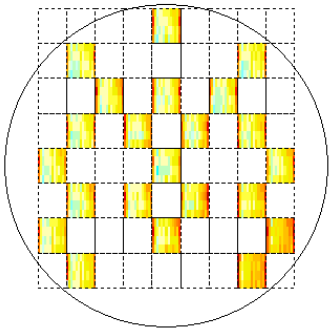


ADT – NXE:3100 CDU COMPARISON

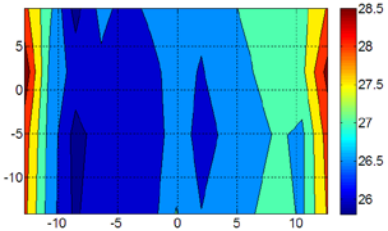
- **No corrections for reticle or process contribution**
  - NXE has larger exposure field and larger wafer coverage

27nm V LS	ADT	NXE:3100
Average CD	26.9nm	26.3nm
CD 3s	2.3nm	2.7nm
Intrawafer 3s	1.0nm	0.7nm
Intradie 3s	2.1nm	2.0nm

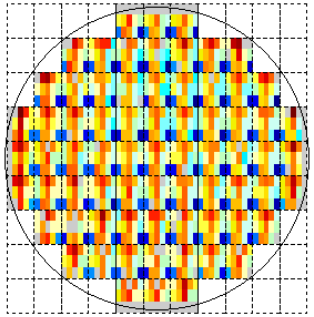
ADT wafer



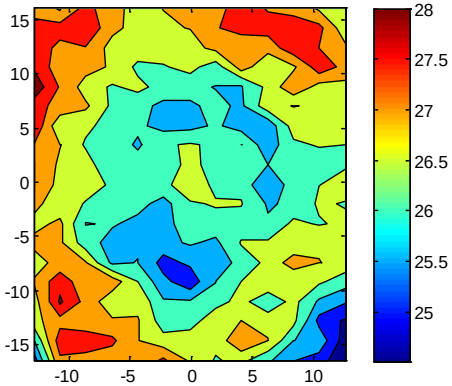
ADT intrafield



NXE wafer



NXE intrafield



For 27nm V LS – similar uniformity on ADT as NXE

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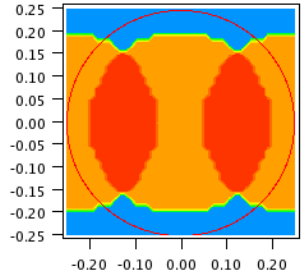
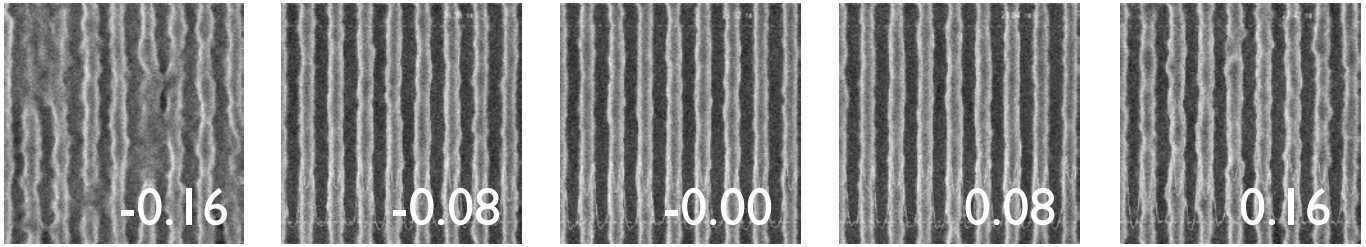
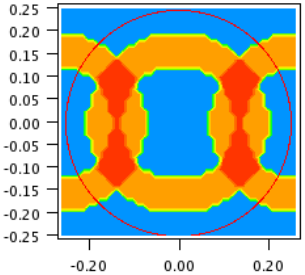
NXE:3100 RESOLUTION ENHANCEMENT FOR OFF-AXIS ILLUMINATION

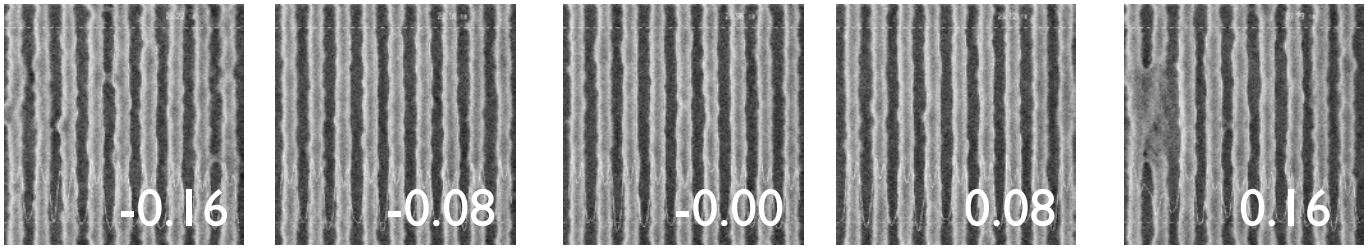
Conventional 27nm V LS



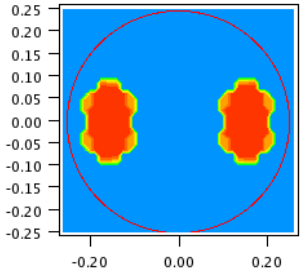


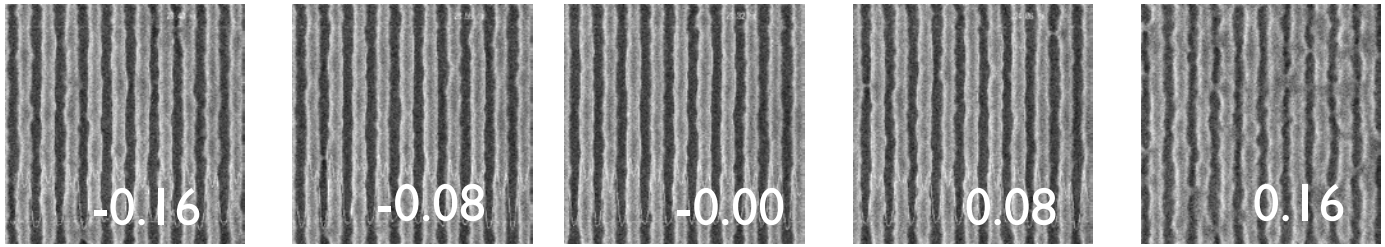
Annular 25nm V LS





X-Dipole 22nm V LS





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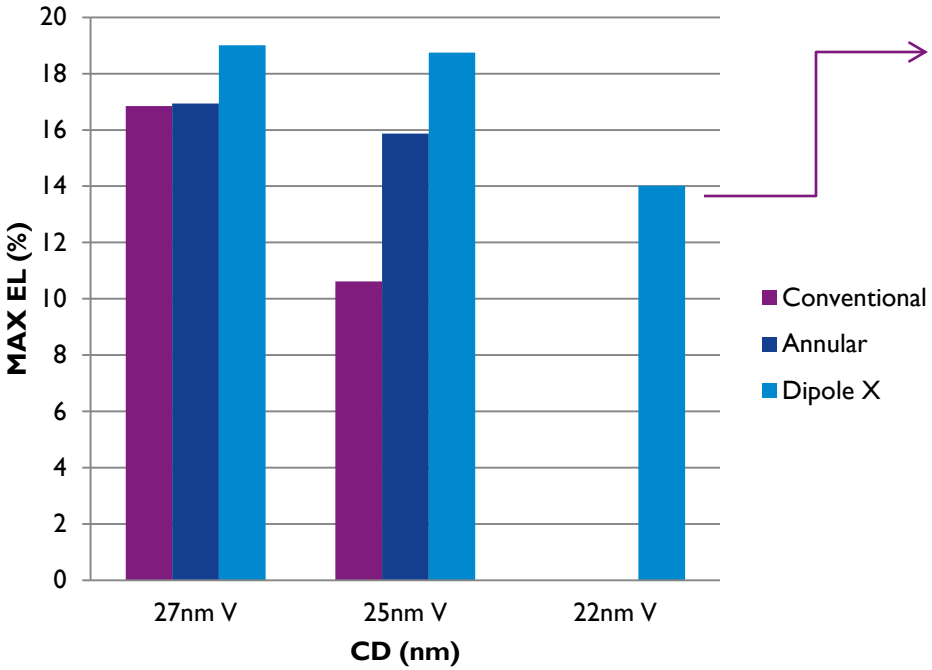
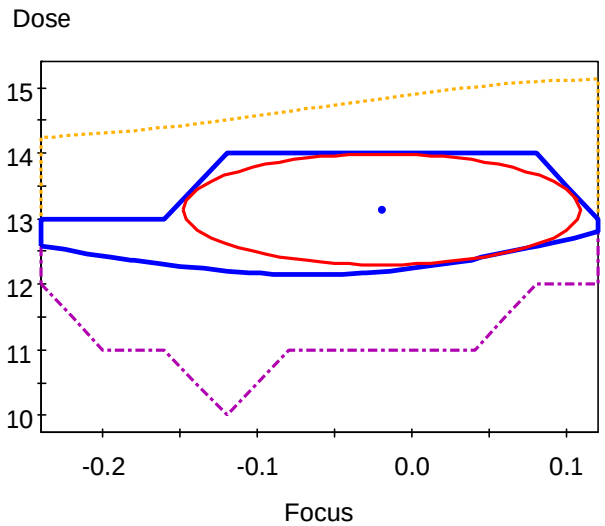
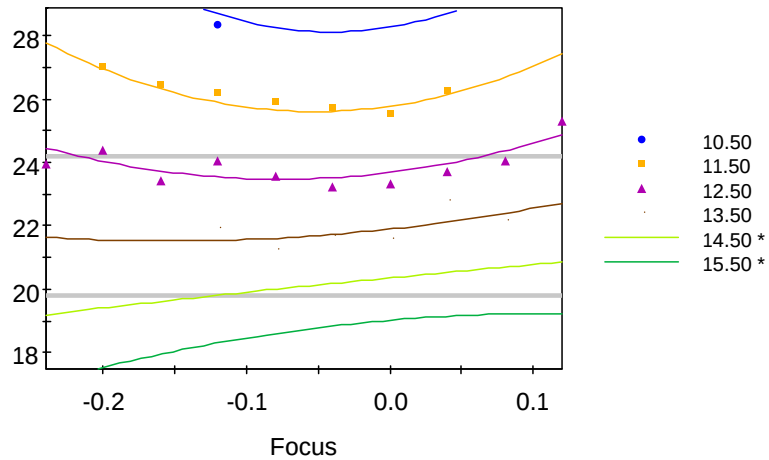






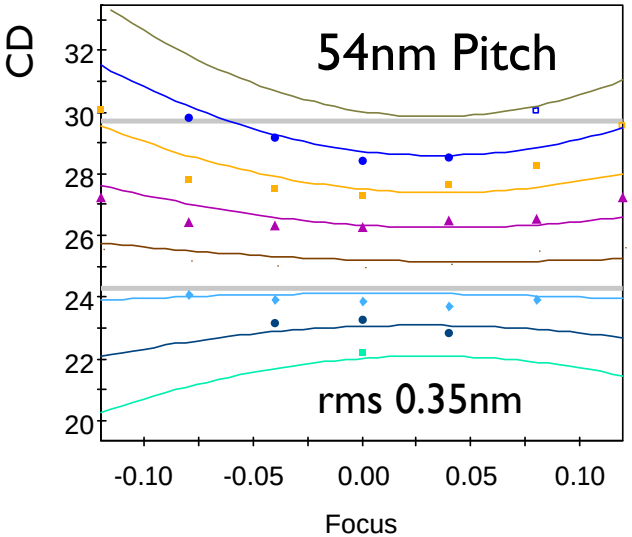
Small process window for 22nm LS using dipole illumination – Limited by process

MODELING OF OFF-AXIS ILLUMINATION IN RIGOROUS SIMULATION IN S-LITHO FOR EUV

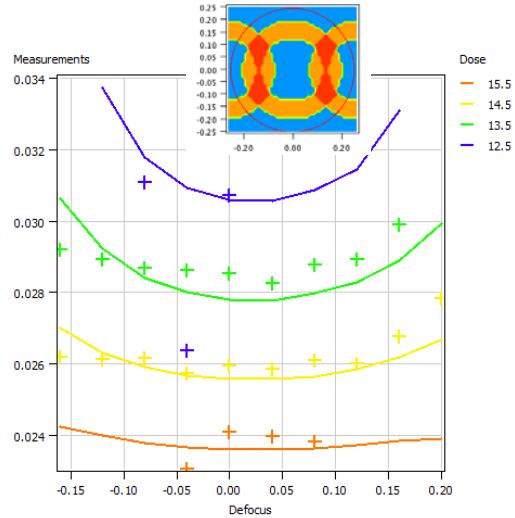
Model calibrated vs. ADT

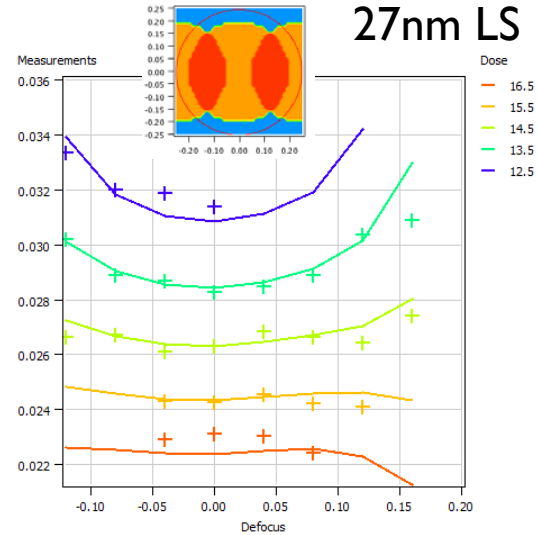
Solid line = model

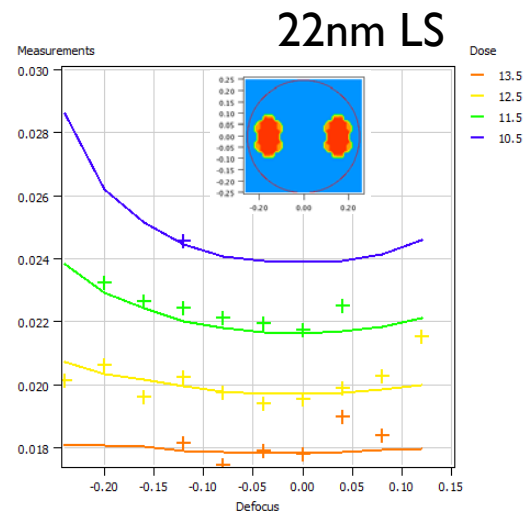
Points = experiment



Adapt Dill C (dose calibration)







2010 ADT resist model with adapted Dill C also predicts NXE:3100 off-axis FEMs

2010 EUVL Symposium, E. Hendrickx

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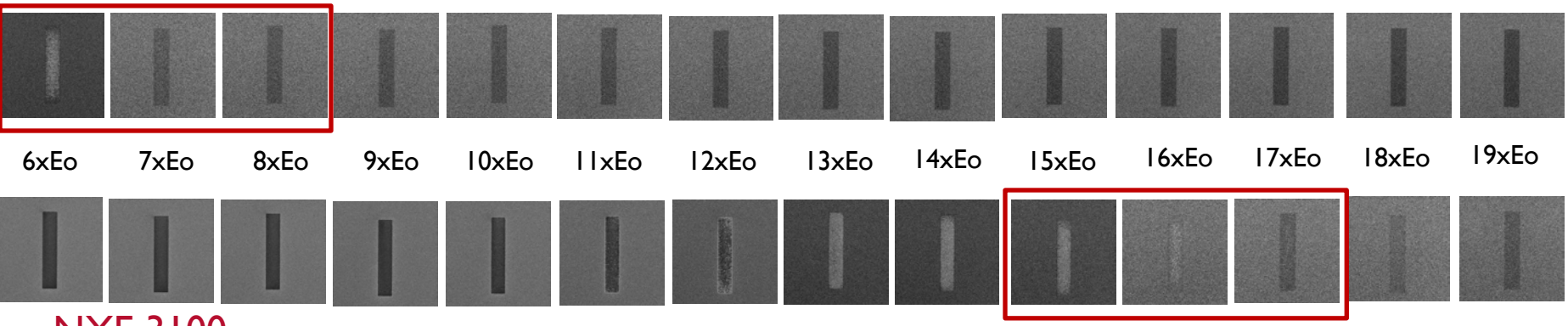
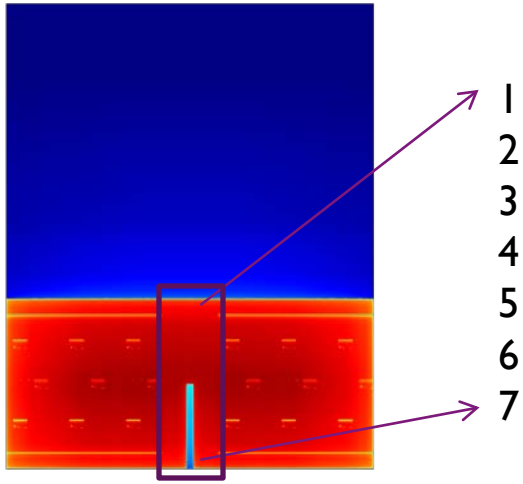
FLARE - ADT VS NXE:3100

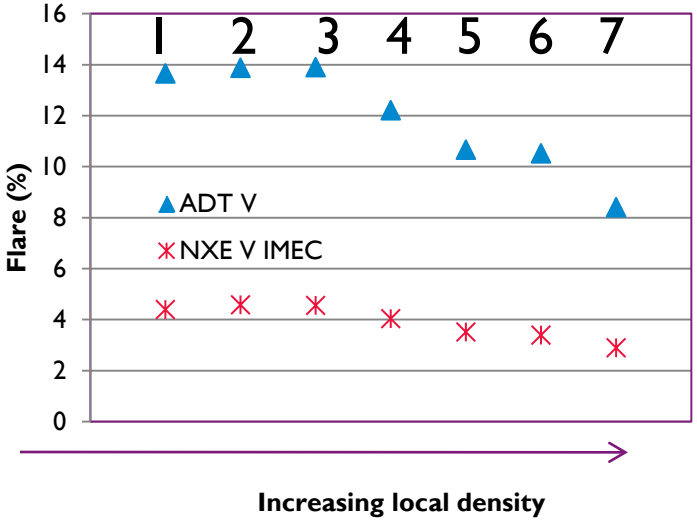
EUV ADT



NXE 3100

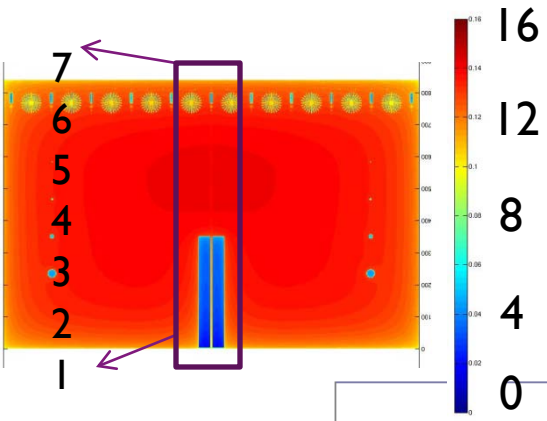
Flaremap of imec flare mask



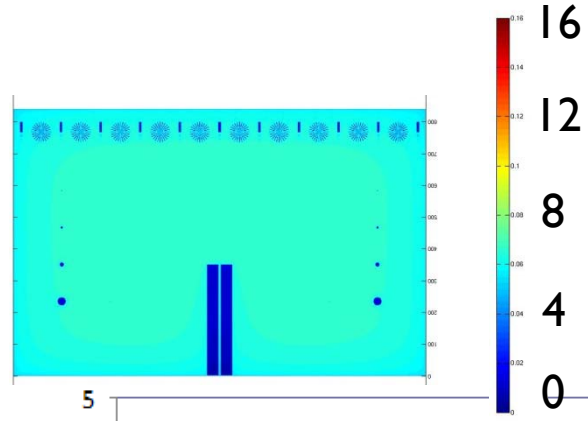


Total flare is reduced 14% to ~5%

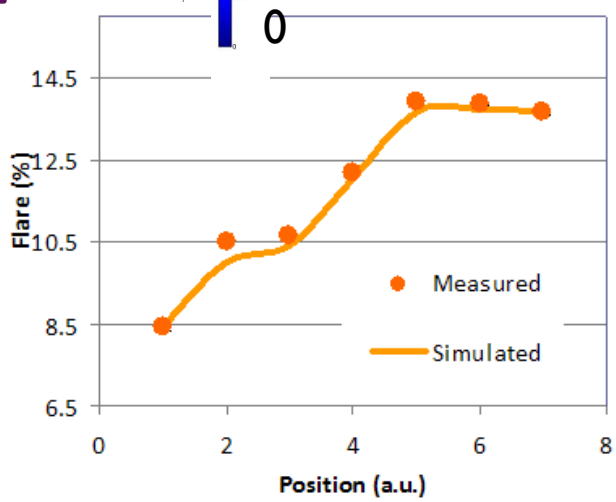
FLARE MODELING ON ADT AND NXE:3100

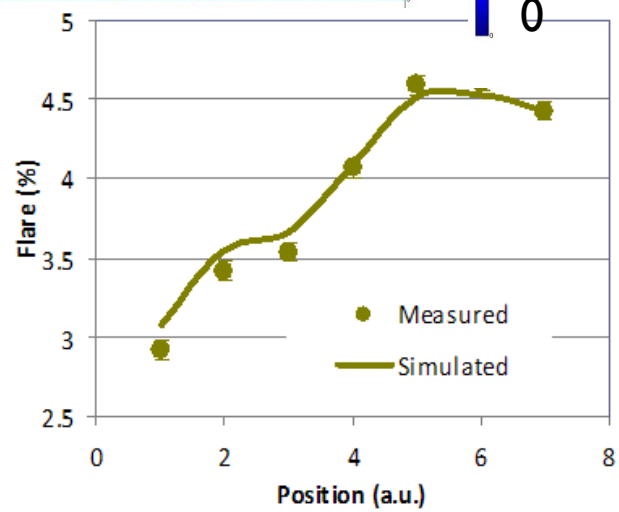


ADT flaremap



NXE flaremap





ADT flare was modeled by 3 EDA's in imec litho program
NXE:3100 flare modeling exercise ongoing

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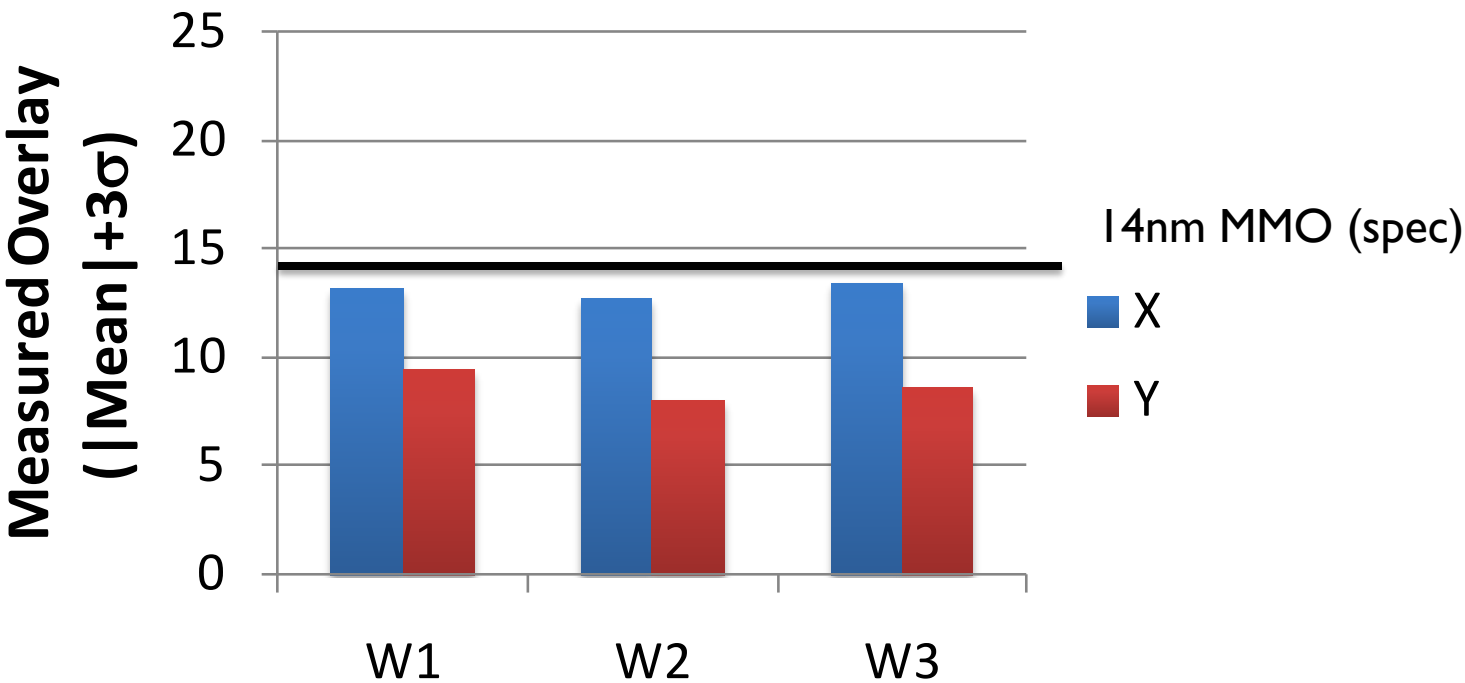
MAIN EUV SPECIFIC SCANNER CONTRIBUTIONS TO OVERLAY

CONTRIBUTION	EFFECT ON OVERLAY	ADT SOLUTION
Reticle (clamp) flatness (due to *non-telecentricity*)	Intrafield distortion	Reticle clamp cleaning and polarity change
Vacuum purge chamber and *thermal* stability	Wafer grid and intrafield stability	Dummy wafer and CPE corrections
Wafer clamping (*electrostatic* chuck)	Wafer grid stability	Zone alignment

Earlier work on ADT showed EUV specific contributions to overlay and suitable mitigation

J. Hermans 2010 SPIE 7636

ADT OVERLAY ON ETCHED REFERENCE WAFER USING ZONE ALIGNMENT AND DUMMY WAFER



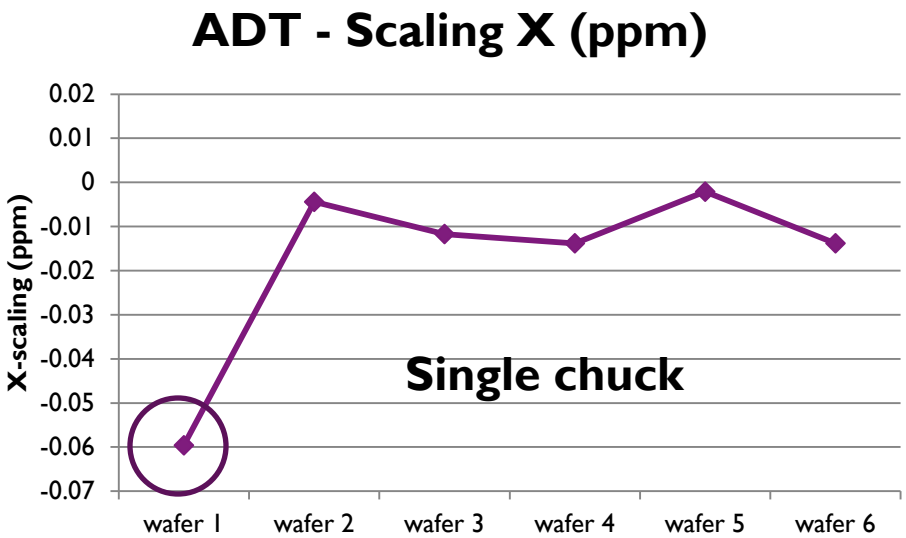
Reference grid from XT:1450

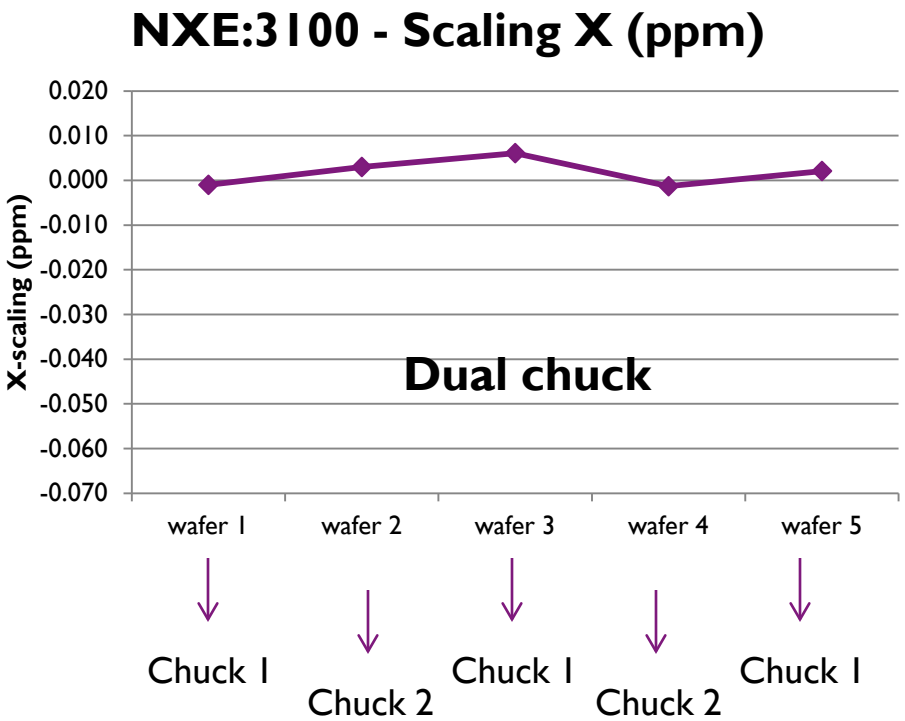
MMO=Matched Machine Overlay (XT:1900Gi to XT:1400E)

After improvements, overlay performance of ADT is within matching specification for immersion lithography

J. Hermans 2010 SPIE 7636

OVERLAY ON ETCHED REFERENCE WAFER ON ADT AND NXE

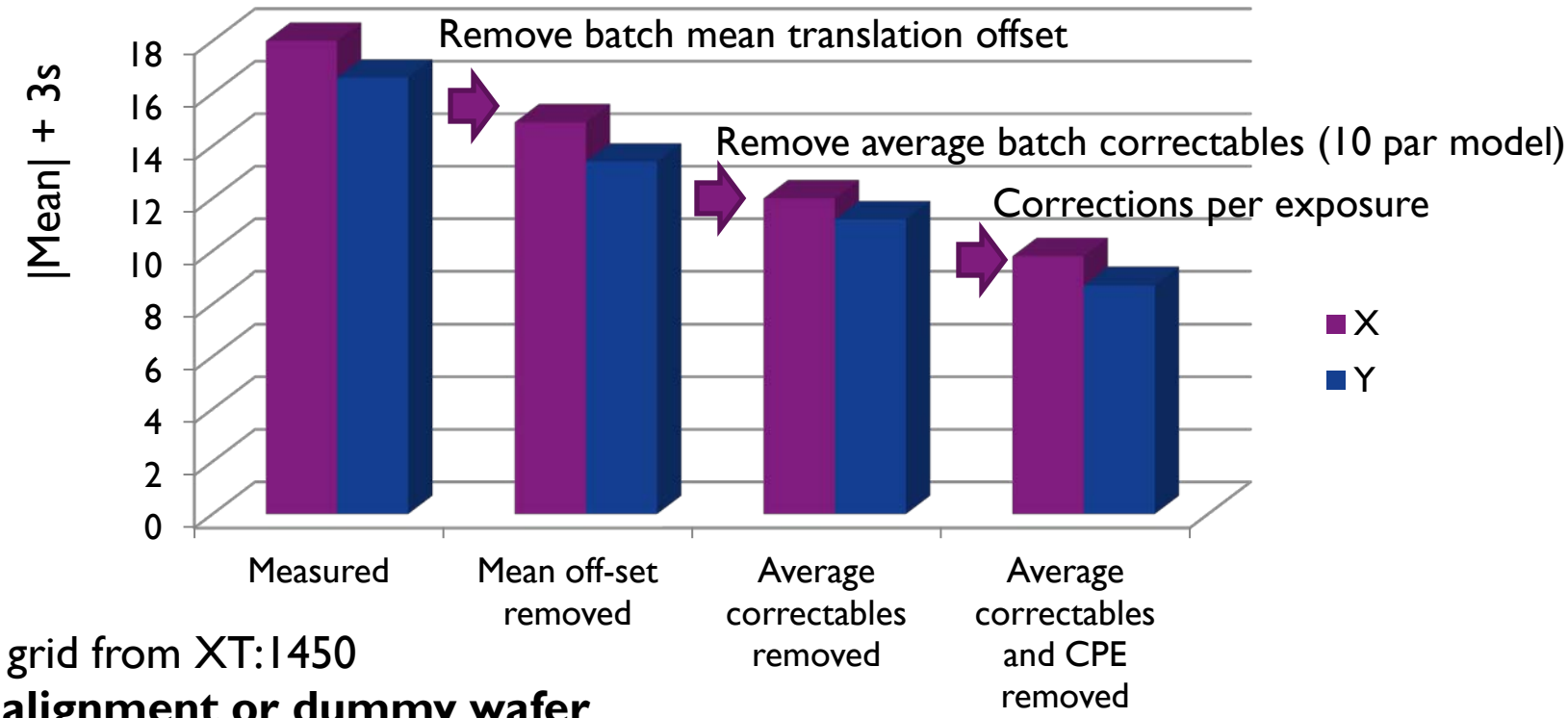




Reference grid from XT:1450
ADT: 25 fields – 26 x 24mm
NXE: 71 fields – 26 x 33mm

X-Scaling through batch on ADT shows 1st wafer effect
NXE:3100 shows better control (dual chuck!)

MODELING OF FIRST 5-WAFERLOT ON NXE:3100 - UNMATCHED



Reference grid from XT:1450

No zone alignment or dummy wafer

Dual chuck mode

Modeling of raw overlay data shows that corrections per exposure are needed for <10nm MMO vs. 1450 dry tool

CONTENTS

EUV ADT & NXE:3100 installation

NXE:3100 vs. EUV ADT

- 27nm LS image formation
- Off-axis illumination
- Flare
- Overlay

Conclusions

CONCLUSIONS

- NXE:3100 has been successfully installed
- First NXE:3100 CD and overlay data look promising

	ADT	NXE:3100
Throughput	~3 hours/wafer	14 min/wafer
IF CDU of 27nm LS Uncorrected	2.1nm	2.0nm
Ultimate resolution	25-27nm	20-22nm (dipole)
Flare	~14%	~5%
Overlay	~14nm shown Dummy wafer Corrections per exposure Zone alignment	<10nm feasible Only corrections per exposure Dual chuck

EUV ITEMS FOR THE NEXT MONTHS – STRAIGHT FROM FAB

(1) After 3 years of ADT, exposing a 15-waferbatch felt fantastic, but...

Can we do it day after day after day after day?

60% NXE uptime is required, as for ADT

(2) Clear resist improvements have been made over the last years, but...

Line edge roughness has to be reduced

(3) **Cleanliness is required! Particle mitigation is not trivial!**

Particles in reticle ML → wafer defect...

Particles deposited on reticle → wafer defect...

Particles on reticle backside → loss of overlay control...

Particles on wafer backside → focus spots...

ML defect mitigation: R. Jonckheere, Session 9

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Xtreme

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