

# EUV BASELINE PROCESS OPTIMIZATIONS FOR NXE:3100 EVALUATION

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## Abstract

The advent of ASML's NXE:3100 EUV pre-production tool at imec brings EUV lithography another step closer to production. For optimal evaluation of the scanner and to assess the current EUV process status, a first evaluation and optimization of the baseline process on TEL's CLEAN TRACK™ LITHIUS Pro™ -EUV is run. Apart from the standard track process optimization, also novel hardware and processes are evaluated like smoothing and backside cleaning. The process performance is evaluated on CD uniformity, pattern collapse and line width roughness.

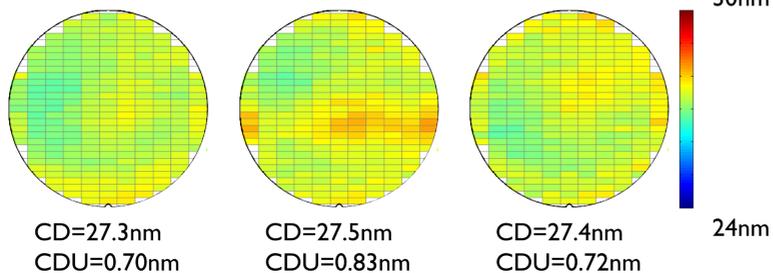
## CD uniformity

Cluster monitoring structure: 27nm L/S. Repeatability test run inline using a single scanner chuck.

3 wafers, single unit processing.

CD measured by scatterometry.

CDU=3\*stdev.



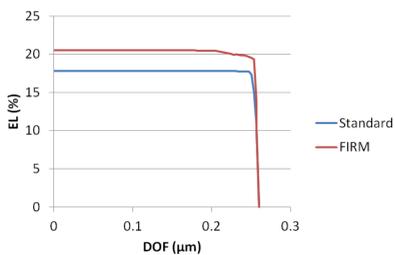
Maximum 0.2nm CD offset between wafers.

Minor fingerprint differences, CDU 0.7-0.8nm 3σ.

## Pattern collapse

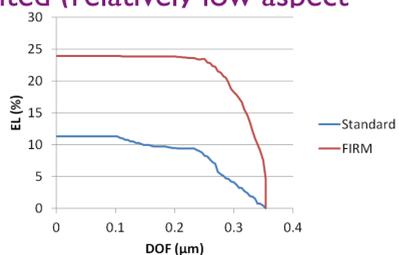
To reduce pattern collapse, rinse with FIRM™ Extreme after development is evaluated.

Process window for 27nm L/S



PW improvement with FIRM™ Extreme on the baseline process is limited since pattern collapse itself is limited (relatively low aspect ratio).

Process window for 32nm L/S with 75nm resist coating thickness

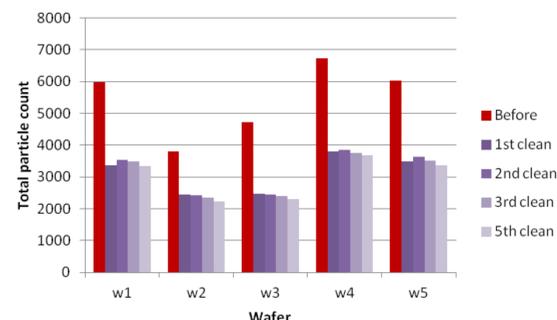


FIRM™ Extreme dramatically reduces pattern collapse on higher aspect ratio process. Large process window improvement.

## Wafer backside cleanliness

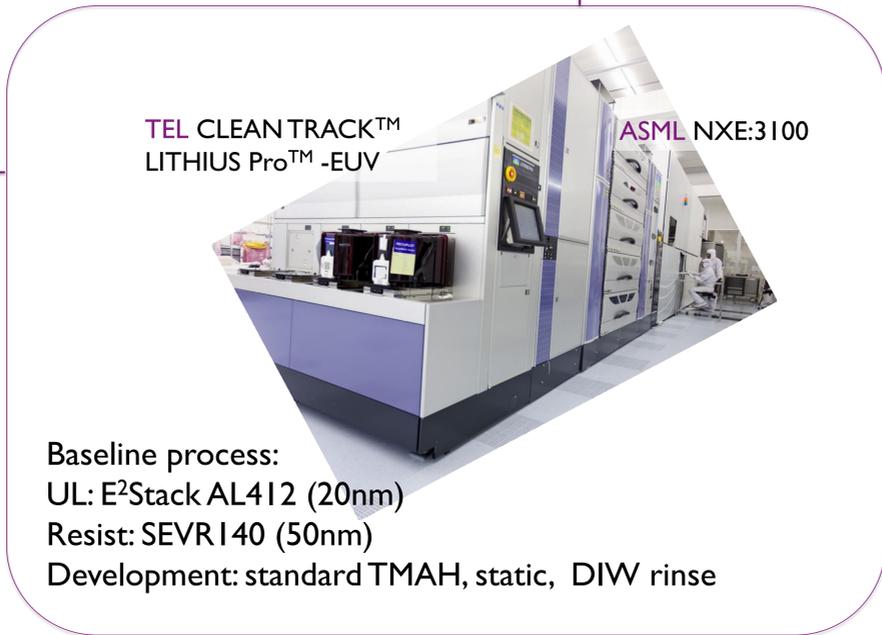
To avoid long scanner down times for chuck cleaning: keep the chuck clean by cleaning the wafer backside in the track just before exposure.

5 wafers with long process history on different tools cleaned 5 times. Backside particles measured.



First clean removes a considerable amount of defects.

Repeated treatment cannot improve the defectivity further. This could indicate that the remaining defects are scratches or indentations in the backside of the Si wafer.

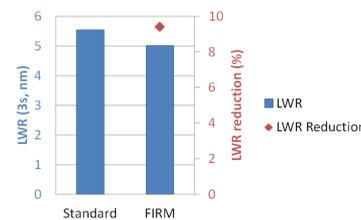


Baseline process:  
UL: E<sup>2</sup>Stack AL412 (20nm)  
Resist: SEVR140 (50nm)  
Development: standard TMAH, static, DIW rinse

## Roughness

Smoothing by FIRM™ Extreme rinse after development.

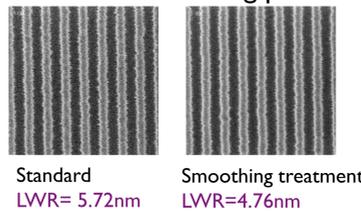
LWR evaluation for 27nm L/S Standard and FIRM process



With FIRM™ Extreme: LWR improvement up to 10%, in line with previous testing of similar rinse processes.

Track smoothing process for lines and CH smoothing:

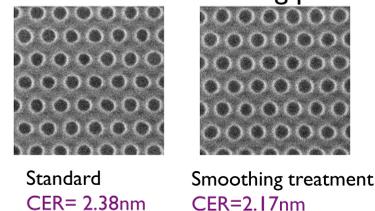
LWR evaluation for 28nm L/S Standard and smoothing process



After first smoothing process optimizations on L/S: LWR reduction by 17% (high/mid frequency range). No detrimental effect on low frequency roughness.

CH seem more regular and uniform but further analysis is required.

Initial result for CH smoothing Standard and smoothing process



## Conclusion

The first NXE baseline process testing revealed no unexpected issues. Process performance is in line with expectations, and first process optimization tests look promising.

BST helps to reduce backside particles and is used as a standard process step before exposure.

The baseline process has good CDU performance (<1nm 3sigma).

FIRM™ Extreme rinse reduces pattern collapse and improves LWR by almost 10%.

Smoothing process: results on dense L/S look promising (17% LWR-smoothing).

First result on CH looks interesting and will be explored further.