EUV resist material performance, progress and process improvements at imec

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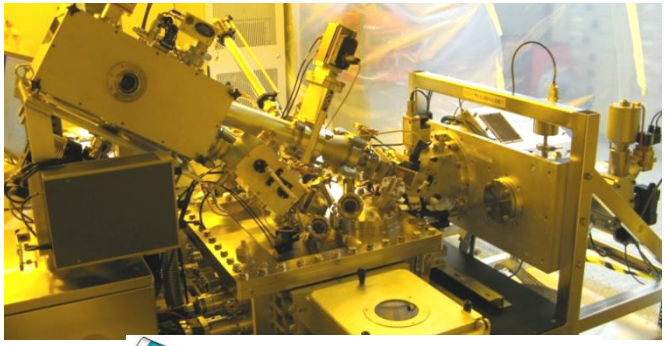
International EUVL Symposium, 17- 20 Oct 2010, Kobe

INTRODUCTION :
Project goal and tool set

ASML EUV ADT (NA=0.25)

Outgassing Tool (EUV Technology)

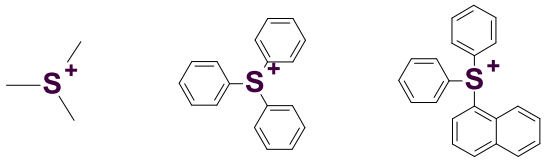


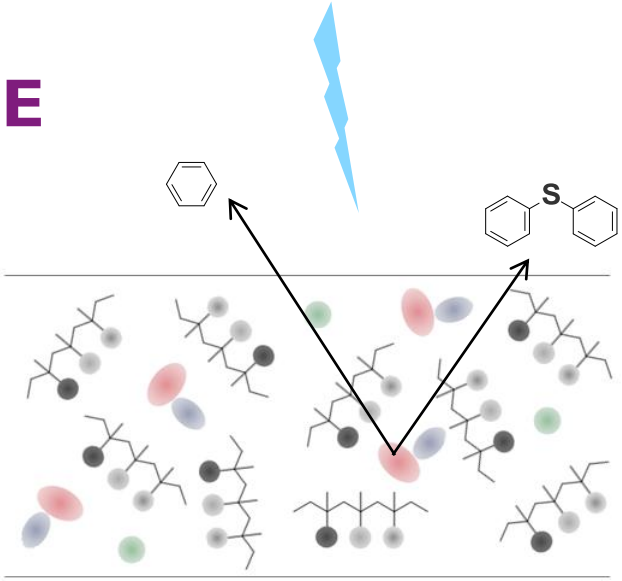
- Resist screening and benchmarking on ASML EUV ADT
  - to follow up the resist progress and to prepare for a process for NXE-3100 tool
  - NXE:3100 requirements : 27nm LS
- EUV resist outgassing & contamination
  - qualification of resist (RGA and WS plate)
  - Gain fundamental understanding on relationship with resist chemistry (poster RE-P04)

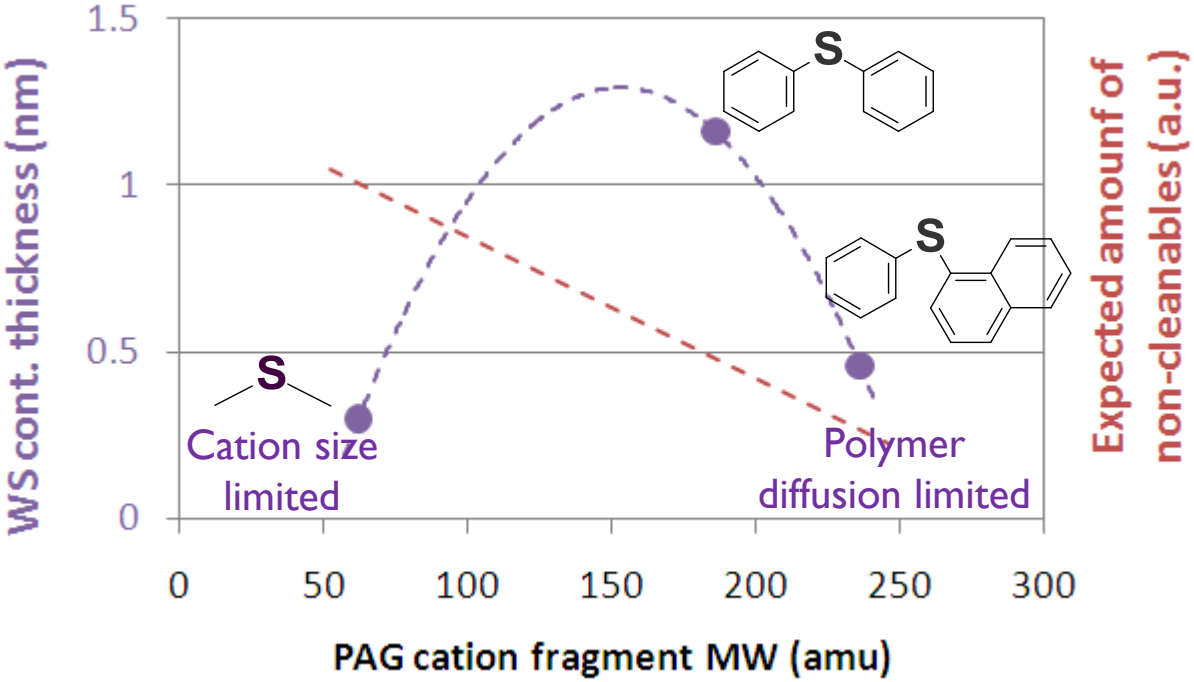
OUTGASSING : PAG TYPE

PAG

Several PAG cations are tested towards WS contamination







Both small PAG cations as well as very heavy PAG cations give lower WS contamination, however it is expected that for S-containing cations the high-MW will result in less non-cleanable contamination

Poster RE-P04
I. Pollentier

OUTLINE

Introduction

Lithographic screening

- Resist screening
- Underlayer screening

Benchmarking

- Lithographic performance
- Process defectivity

Process improvements

- TBAH
- FIRM

RESIST PERFORMANCE TARGET FOR 2010 ON ADT (NA=0.25, σ=0.5)

Resist screening

- outgassing testing (RGA)

- Litho performance screening
  - Sensitivity, LER, ultimate resolution
  - Z-factor

$$\text{Imec nZ} = \frac{\text{Material Z-factor}}{\text{IMEC Target Z-factor}}$$

  - Process windows at low and high flare for dense and iso lines

Benchmarking (track)

- Line-end shortening, through pitch
- 32nm Contact holes
- Process defectivity

Target	H1 2010	H2 2010
Ultimate resolution-resolved HP	26nm	26nm
Resolution Line/Spaces HP(nm) DOF for 1:1 L/S at 10% EL Maximum EL	30nm 120nm >15%	28nm 100nm >10%
Resolution Iso Lines (nm) DOF for iso Line at 10% EL Maximum EL	30 100 >15%	28 80 >10%
LER on 30nm L/S (nm 3sig)	4nm	3.5nm
Dose-to-size at 30nm L/S (mJ/cm^2)	<15	<15
Resolution Contacts 1:1 (nm) Max DOF Max EL	32nm >120nm >10%	30nm
Resist Thickness (nm)	50-60nm	50nm

* Z-factor : Thomas Wallow, et al, SPIE 69211F (2008)

(Resolution ; nm)^3 * (LER; nm)^2 * (Sensitivity; mJ/cm^2) ~ Constant [Z-factor (mJ*nm^3)]

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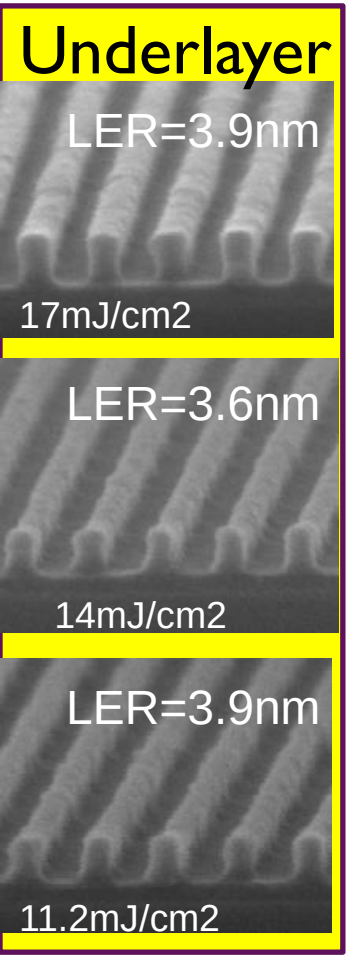
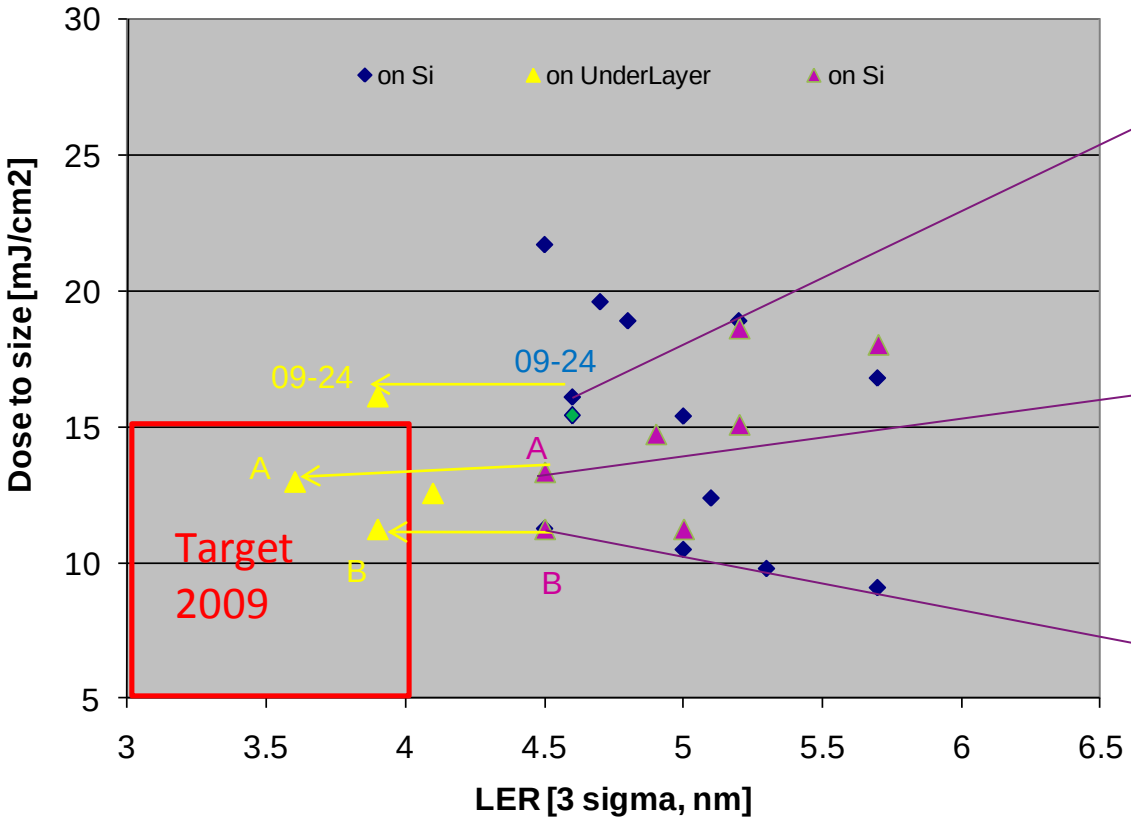
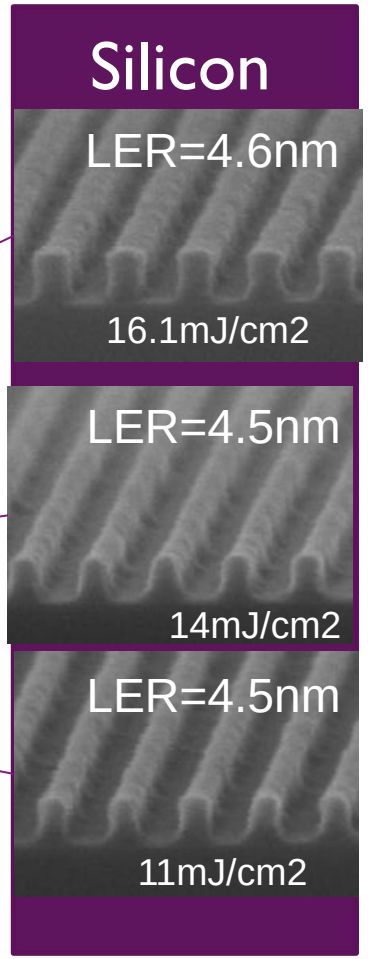
RESIST STATUS in 2009
sensitivity vs LER for 32nm LS



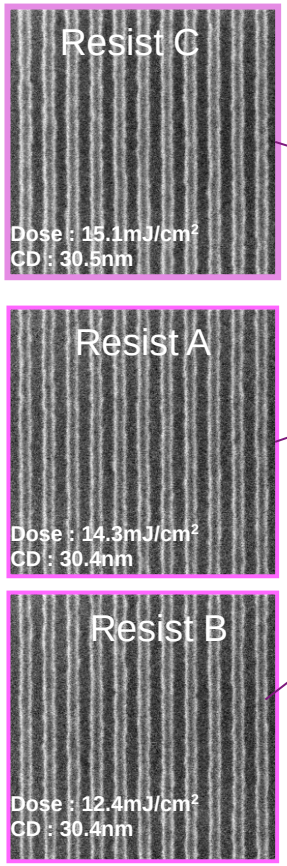


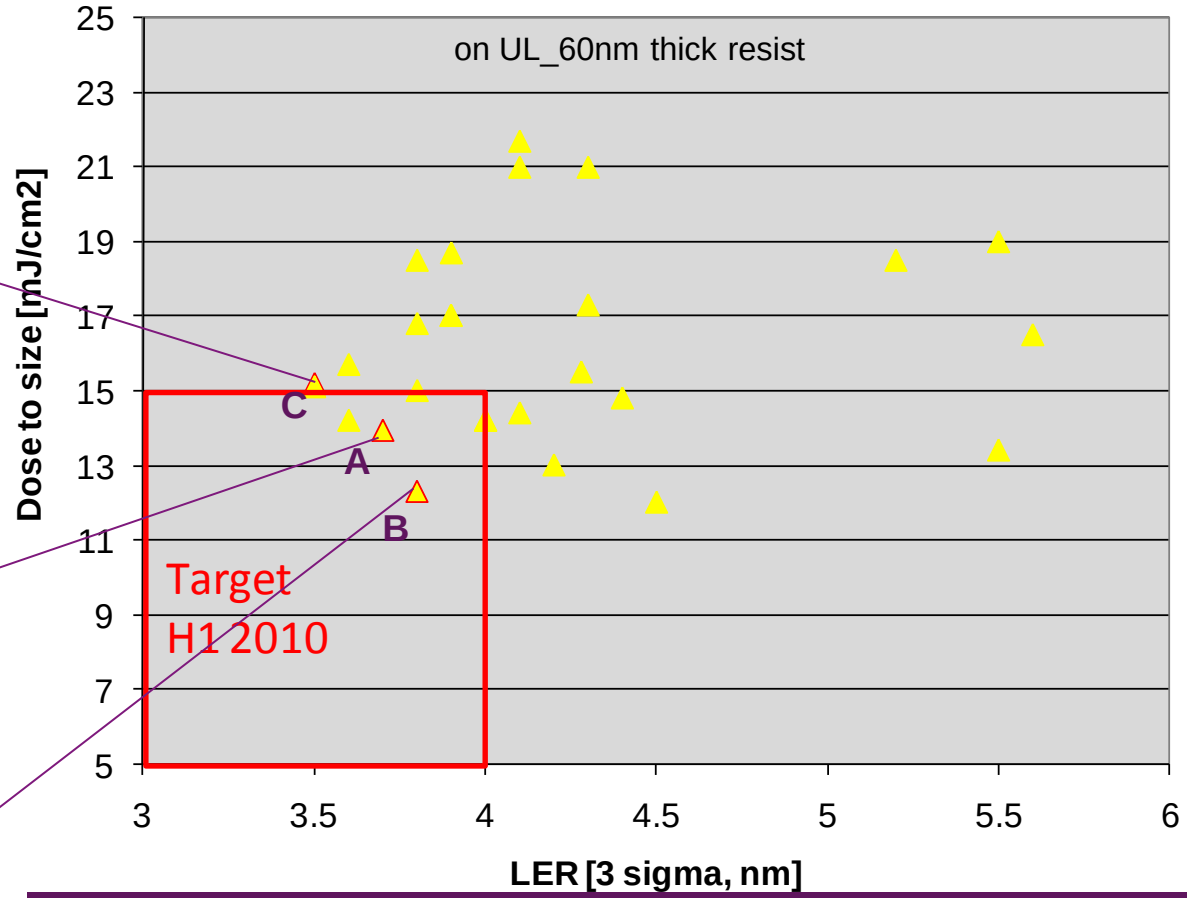


Improvement in LER with 15-20% by the use of underlayer
All resist screening carried out on Underlayer

Sensitivity vs. LER for 30nm LS on underlayer

Resist thickness 60nm





Some materials meeting the 2010 H1 target for sensitivity and LER
Resist A,B,C materials installed on track for detailed benchmarking

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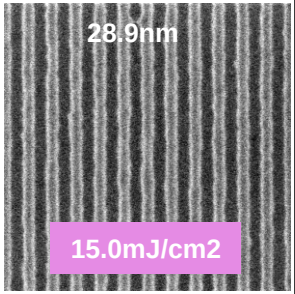
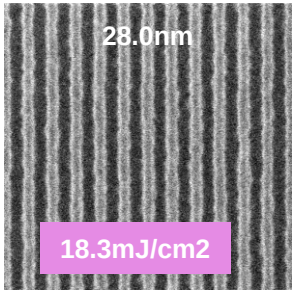
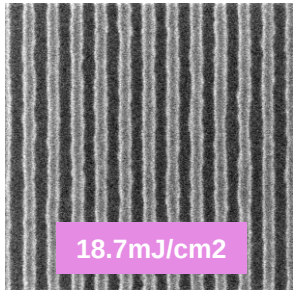
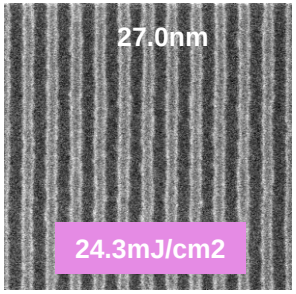
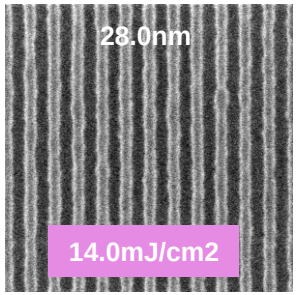
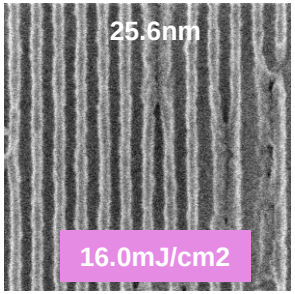
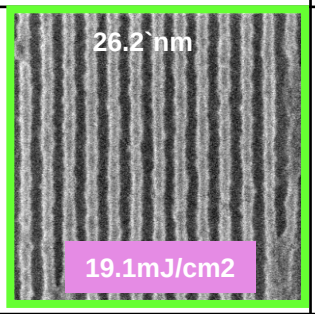
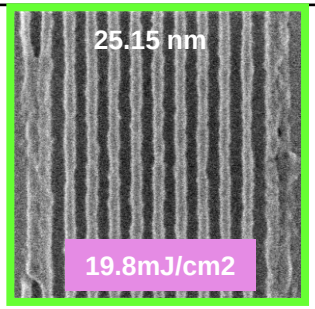
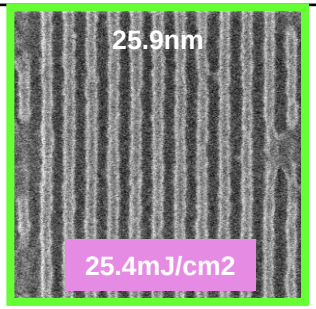
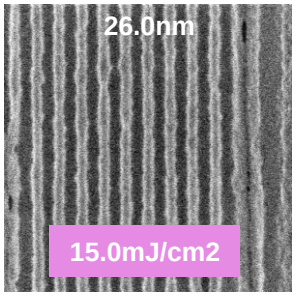
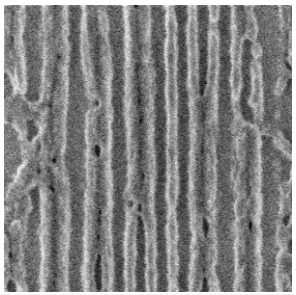
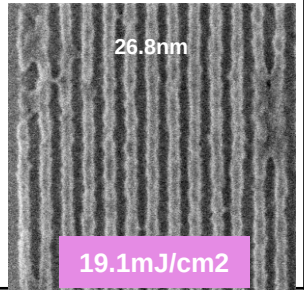
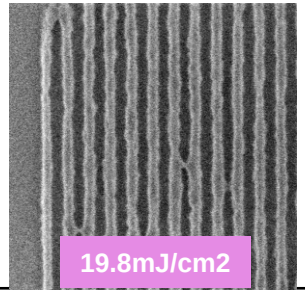
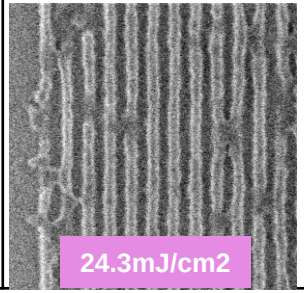
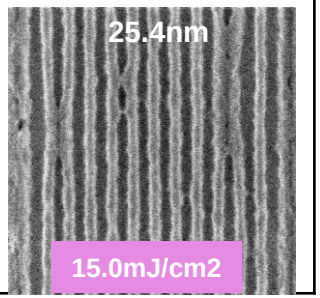
RESIST SCREENING : ULTIMATE RESOLUTION

60nm resist thickness

Resolution	ADT10-16	ADT10-02	ADT10-05	ADT-09-58	ADT10-18
28nm HP					
26nm HP					
25nm HP					

Feasibility of 26nm HP resolution in 3 resists at 60 nm FT
Pattern collapse is major resolution limiting factor

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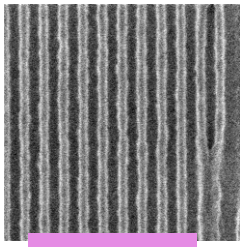
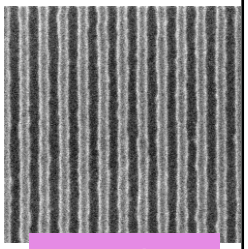
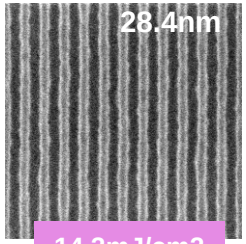
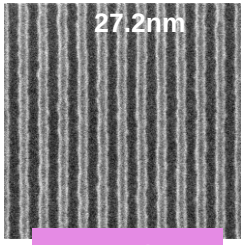
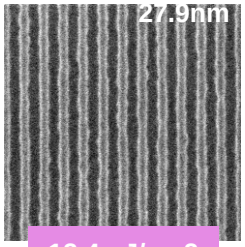
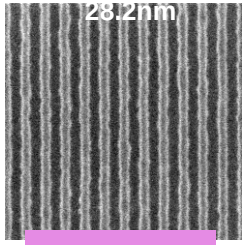
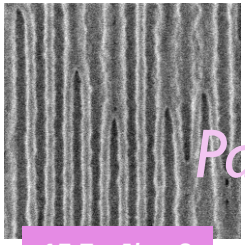
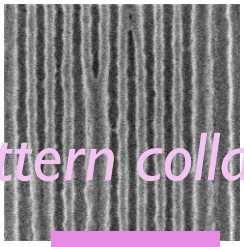
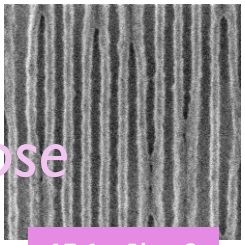
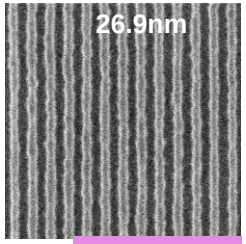
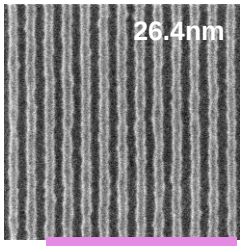
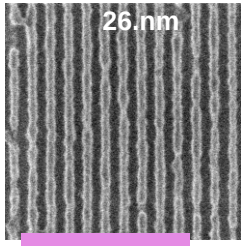
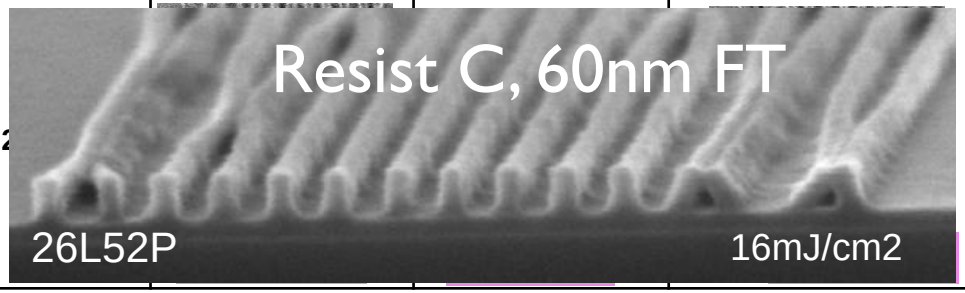
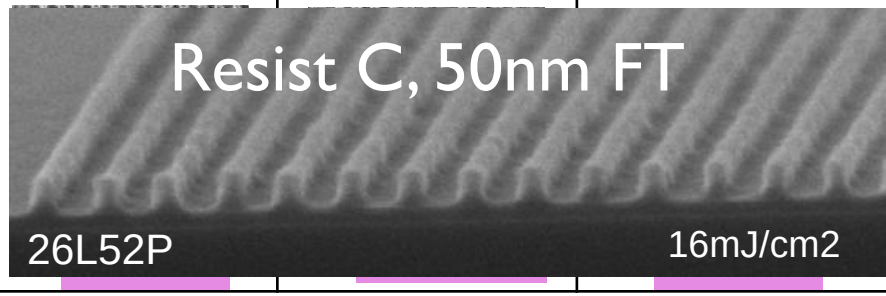
3 RESIST FOR BENCHMARKING

ULTIMATE RESOLUTION, 60NM VS 50NM RESIST THICKNESS

Resolution	Resist A 62nm thickness	Resist B 62nm thickness	Resist C 60nm thickness	Resist A 50nm thickness	Resist B 50nm thickness	Resist C 50nm thickness
28nm HP	 15mJ/cm2	 12.4mJ/cm2	 28.4nm 14.2mJ/cm2	 27.2nm 14.3mJ/cm2	 27.9nm 12.4mJ/cm2	 28.2nm 15.2mJ/cm2
26nm HP	 15.7mJ/cm2	 13mJ/cm2	 15.1mJ/cm2	 26.9nm 15mJ/cm2	 26.4nm 13.0mJ/cm2	 26.nm 16mJ/cm2

Pattern collapse





Decrease resist thickness → reduced pattern collapse and improved resolution

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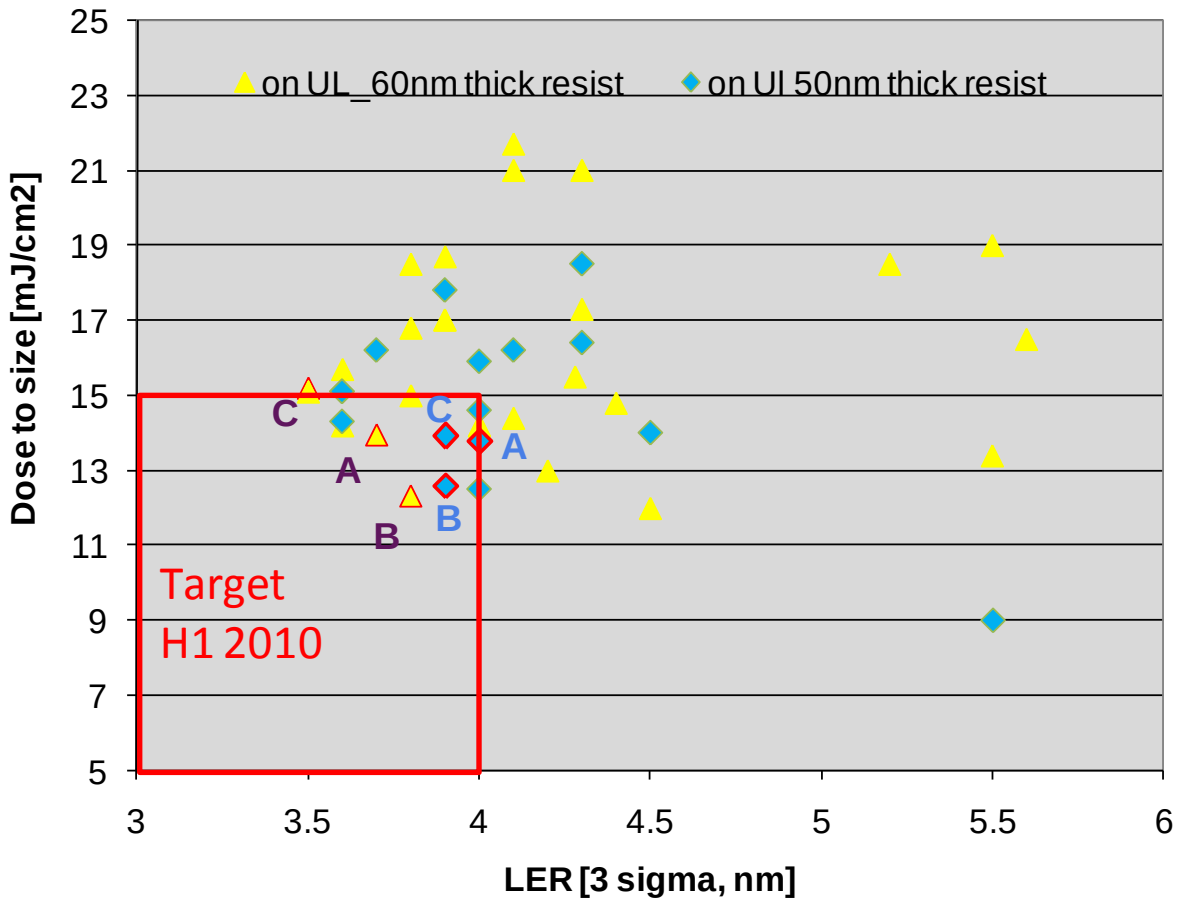
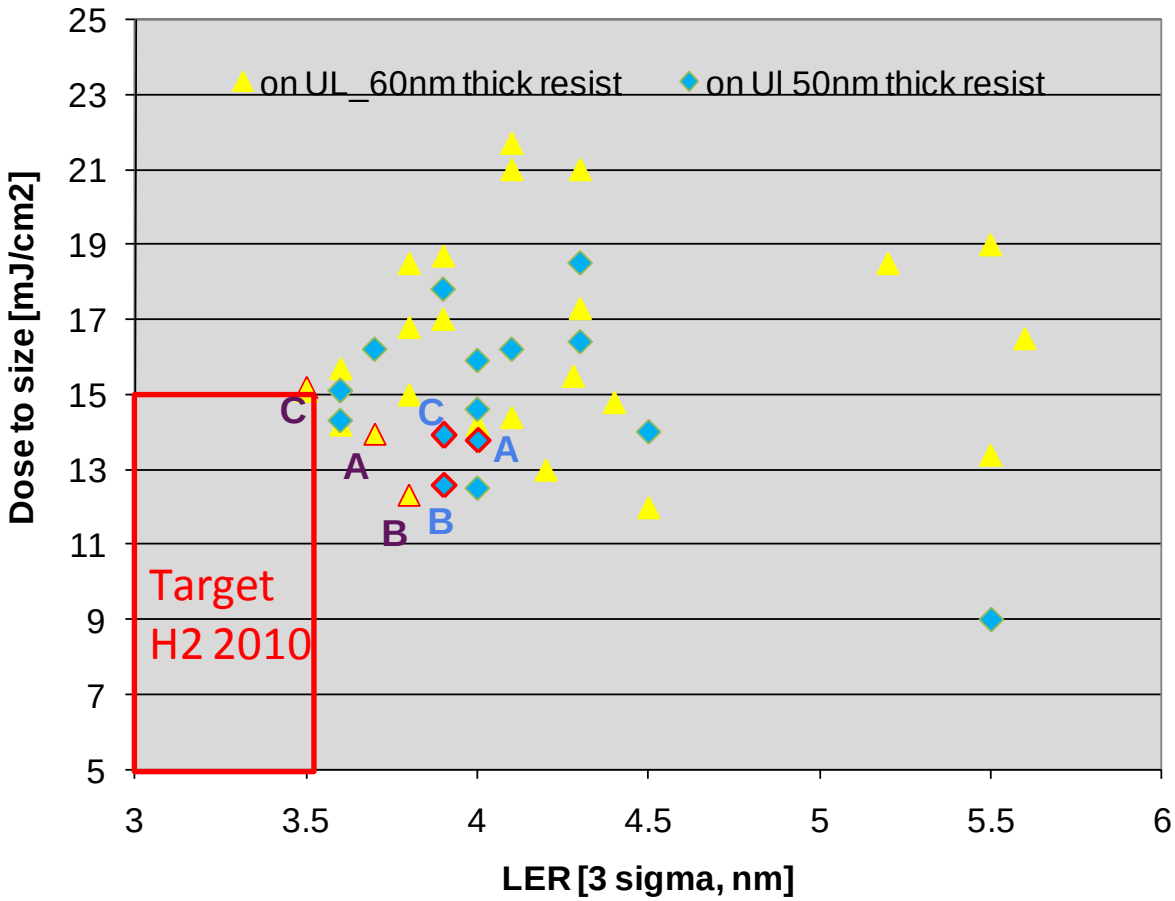
EFFECT OF RESIST THICKNESS
Sensitivity vs. LER for 30nm LS on UL



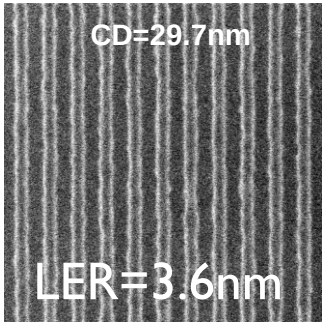
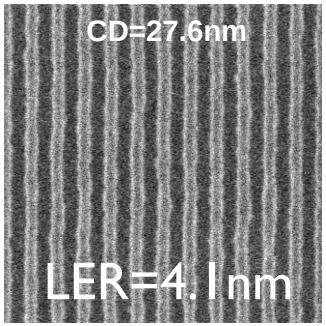
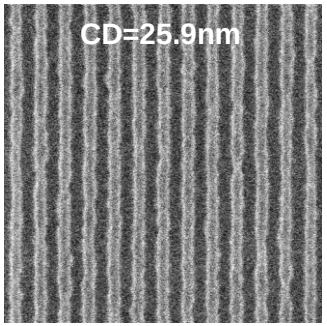
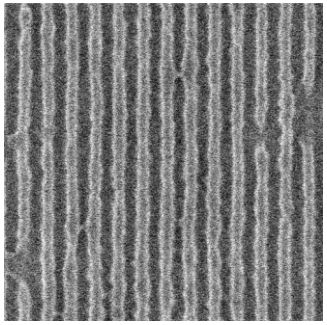
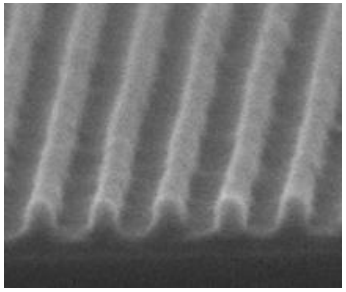
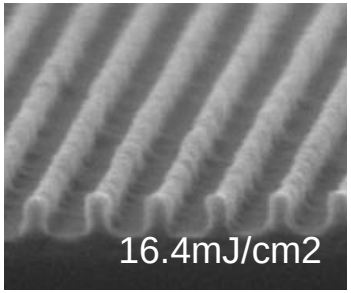
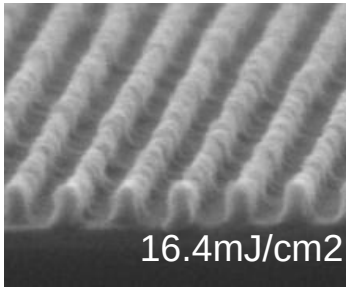
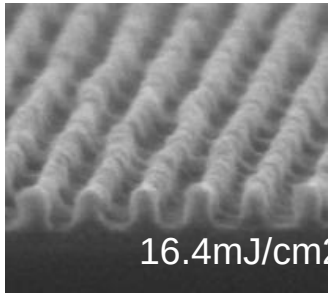
Reduction of resist thickness from 60nm to 50nm results in an increase in LER

EFFECT OF RESIST THICKNESS
Sensitivity vs. LER for 30nm LS on UL



Reduction of resist thickness from 60nm to 50nm results in an increase in LER, no resist meets the target spec of 3.5nm LER in 50nm thickness

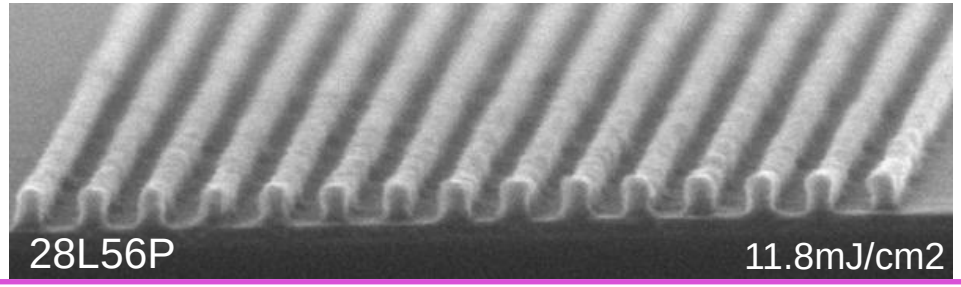
STATE-OF-THE-ART EUV RESIST PERFORMANCE ON ASML EUV ADT (0.25 NA)

30nm LS	*28nm LS*	*26nm LS*	*25nm LS*
			
30L60P @15 mJ/cm^2	28L56P @15.7 mJ/cm^2	26L52P @17.1 mJ/cm^2	25L50P @17.1 mJ/cm^2
			

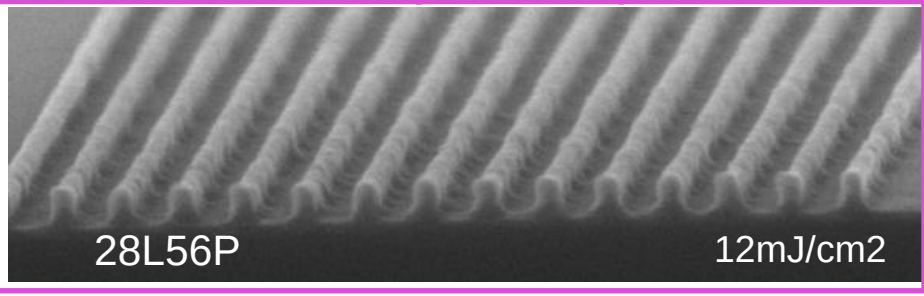
50nm FT

UNDERLAYER SCREENING
Profiles for 28nm LS (Resist B)

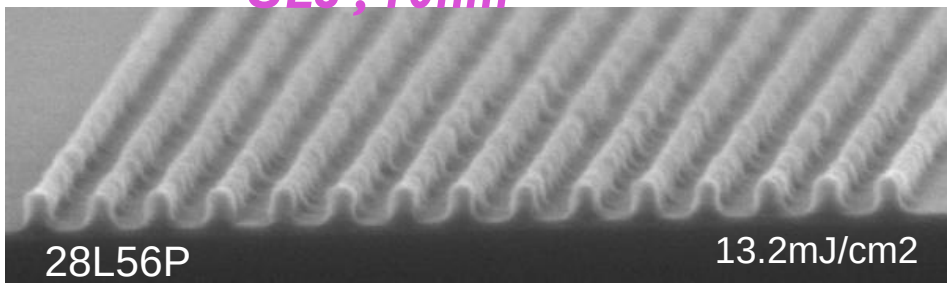
Standard UL(on track), 20nm



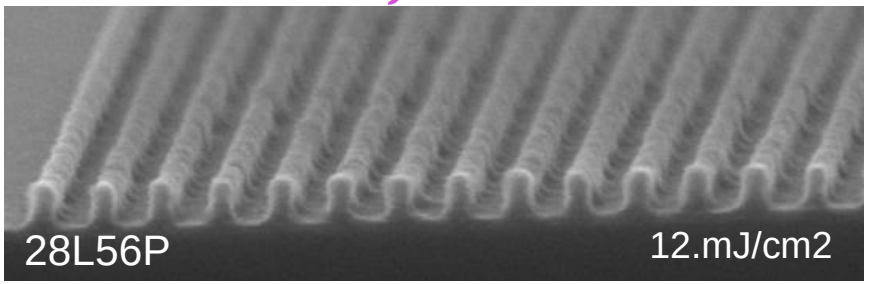
UL3 (on track), 10nm



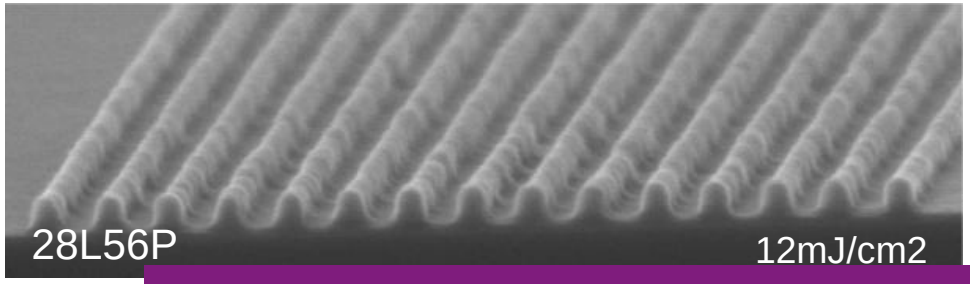
UL8 , 10nm



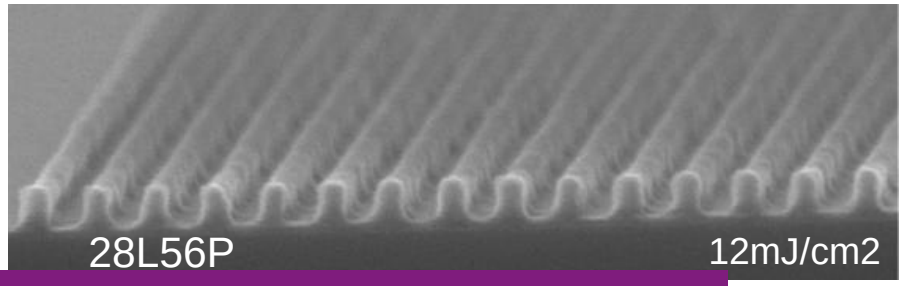
UL5, 10nm



UL12, 10nm



UL6, 10nm



Different Underlayer showed only minor differences in LER, and process windows
Standard UL and UL12 showed the lowest LER and reasonable PW

imec
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OUTLINE

Introduction

Lithographic screening

- Resist screening
- Underlayer screening

Benchmarking

- Lithographic performance
- Process defectivity

Process improvements

- TBAH
- FIRM

Benchmarking 28nm L/S, 50nmFT

	RESIST A	RESIST B	RESIST C
STD UL 20nm	14.3 mJ/cm^2 LER=4.2nm	12.4mJ/cm^2 LER=4.2nm	15.2 mJ/cm^2 LER=4.3nm
UL3 10nm	14.5 mJ/cm^2 LER=4.4nm	12.0mJ/cm^2 LER=4.6nm	15.2mJ/cm^2 LER=4.3nm

Resist B on std underlayer shows highest sensitivity and lowest LER

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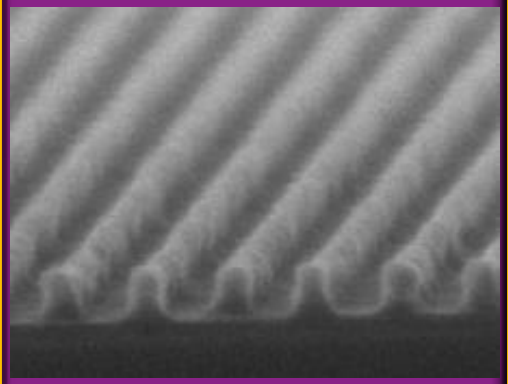
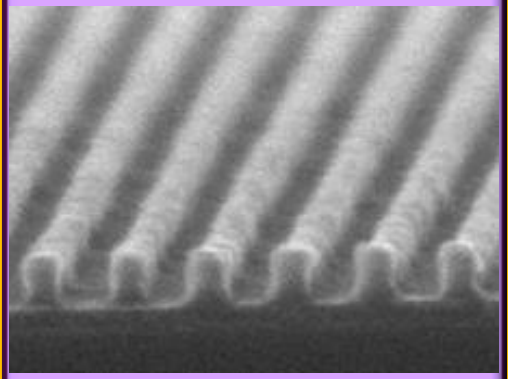
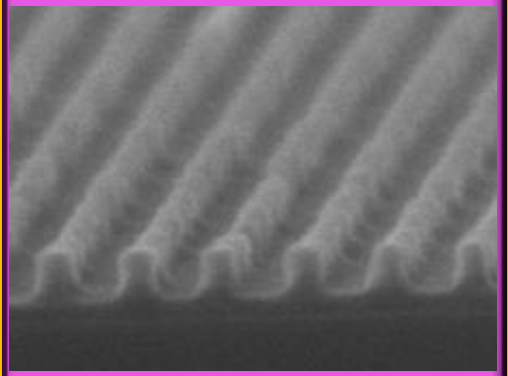
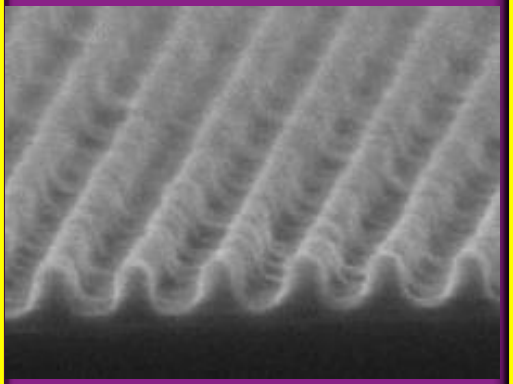
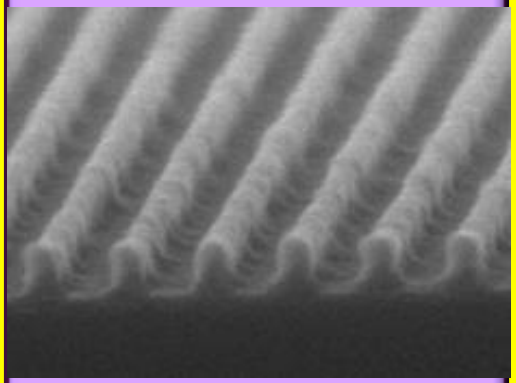
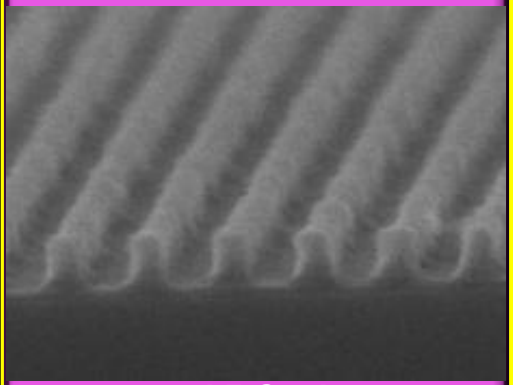
28nm LS CROSS SECTIONS

	RESIST A	RESIST B	RESIST C
STD UL 20nm	13.6mJ 	12.4mJ 	15.2mJ 
UL3 10nm	 13.9mJ	 12.0mJ	 15.2mJ

Resist B on std underlayer shows highest sensitivity and lowest LER

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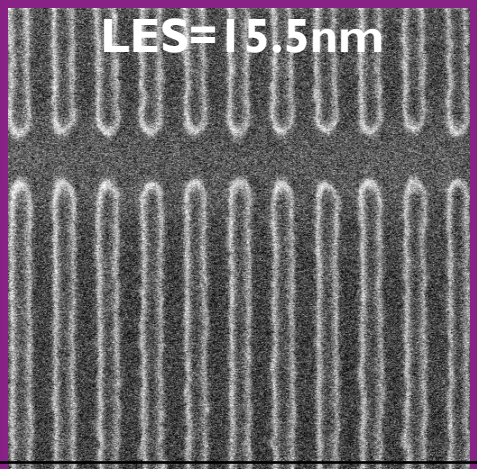
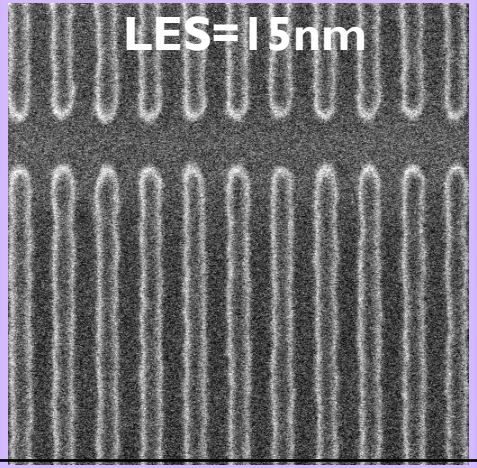
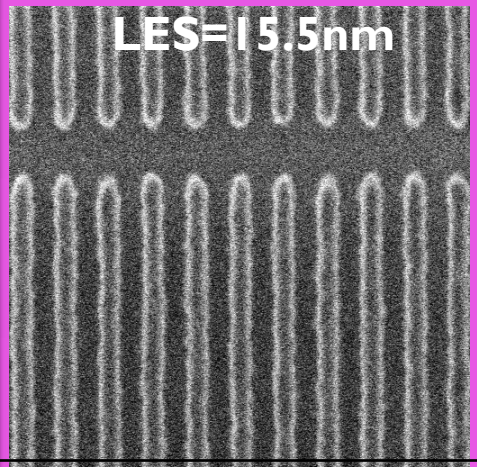
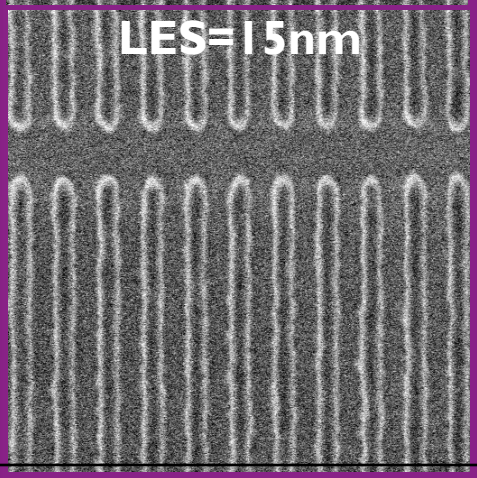
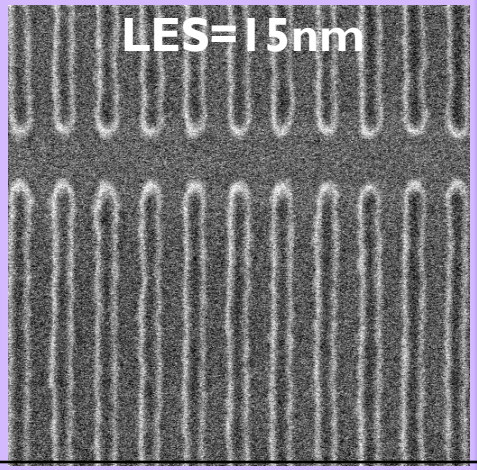
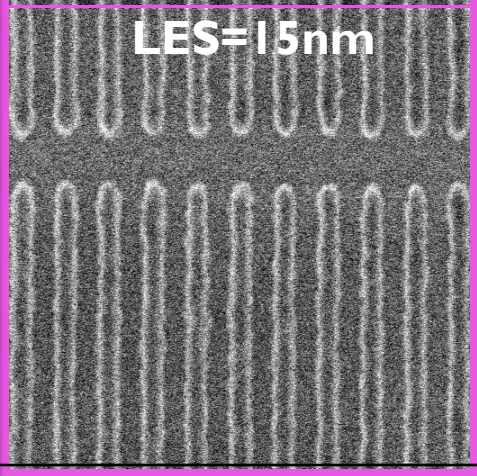
32nm LINE END SHORTENING

	RESIST A	RESIST B	RESIST C
STD UL 20nm	 LES=15.5nm	 LES=15nm	 LES=15.5nm
UL3 10nm	 LES=15nm	 LES=15nm	 LES=15nm

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32nm HP CONTACT HOLES

	RESIST A	RESIST B	RESIST C
STD UL 20nm	17.1 mJ/cm^2 LCDU=1.3nm	14.8mJ/cm^2 LCDU=1.7nm	17.6 mJ/cm^2 LCDU=1.7nm
UL3 10nm	16.3 mJ/cm^2 LCDU=1.7nm	13.8mJ/cm^2	17.6 mJ/cm^2 LCDU=1.4nm

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OUTLINE

Introduction

Lithographic screening

- Resist screening
- Underlayer screening

Benchmarking

- Lithographic performance

Process defectivity

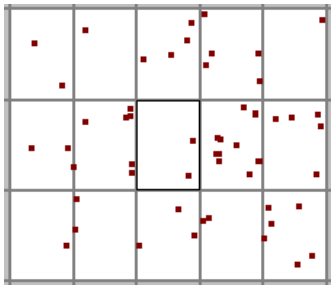
Process improvements

- TBAH
- FIRM

Resist process defectivity at 40nm hp

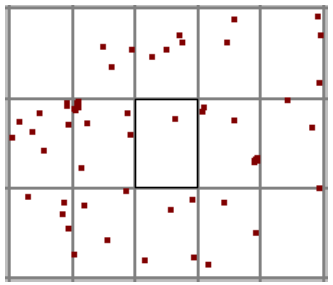
Si substrate

Resist X



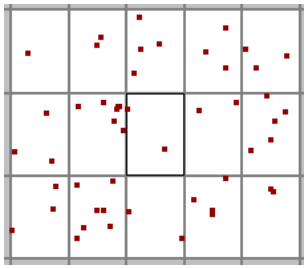
Total = 78 defects
=> Density ~
0.62 defects/cm²

Resist Y



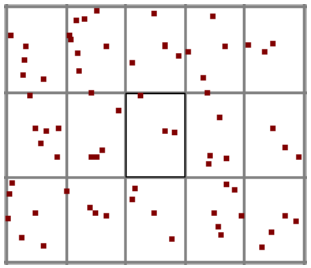
Total = 62 defects
=> Density ~
0.5 defects/cm²

Resist A



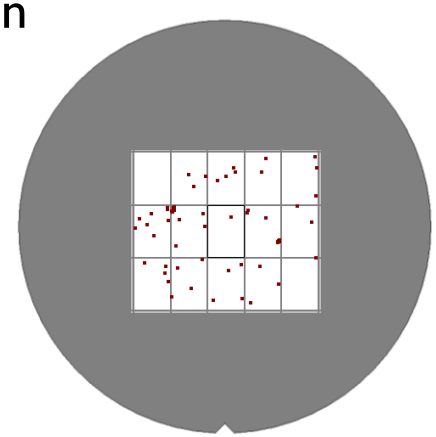
Total = 52 defects
=> Density ~
0.42 defects/cm²

Resist B



Total = 77 defects
=> Density ~
0.62 defects/cm²

Process defectivity for resist on silicon



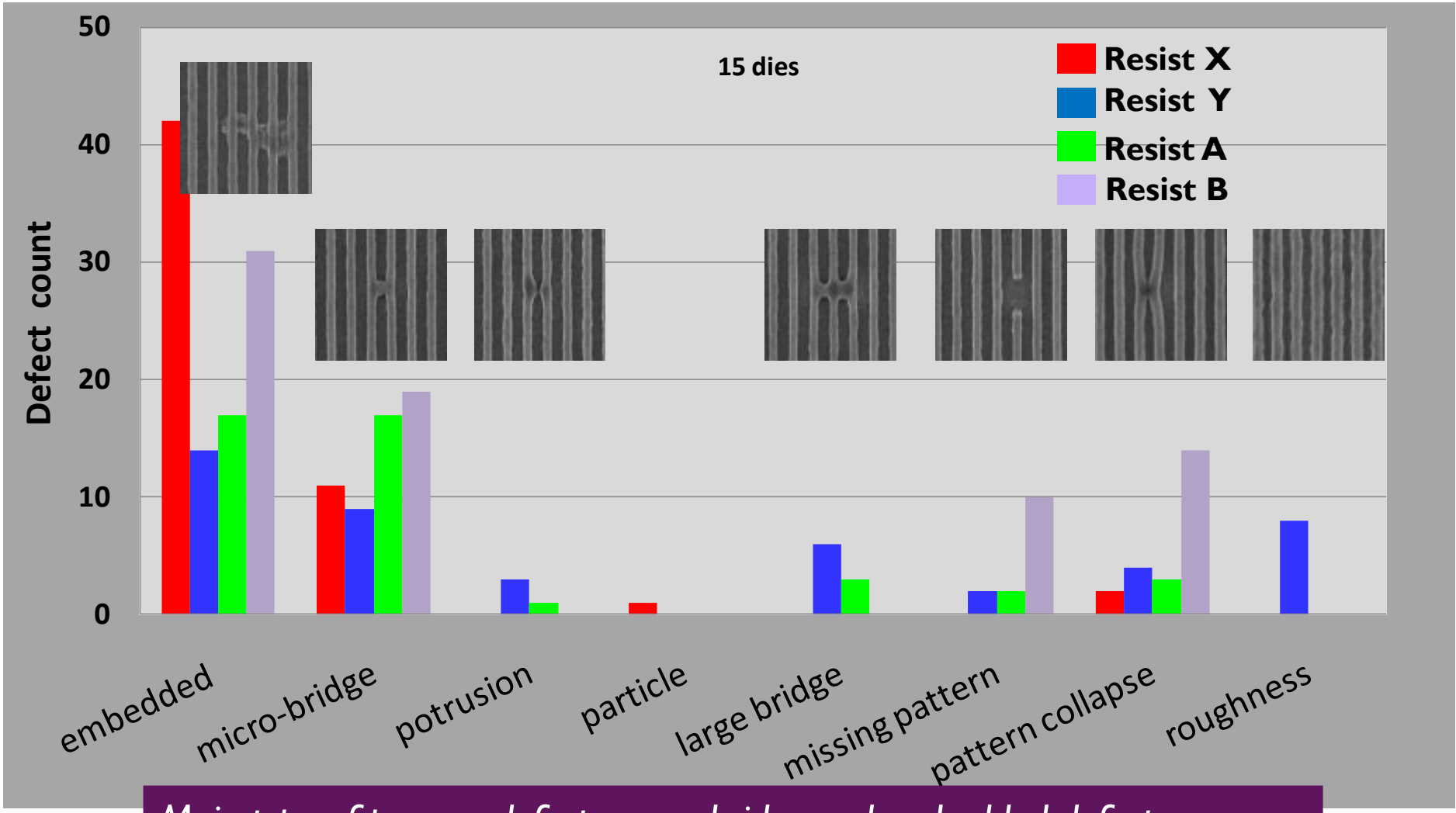
- Resist thickness 60-65nm on silicon
- Reticle : DEFECT40FF : 40nm LS
- 15 Fields, 26x33mm² field size
- Defect measurement KLA 2800
- Defect review/classification
  G3- SEMVision

Comparable defectivity levels for the EUV resist ,average defect density < 0.6 defects/cm²

Poster RI-P09, Dieter Van den Heuvel

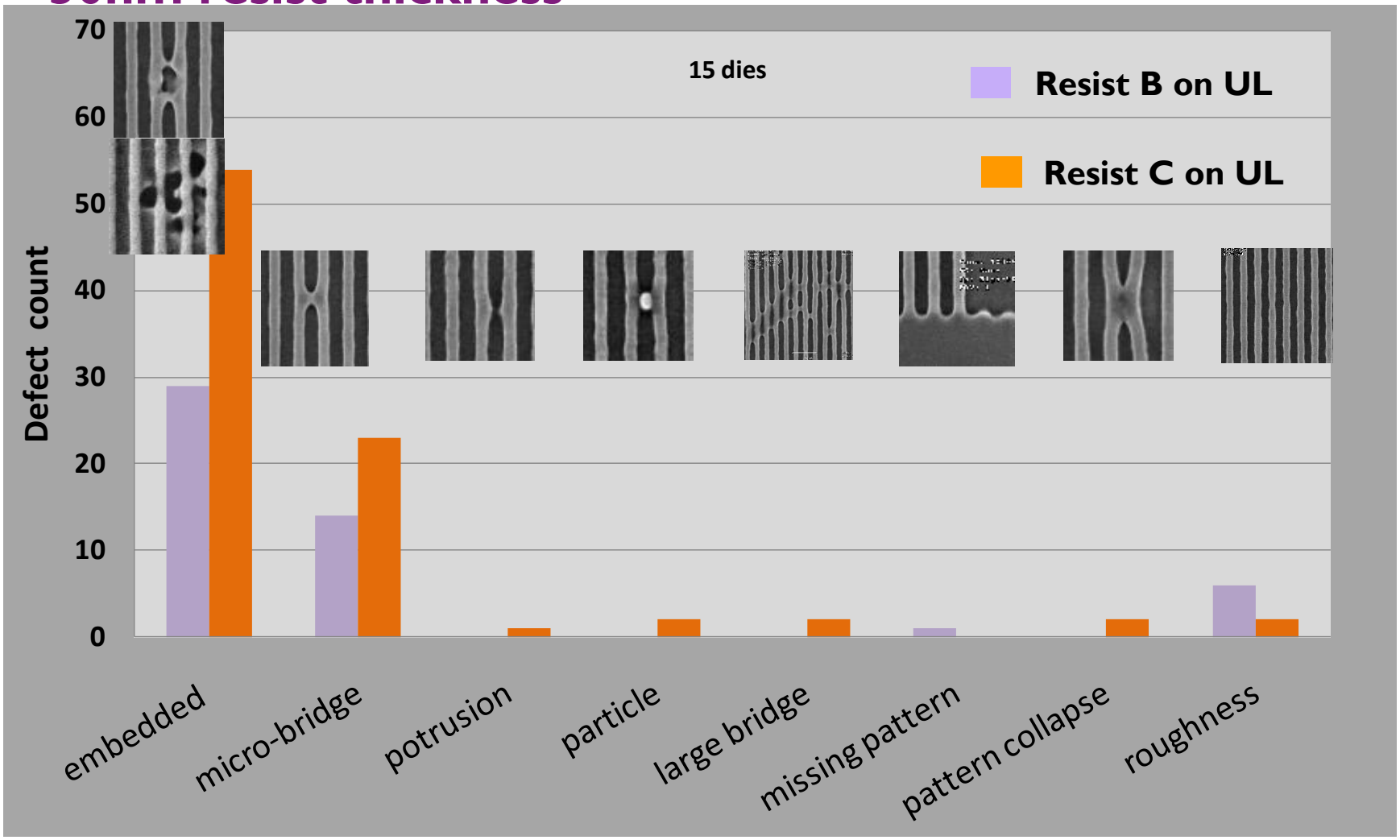
Process defectivity classification (40nm HP)

60nm-65nm thick resist on Si substrate



Main type of process defects are µ-bridge and embedded defects
No EUV resist specific defects

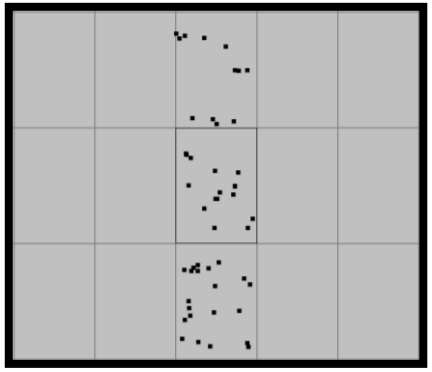
Process defectivity resist on underlayer (40nm HP) 50nm resist thickness



Main type of process defects are µ-bridge and embedded defects in resist or in underlayer. Total defect densities ~ 0.4-0.69 defects/cm²

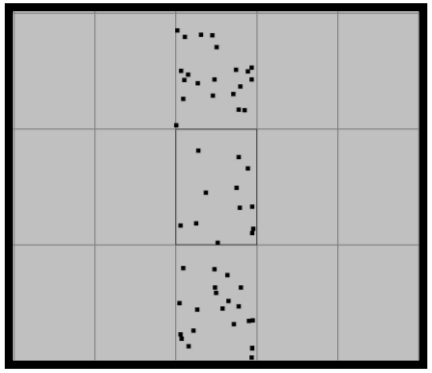
Resist process defectivity at 32nm HP on 20nm std underlayer

Resist Y



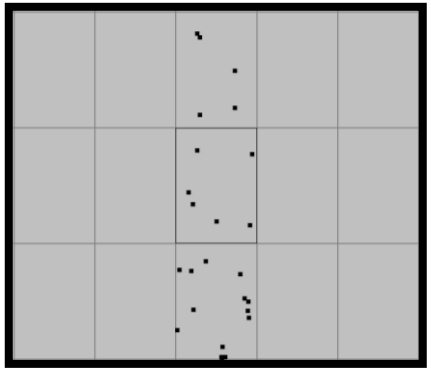
Total = 51 defects => Density ~ 2.1 defects/cm^2

Resist A

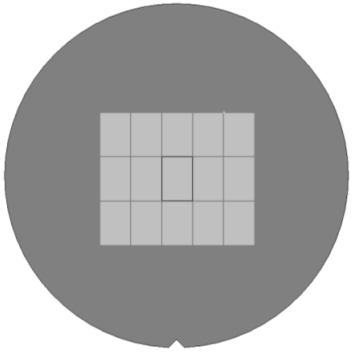


Total = 56 defects => Density ~ 2.3 defects/cm^2

Resist B



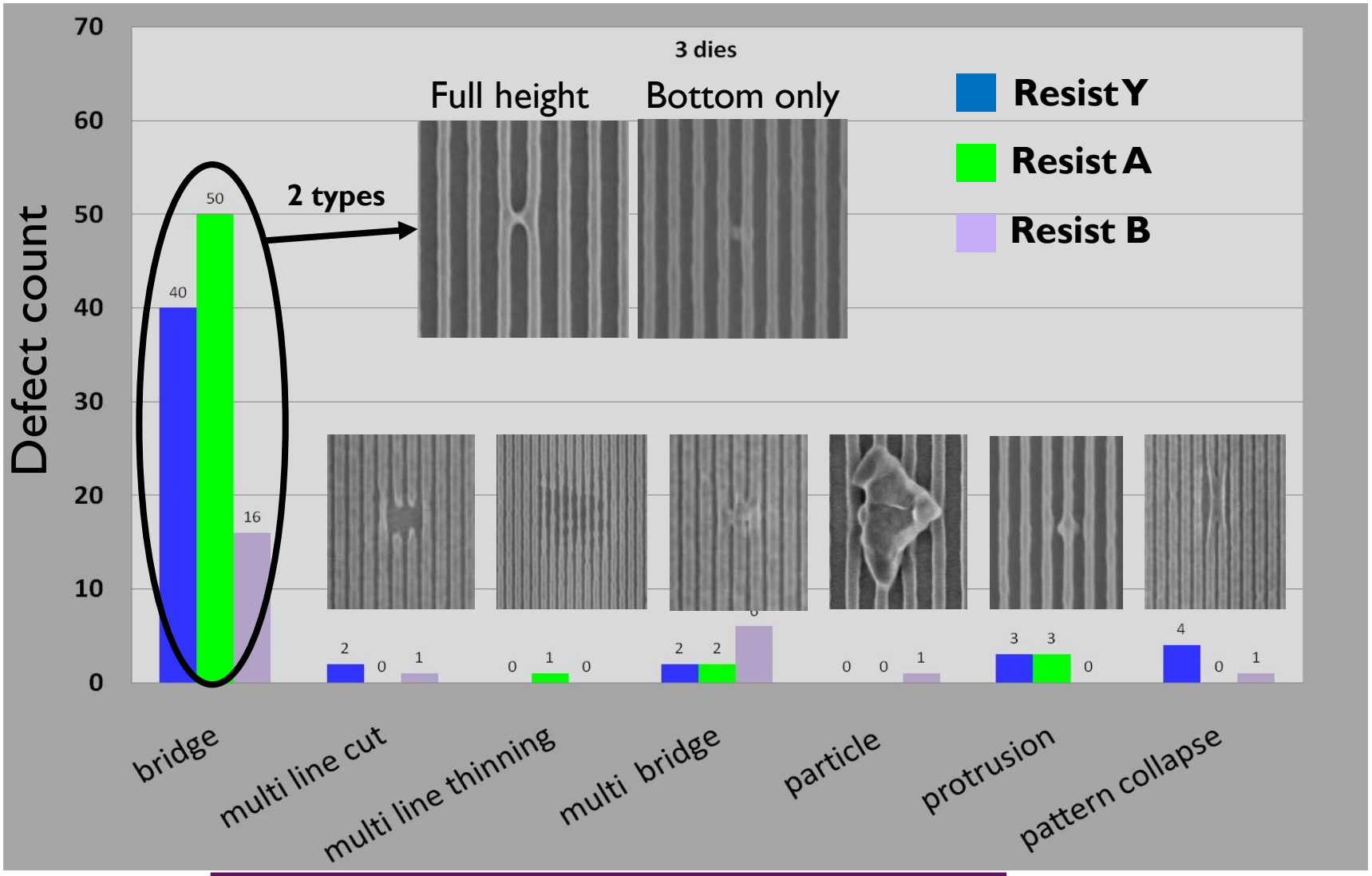
Total = 25 defects => Density ~ 1.0 defects/cm^2



- Reticle : DEFECT32FF
- 15 Fields exposed, 26x33mm^2 field size
  3 fields measured
- Applied UVision 4 Inspection
- Applied SEMVision G4 Defect Analysis

*Process defect levels **at 32nm HP** are in the order of 1 to 2 defects/cm^2*

DEFECT CLASSIFICATION 32NM HP



Main type of process defects are bridge defects

OUTLINE

Introduction

Lithographic screening

- Resist screening
- Underlayer screening

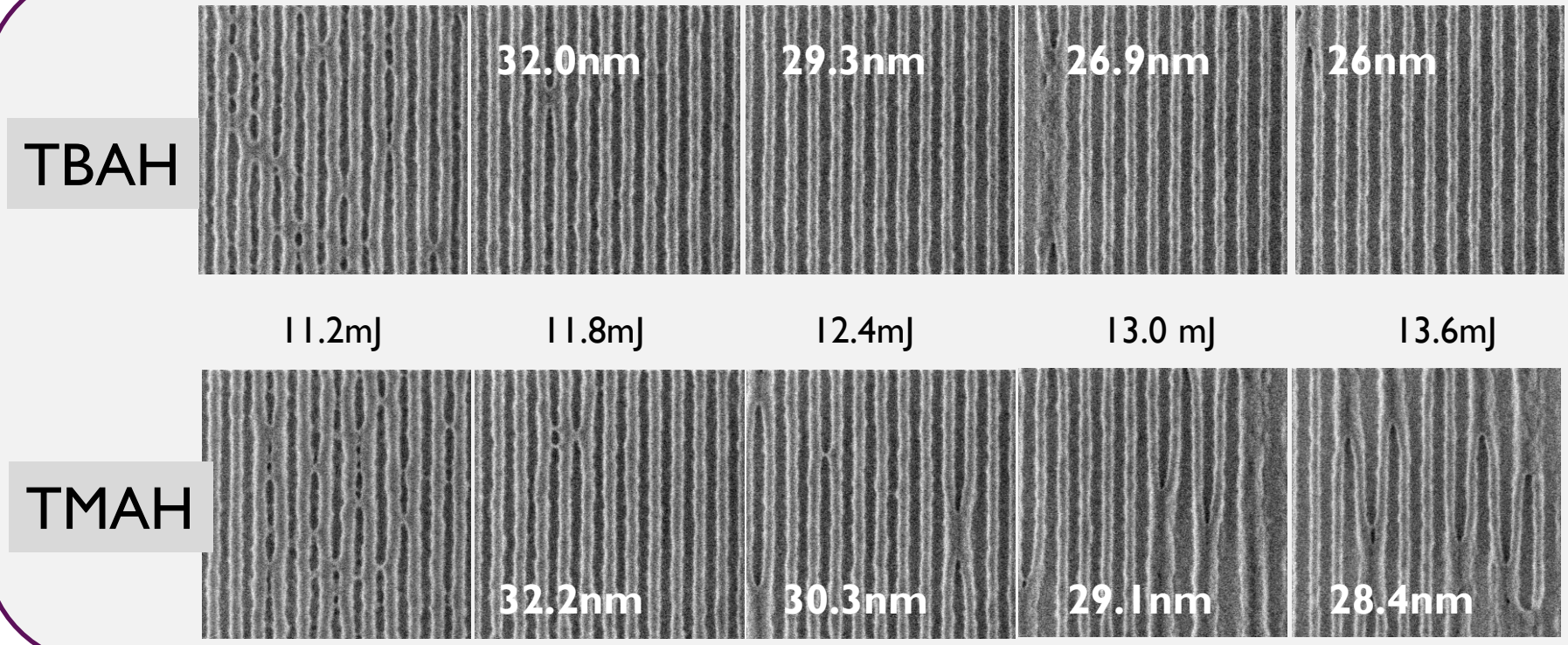
Benchmarking

- Lithographic performance
- Process defectivity

Process improvements

- TBAH
- FIRM

APPLICATION OF TBAH DEVELOP
28nm LS, resist B, 60nm FT

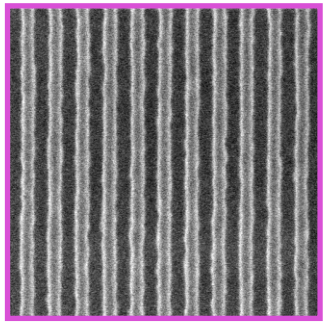


TBAH developer improves the pattern collapse margin for Resist B
TBAH resulted in 6% photospeed improvement (Based on 30nm L/S)

Poster RE-P05, Roel Gronheid

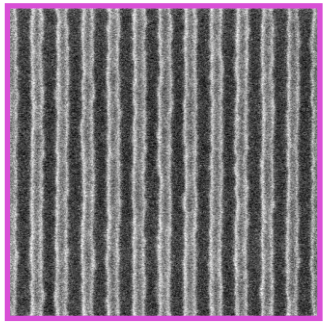
APPLICATION OF TBAH DEVELOPMENT
Resolution of resist B on UL, 60nm FT

TBAH



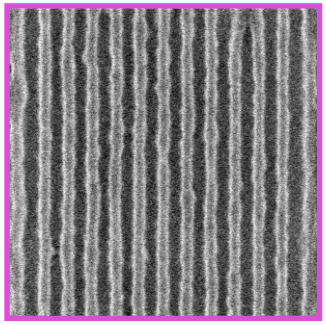
CD=30.1nm
Dose 11.8mJ

30nm



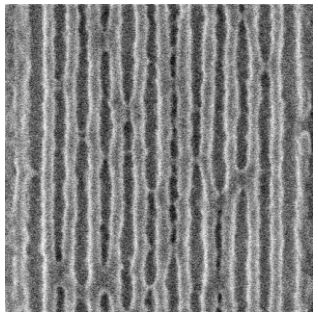
CD=26.9nm
Dose 13mJ

28nm



CD=26.3nm
Dose 14.2 mJ

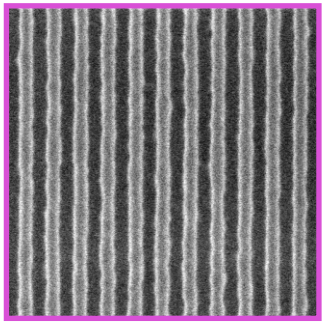
26nm

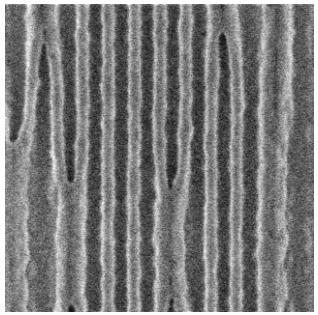


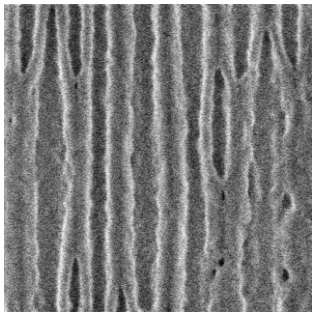
CD=25.5nm
Dose 14.2 mJ

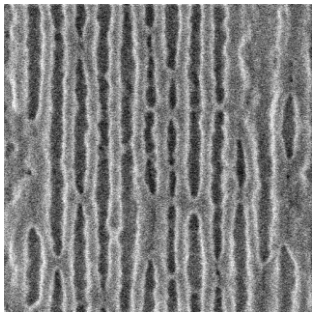
25nm

TMAH









Clear improvement in resolution with TBAH by reduction in pattern collapse

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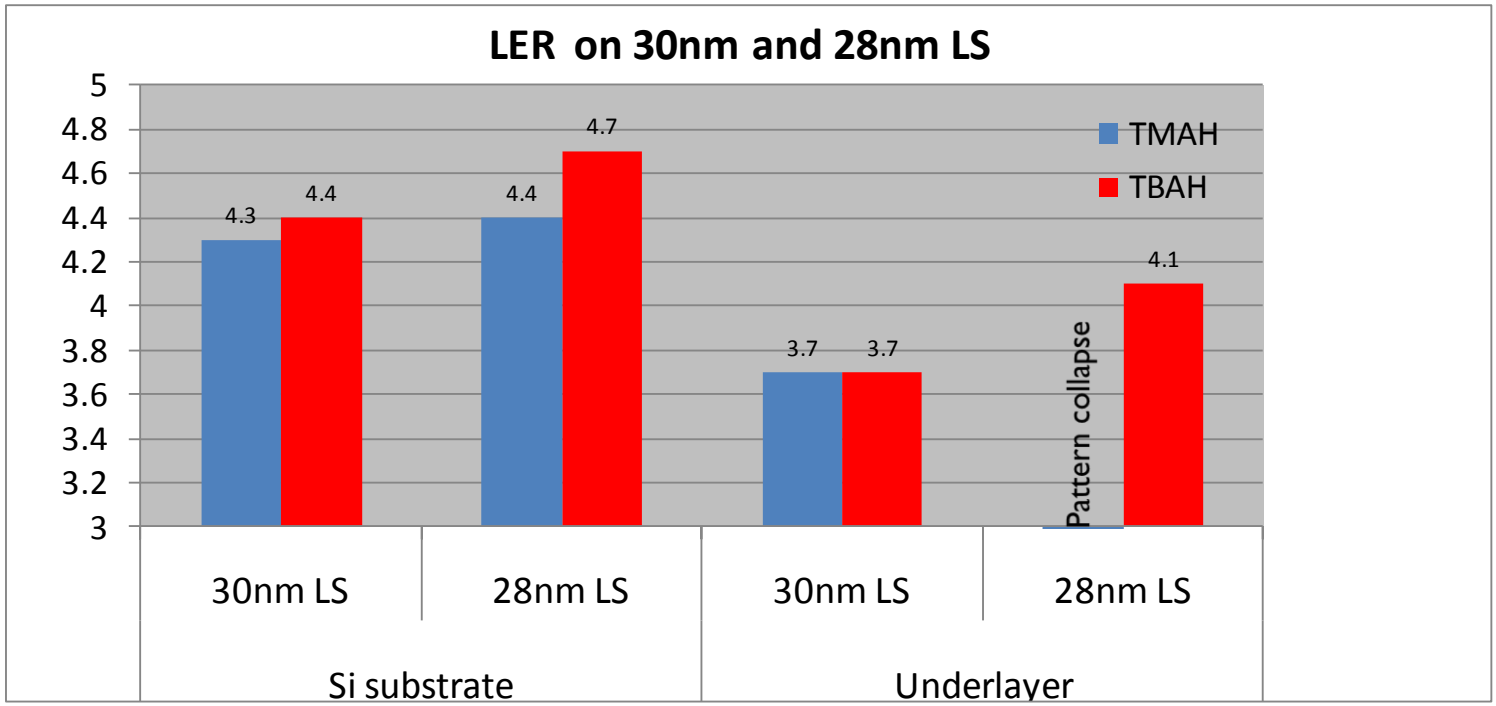
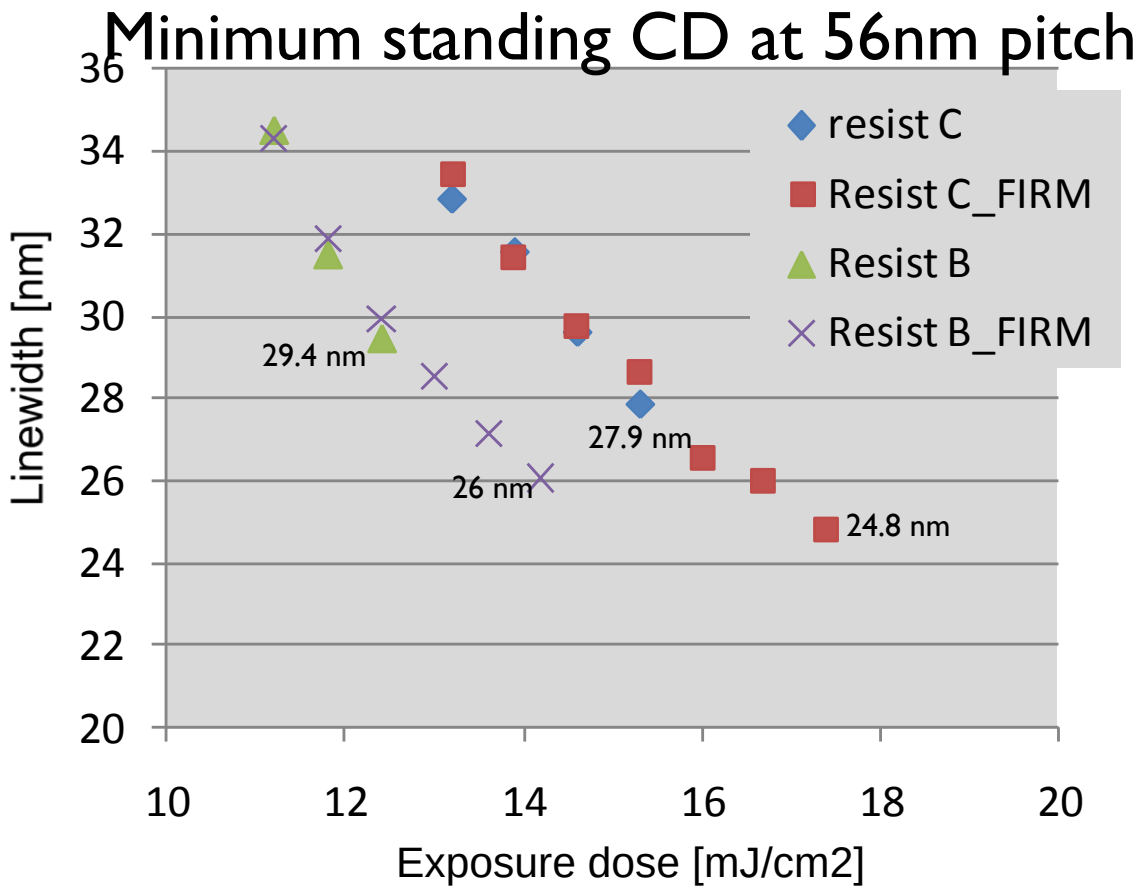
TMAH VS. TBAH DEVELOP LER COMPARISON



The use of TBAH developer has no positive effect on LER
Up to 15 % improvement in LER by the application of an underlayer

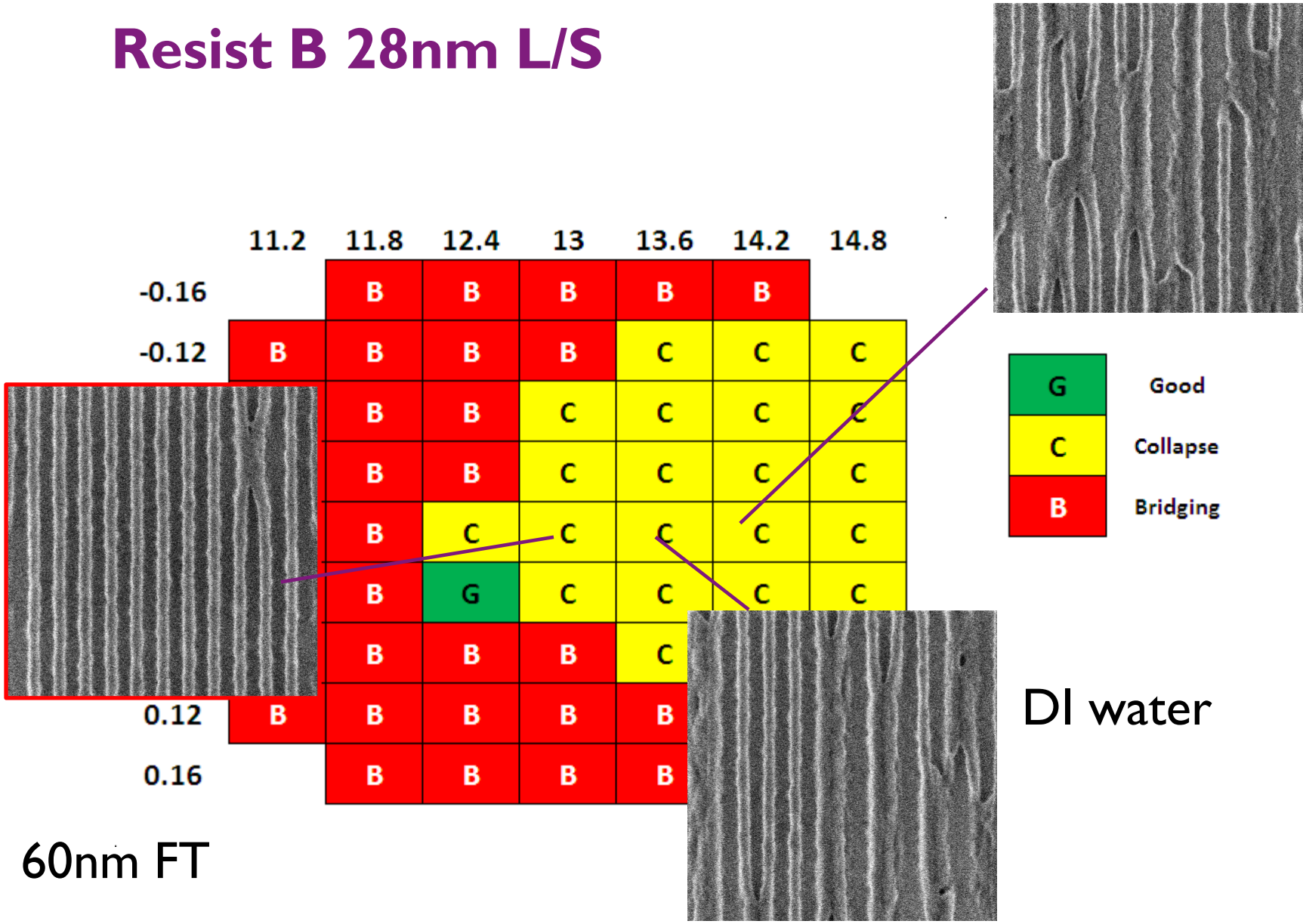
APPLICATION OF FIRM™EXTREME
Pattern collapse margin for 28nm hp, 60nm FT



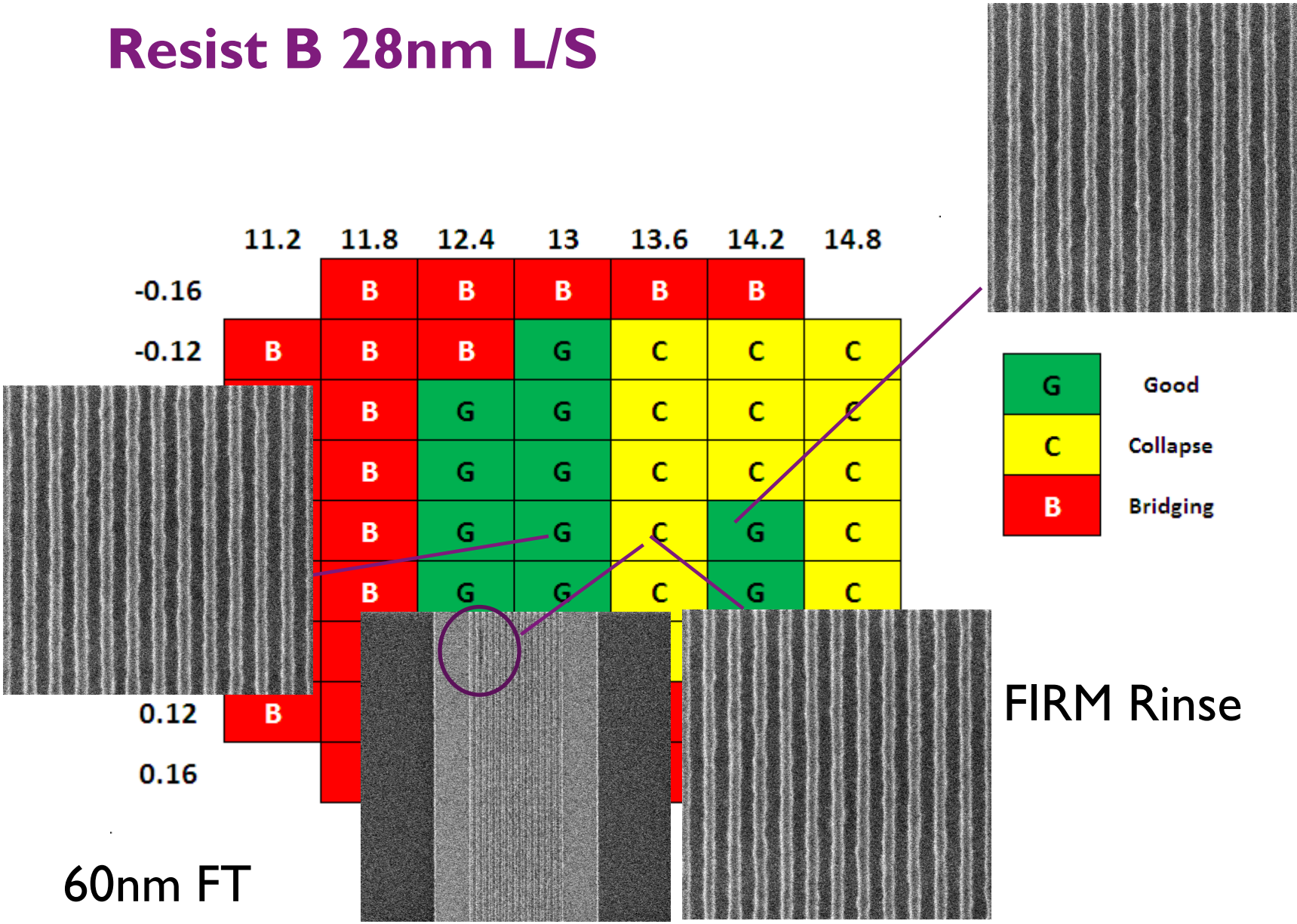
No impact on resist sensitivity
Clear improvement in pattern collapse margin with FIRM for both resists

See also ***Poster*** *RE-P03*

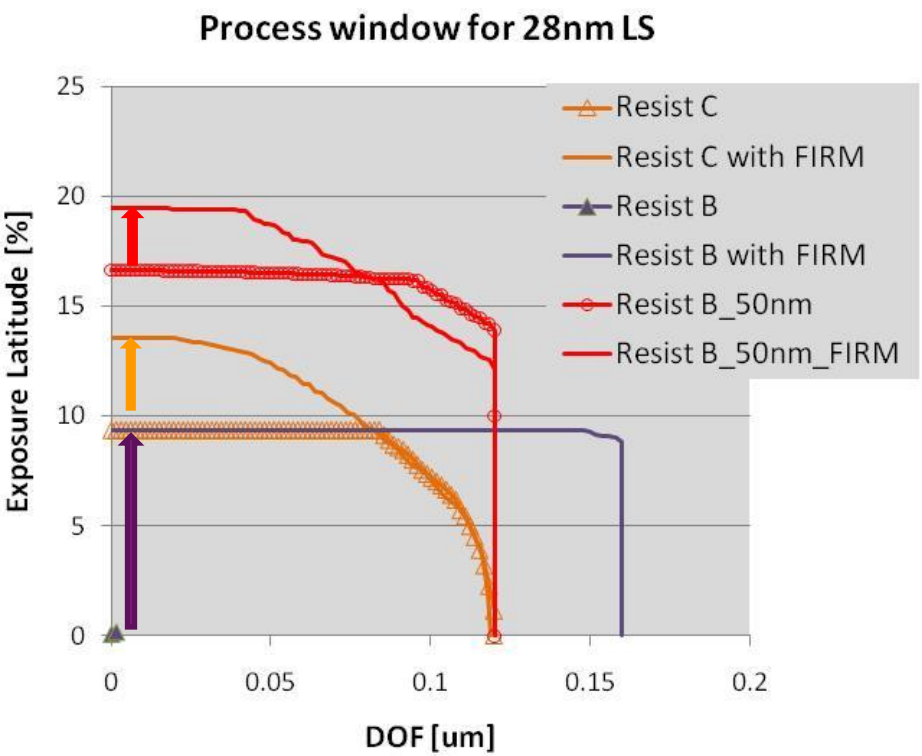
Effect of FIRM Rinse on Process Window Resist B 28nm L/S

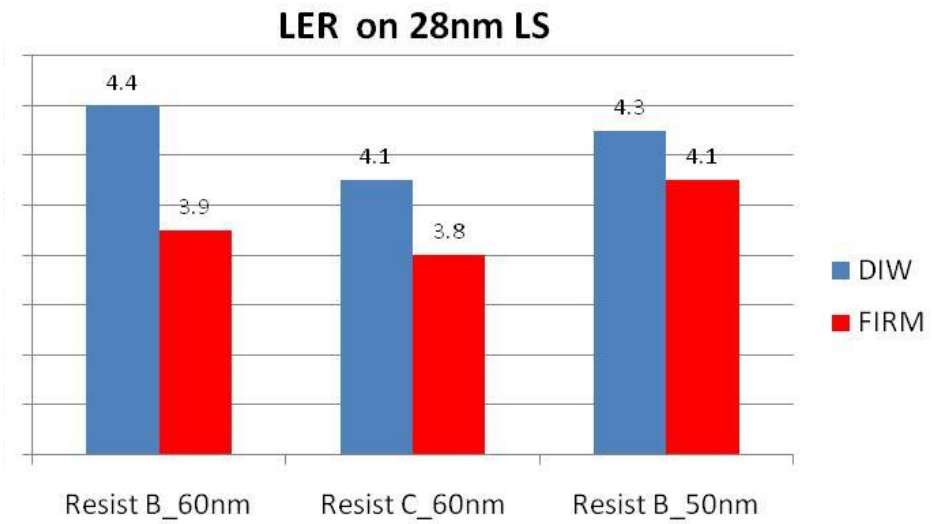


Effect of FIRM Rinse on Process Window Resist B 28nm L/S



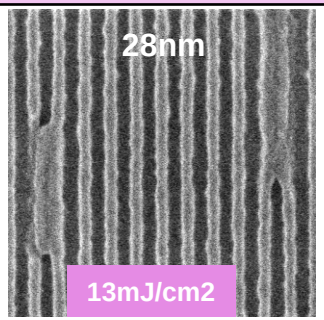
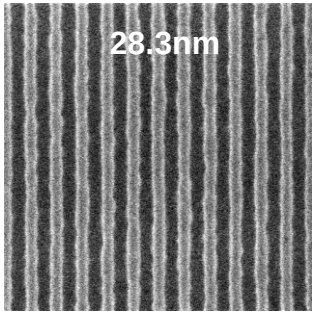
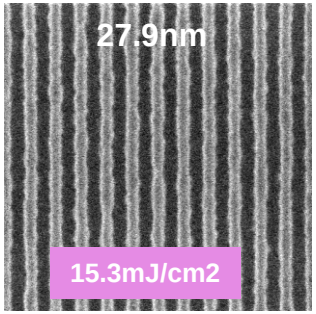
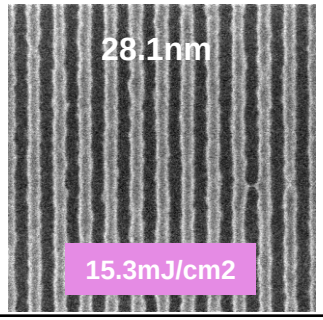
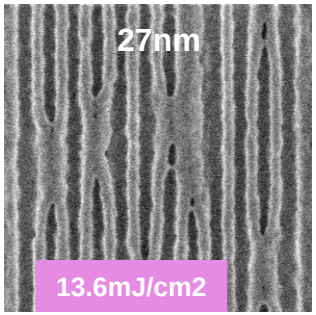
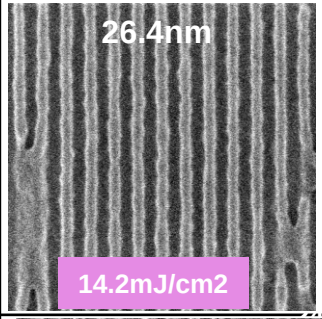
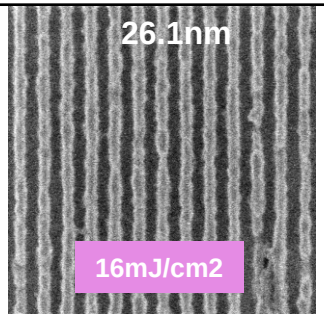
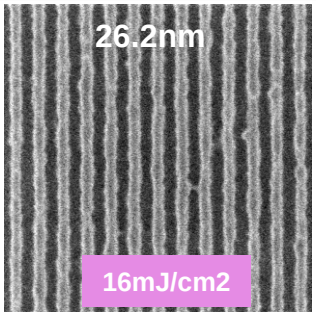
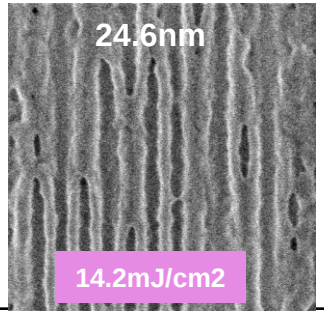
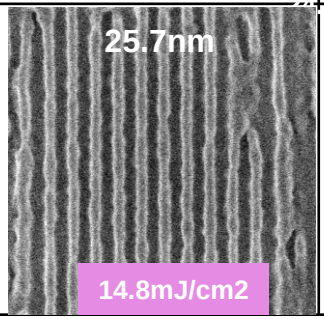
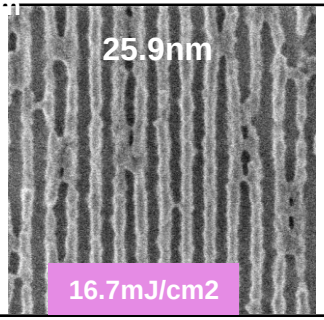
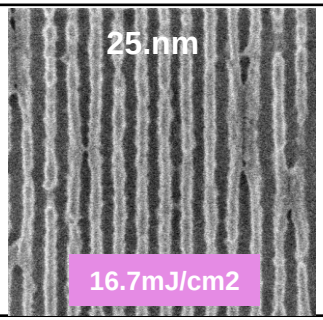
Effect of FIRM on process windows and LER Resist B and C, 28nm HP





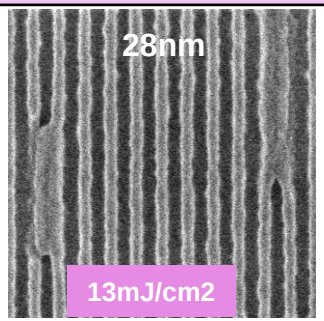
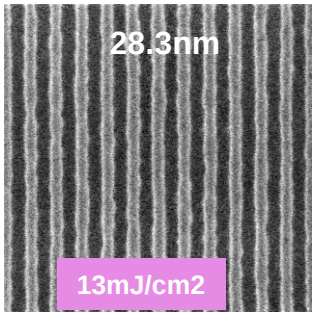
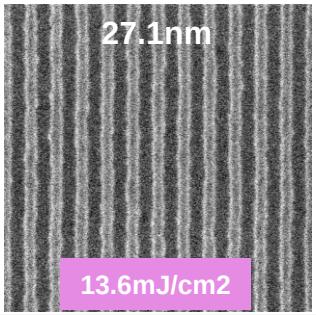
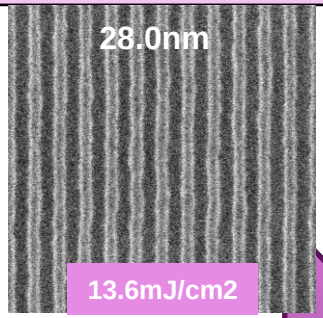
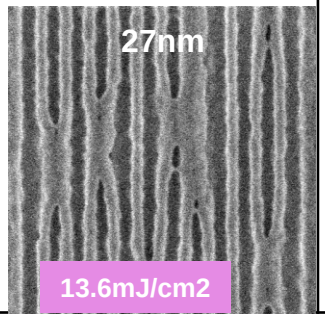
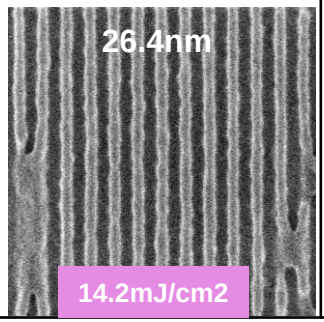
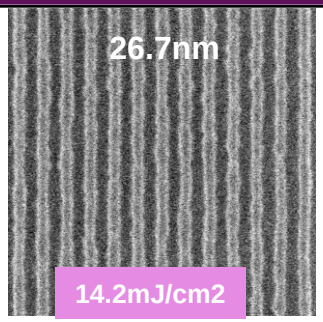
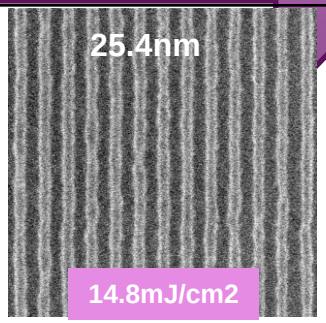
Clear process window and LER improvement with FIRM Rinse for 28nm L/S for both resists

FIRM rinse on ultimate resolution in 60nm resist thickness for resist B and C

Resolution	Resist B DI-water	Resist B FIRM	Resist C Di-water	Resist C FIRM
28nm HP				
26nm HP				
25nm HP				

Clear improvement in resolution from >28nm to sub-28nm for resist B

Resist B : Ultimate performance
Reduction in resist thickness combined with FIRM

Resolution	Resist B DI-water 60nm thickness	Resist B FIRM 60nm thickness	Resist B Di-water 50nm thickness	Resist B FIRM 50nm thickness
28nm HP				
	LER= EL=0% UR=29	LER=3.9 EL=9% UR=28 NanoZ=1.3	LER=4.3 EL=17% UR=26.5 NanoZ=1.38	LER=4.1 EL=19% UR=26 NanoZ=1.2
26nm HP				

Improved process window and LER on 28nm LS and resolution down to 26nm hp lines in 50nm thickness combined with FIRM

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SUMMARY AND CONCLUSION

- Steady progress in resist performance :
  - Sub-28nm feature resolution demonstrated on ADT with PW
  - Acceptable process defectivity levels for EUV resists
- Main challenges remain LER and pattern collapse
  - Application of an appropriate underlayer improved the LER
  - Resist thickness reduction improves the pattern collapse and resolution but at the expense of higher LER.
- Process improvements have been investigated :
  - TBAH development
    - Improves pattern collapse and resolution
    - No improvement in LER
  - FIRM rinse
    - Improves the pattern collapse margin and LER for two different resists (chemistries)

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