Printability and Inspectability of Programmed and Real Defects on the Reticle in EUV Lithography

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Outline

- Objective of the presentation
- Experimental procedure
- Defect printability using programmed pit defect
  - Reticle fabrication method
  - Minimum defect printability as location, size, and height
- Defect printability using real defect
  - Defect verification method without EUV AIMS
  - Printability based on wafer inspection & review using defect map
- Summary of presentation

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Objective of the Presentation

- Preparation of defect-free reticle is the top critical issue to launch EUVL into HVM.
- How can we accomplish it?
  - Blank inspection tool and defect review tool should be ready on time.
    However, introduction of reticle inspection & defect review tools is a big concern.
  - Practical printability and specification of defects should be primarily studied & defined.
- In this presentation, we will mainly discuss…
  - Printability study of blank defects
  - Their printability and inspectability in EUV and DUV wavelength
  - Defect verification method using current not enough infra-structure
- Two EUV reticles, with programmed pit defect and native defects, are used to evaluate the defect printability.

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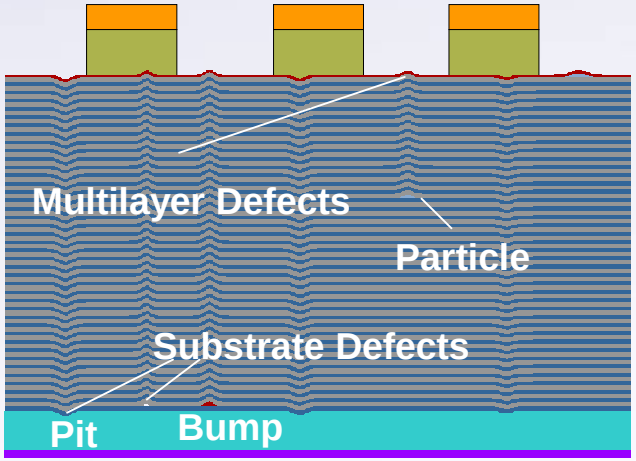
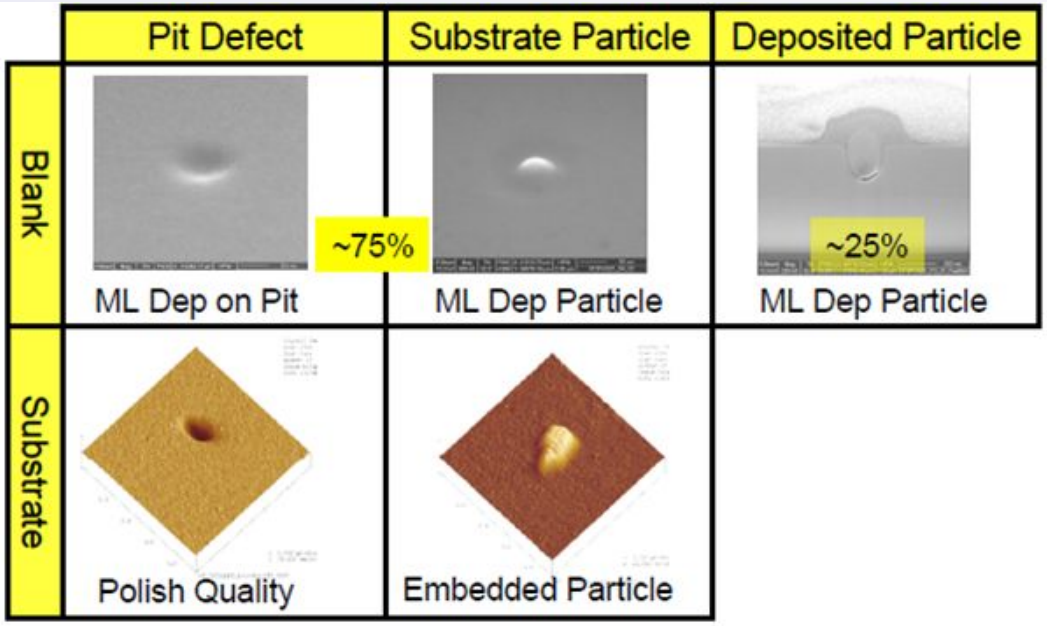
Defect Sources on the Blank

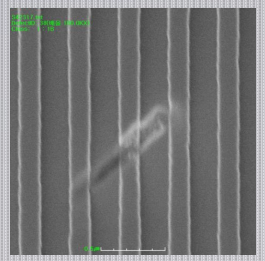
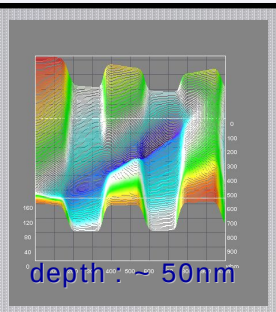
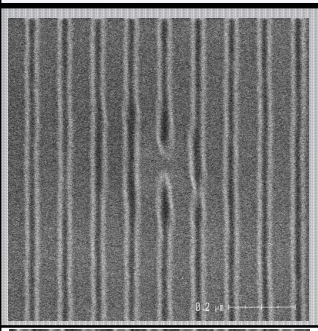
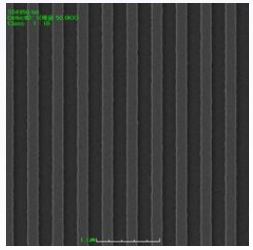
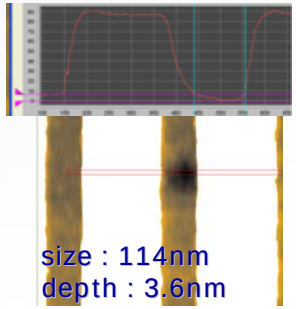
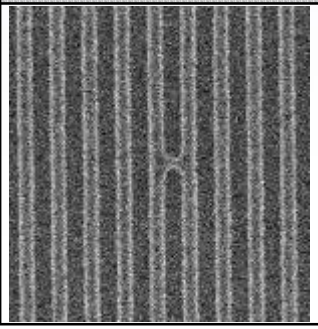




Yun, H, et al., Proc. of SPIE Vol. 7379, 73790G (2009).

- Blank defect reduction and its inspection tool are challenge for successful EUV lithography development.
- 75% of blank defects are originated from the substrate.
  - Substrate defects including pits & bumps (particle) are the most dominant defect types in EUV blanks.
  - Polishing & cleaning steps of LTEM substrate is the key process to reduce blank defects.

Detectability and Printability of Blank Defect

	Blank inspection	Reticle inspection	Mask SEM	AFM on reticle	Wafer SEM	Wafer inspection
Deep blank defect	Detected	Detected				Detected
Shallow blank defect	Not detected	Not detected				Detected

- Large phase defects can be easily detected by both reticle & wafer inspections.
- However, in the case of small phase defects (pits & bumps), It is hard to be detected by current blank and reticle inspection tools.
- This paper will present the requirement of the defect specification and defect review tool to qualify an EUV mask.

Experimental Procedure

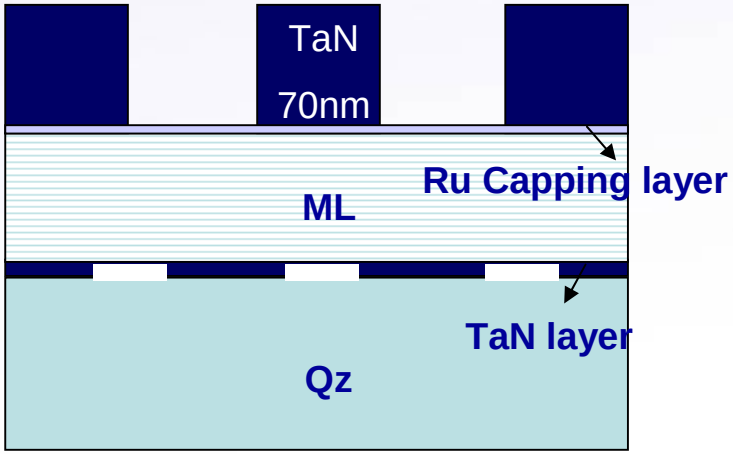
1. Reticle with programmed pit defect
   - Defect printability as minimum size, depth, location of programmed pit defect
   - Blank inspection, EUV ADT, SEMATECH Berkley AIT

2. Full field EUV reticle of contact array pattern with natural blank defect
   - Evaluate if wafer inspection tool can be used instead of EUV AIMS™.
   - Blank inspection, EUV ADT exposure, pattern inspection tool, wafer inspection tool

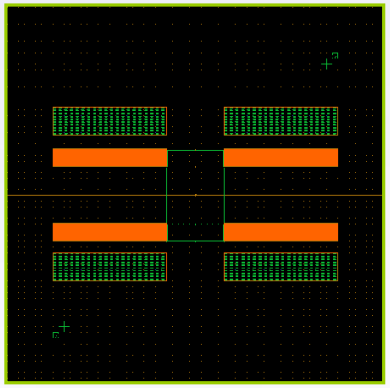
1) Programmed Pit Defect

1) Thin TaN layer to make pit

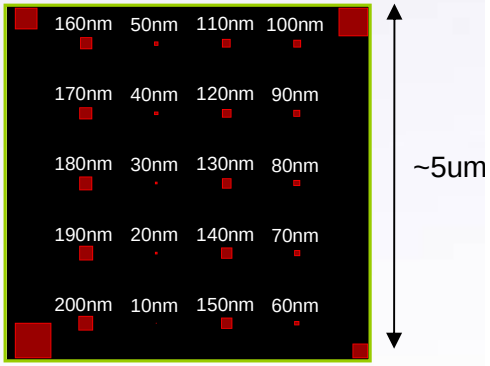
2) ML deposition & absorber patterning



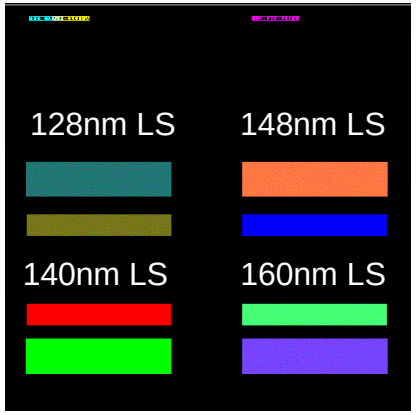
Layout1 : Pit array pattern



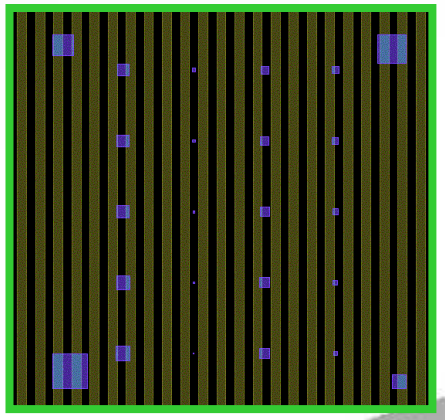
Pit array unit
(Designed size)



Layout2 : L/S pattern



Pit array unit under
absorber pattern



- We used smoothing ML deposition to make shallow defect.
- After finishing all process, various size pit defects are located under absorber pattern.

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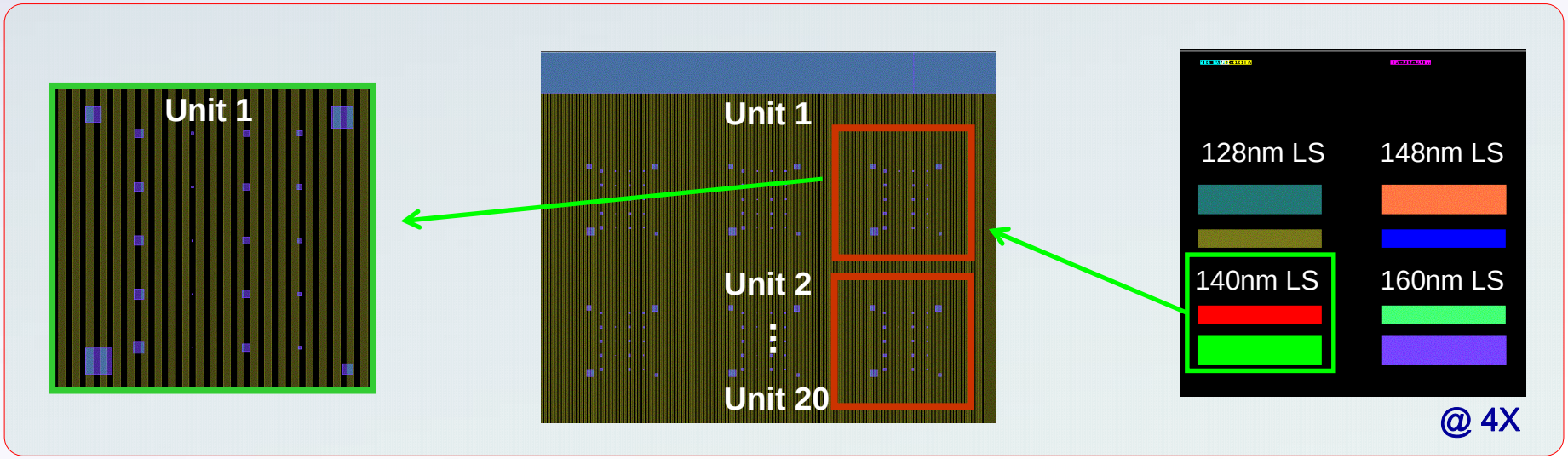
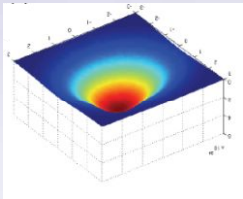
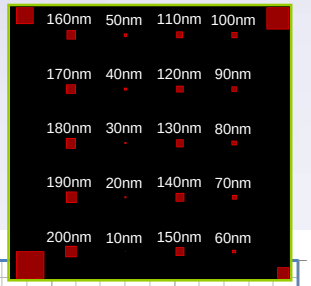
Pit Defect Position After Absorber Patterning



- As no alignment option was used during e-beam writing, pit array position slightly moves along the y-axis. Degree of shift of defects in each unit is ~16nm. So, we can see the defect printability as its position.
- In order to verify pit defect printability on the various defects' position, ~20 points were reviewed during defect review on the region of 140nm HP L/S (35nm in wafer scale)

Characterization of Programmed Pit Defect

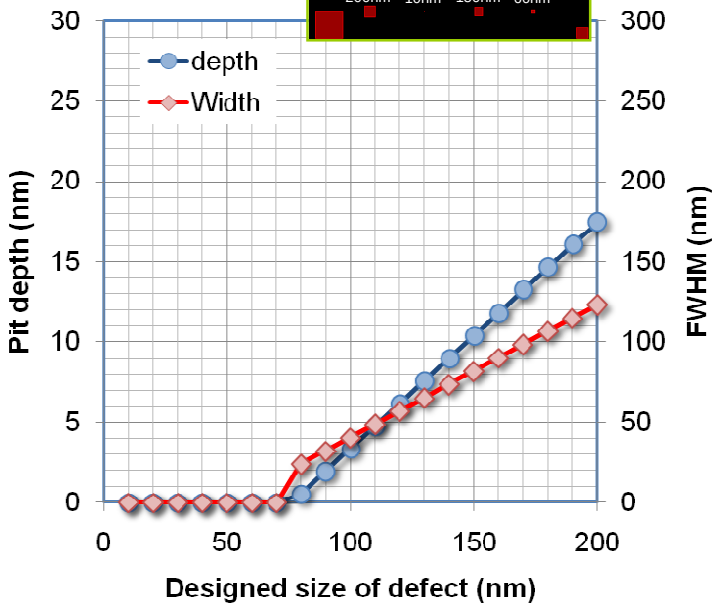


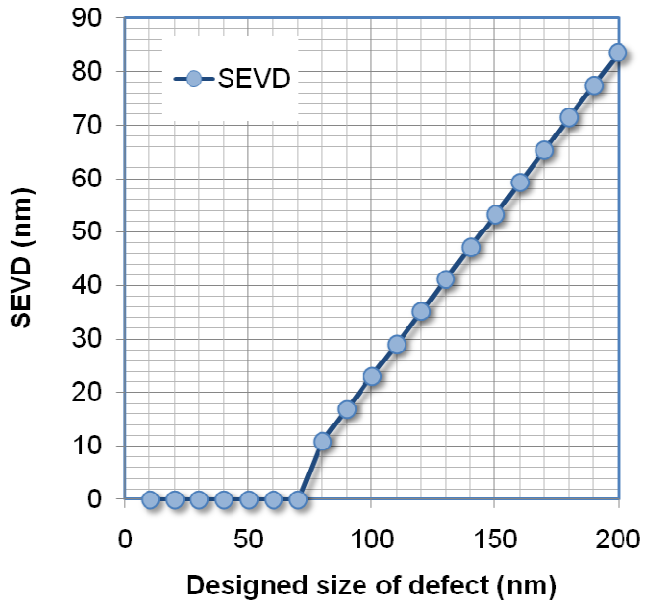


$$(SEVD)_{Gaussian} = 2\left(\frac{3h_0(FWHM)^2}{16\ln(2)}\right)^{\frac{1}{3}}$$

$$\text{pit depth} = h_0$$

$$\text{pit width} = FWHM$$

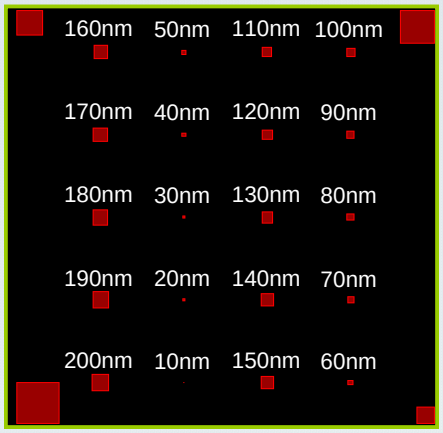




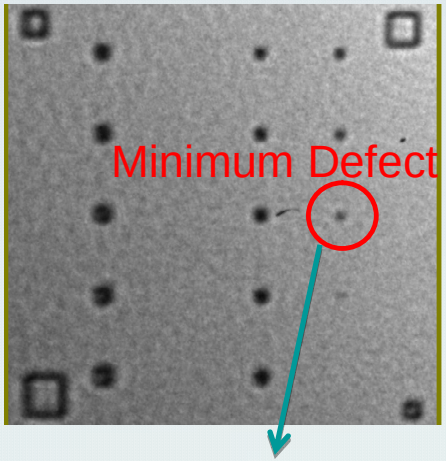
- ML smoothing deposition method is used to make shallow defect.
- Measured width and depth can be converted to SEVD (spherical equivalent volume diameter) using gaussian defect scheme.
  - Minimum defect size : 0.55nm depth, 23.9nm FWHM, 11nm SEVD

Pit defect visibility on Blank Inspection Tool

Design of Programmed defect

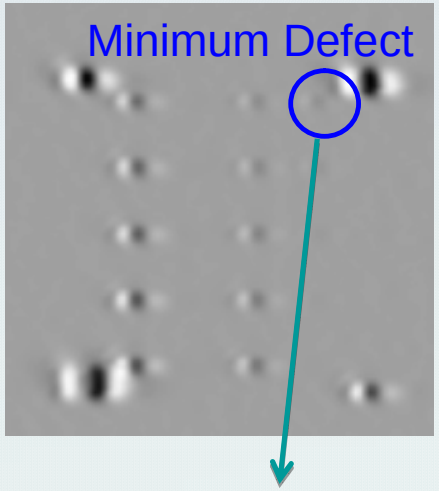


SEMATECH-LBNL AIT



FWHM : 23.9nm, depth : 0.56nm
SEVD : 11nm

M7360

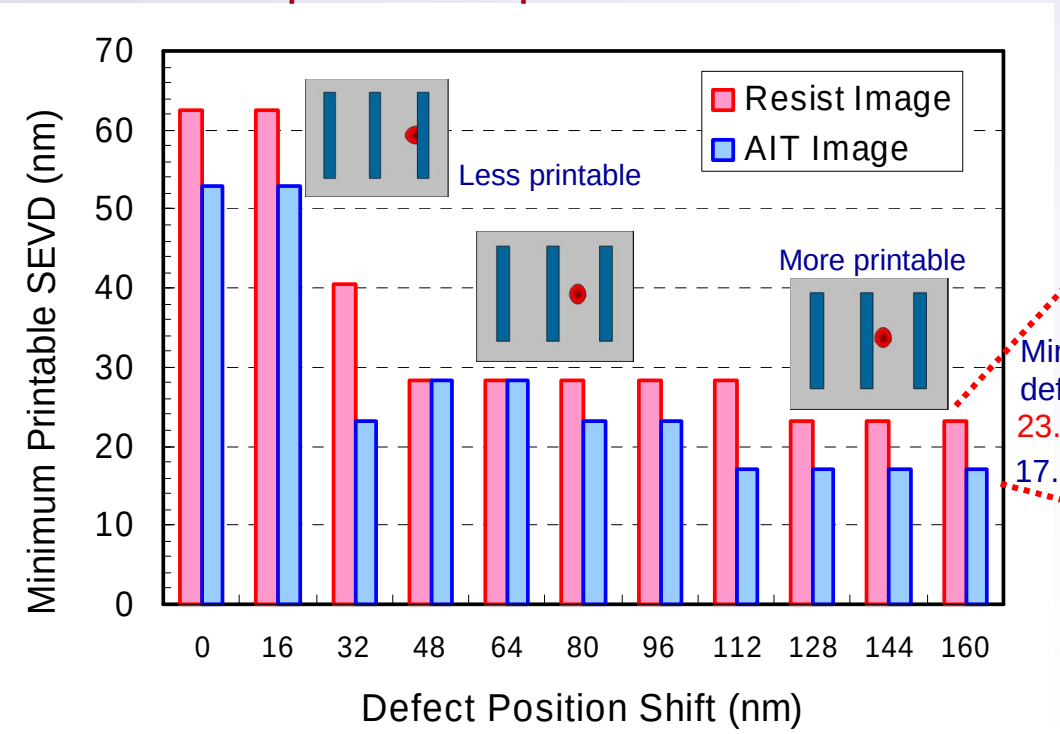


FWHM : 40.5nm, depth : 3.4nm
SEVD : 23.1nm

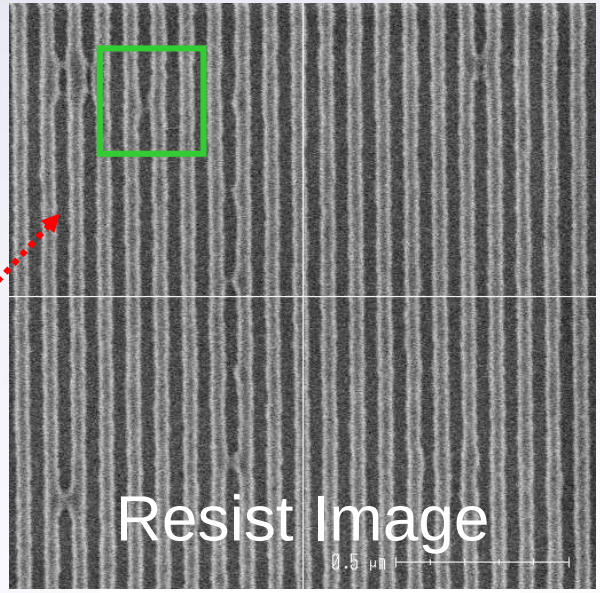
- Visibilities of pit defects on review images before absorber deposition (not inspection mode) are compared.
- Defect visibility on AIT is more sensitive than DUV blank inspection.
- We will see the minimum printable defects after absorber patterning using AIT and EUV ADT.

Minimum Defect Printability

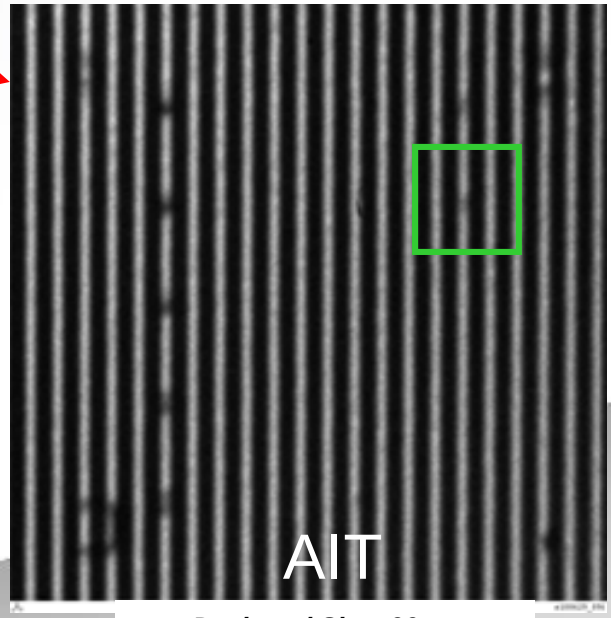
Minimum printable pit defect on 35nm HP



Min. printable defect in SEVD
23.1nm : Resist
17.1nm : AIT



Designed Size: 100nm
SEVD : 23.1nm
Width : 40.5nm, depth : 3.4nm

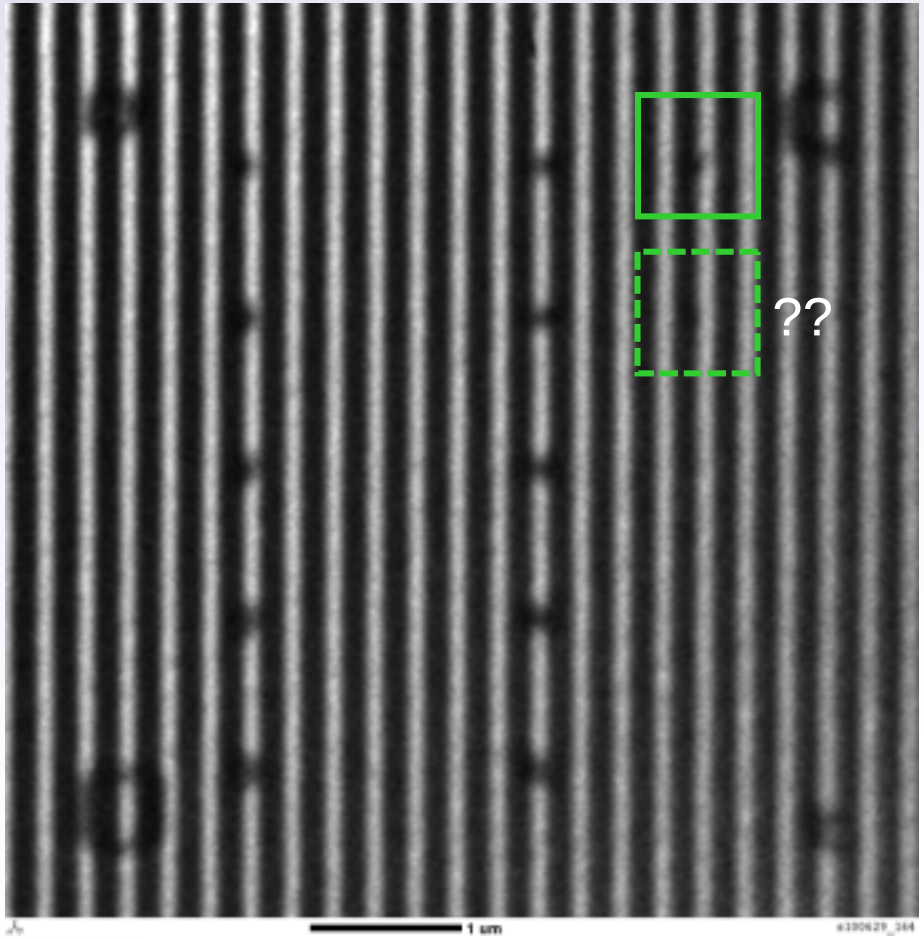


Designed Size: 90nm
SEVD : 17.1nm
Width : 32.3nm, depth : 2.0nm

- When defects are located in the middle of ML area. AIT can see minimum printable defect of 23.1nm in SEVD, but ADT can see 28.3nm in SEVD.
- When defects are located near absorber sidewall, it will be more printable. AIT can see minimum printable defect of 17nm in SEVD, but ADT can see 23.1nm in SEVD.
- Defect printability is very sensitive to the defect position. Blank inspection tool's specification should be based on the critical case.

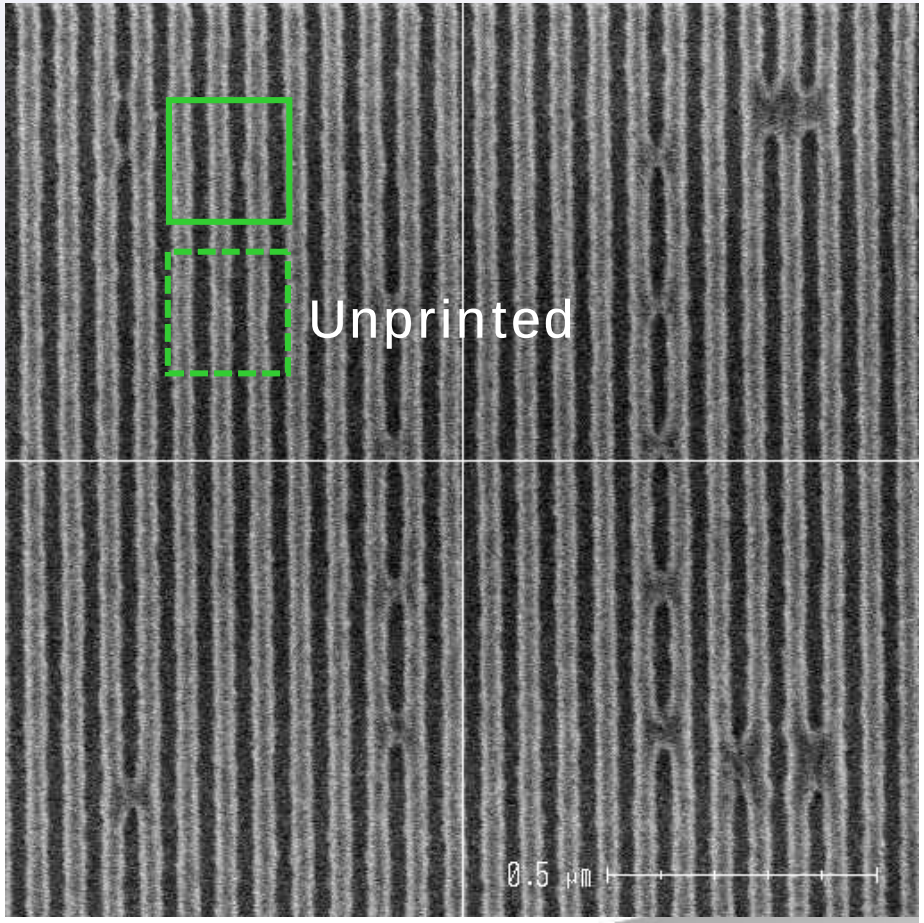
Defect Printability Through Focus

Best focus



AIT

Designed Size: 100nm
SEVD : 23.1nm
Width : 40.5nm, depth : 3.4nm



Designed Size: 100nm
SEVD : 23.1nm
Width : 40.5nm, depth : 3.4nm

Wafer SEM

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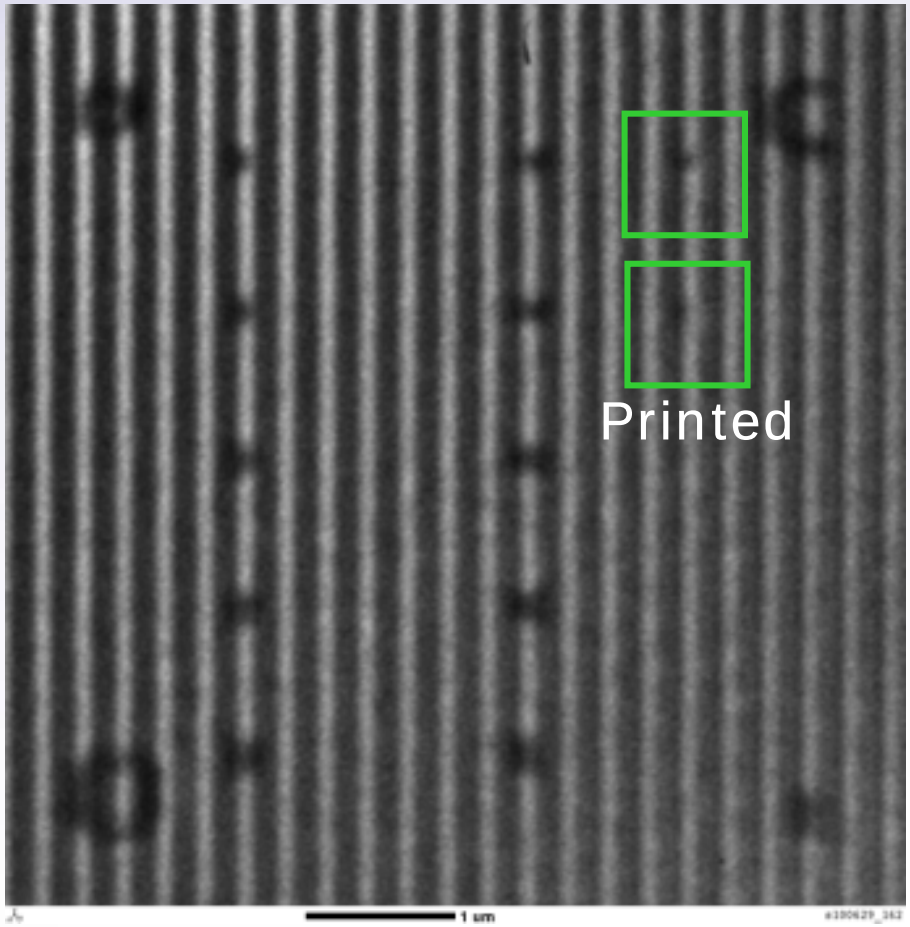
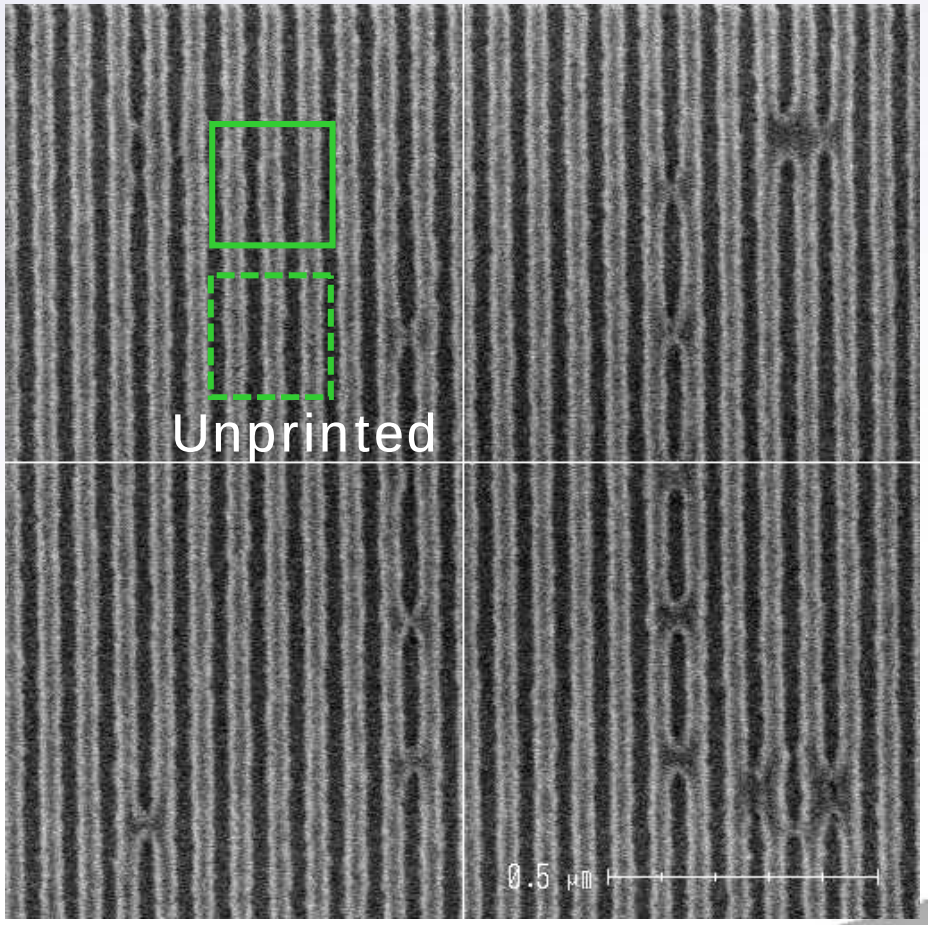
- Δ focus

pits become more printable at (–) defocus.



AIT

Designed Size: 90nm
SEVD : 17.1nm
Width : 32.3nm, depth : 2.0nm



Designed Size: 100nm
SEVD : 23.1nm
Width : 40.5nm, depth : 3.4nm

Wafer SEM

- LWR on the wafer SEM image makes gap between AIT and wafer image.
- When better resists are available in the future, this gap can be decreased.

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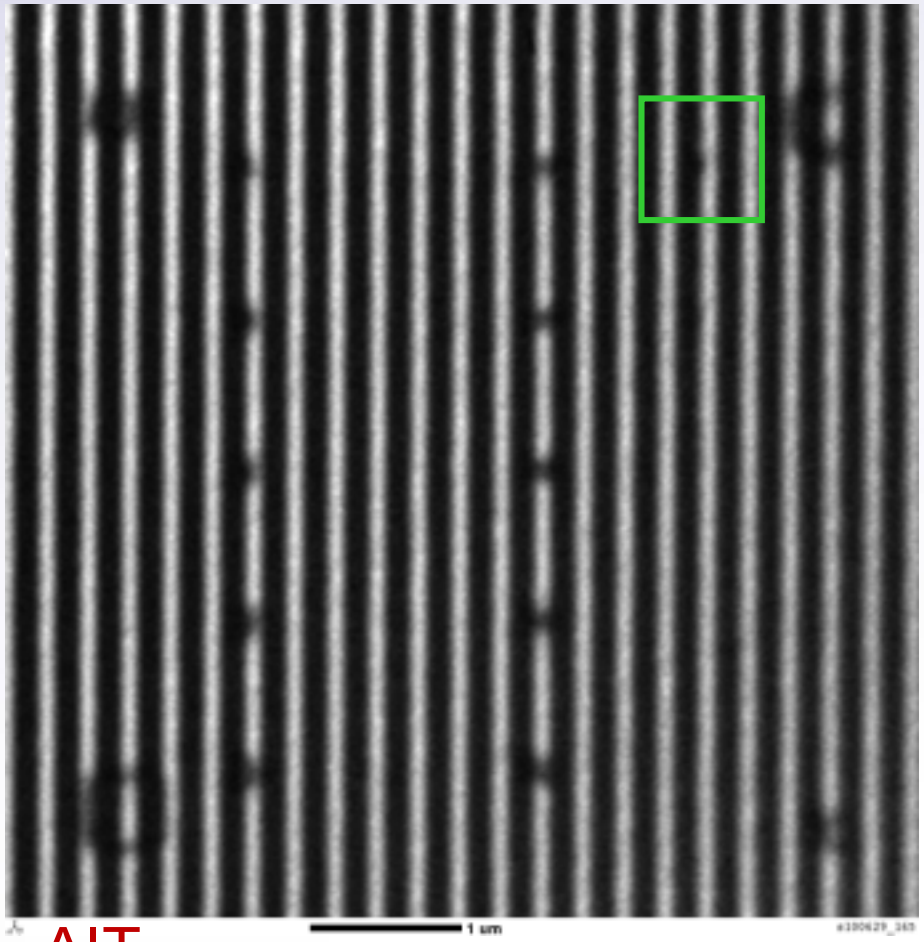
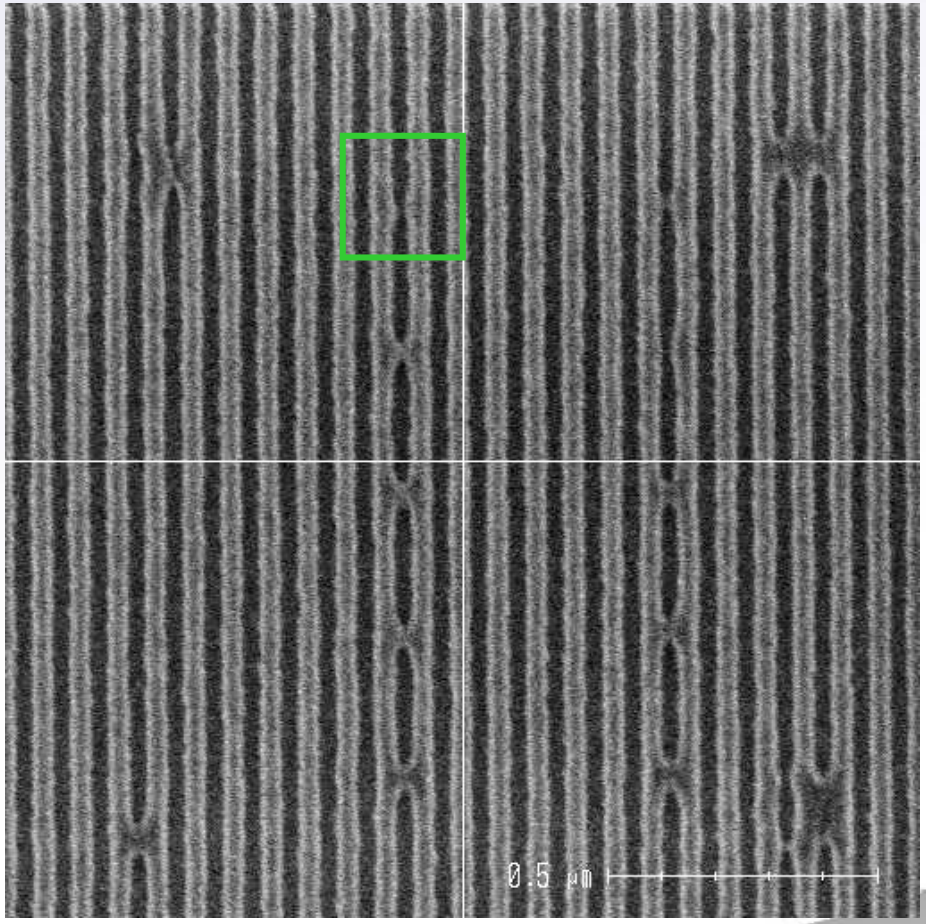
pits become less printable at (+) defocus.

+ Δ focus



AIT

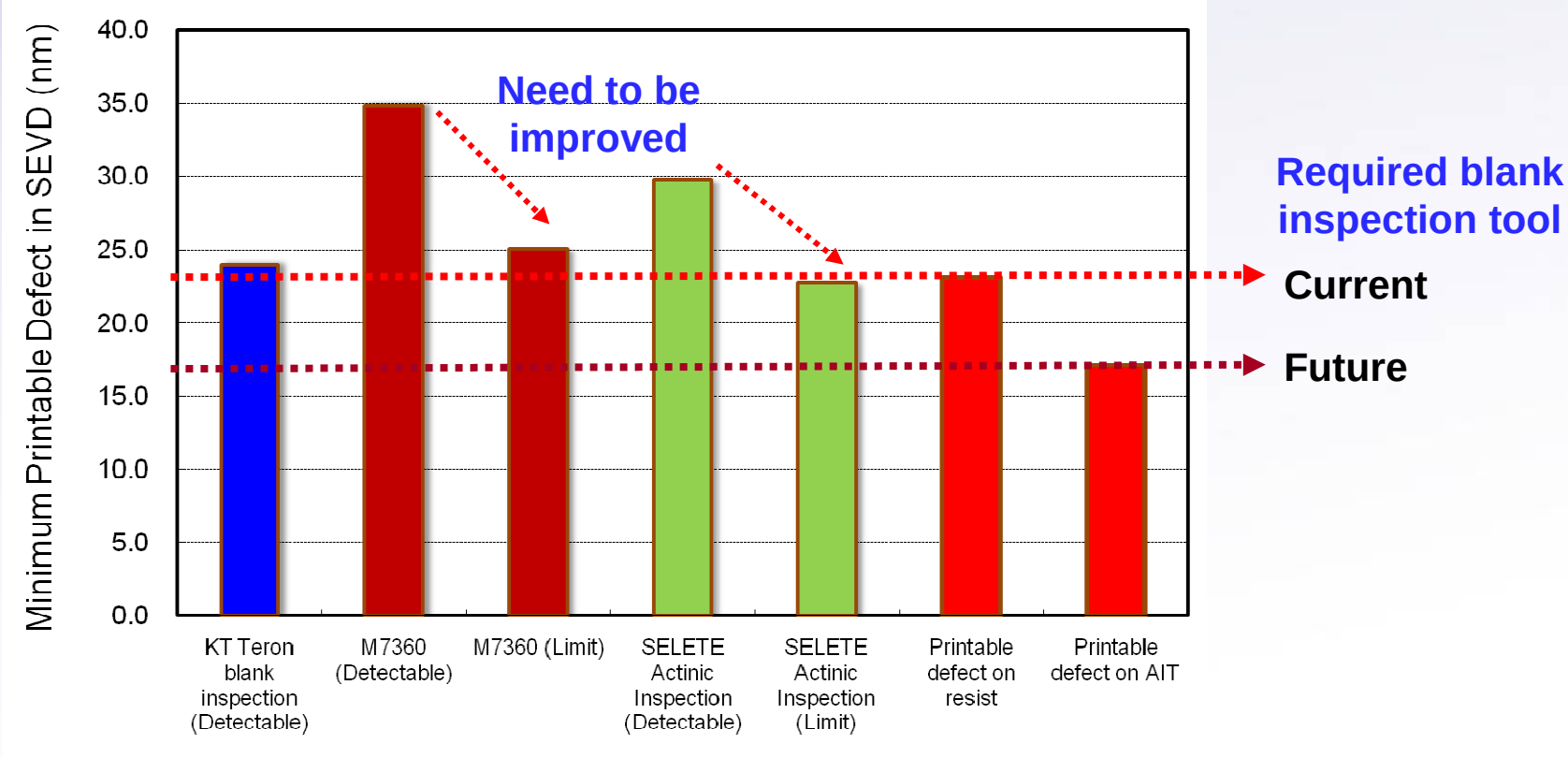
Designed Size: 100nm
SEVD : 23.1nm
Width : 40.5nm, depth : 3.4nm



Designed Size: 110nm
SEVD : 29.5nm
Width : 50nm, depth : 4.5nm

Wafer SEM

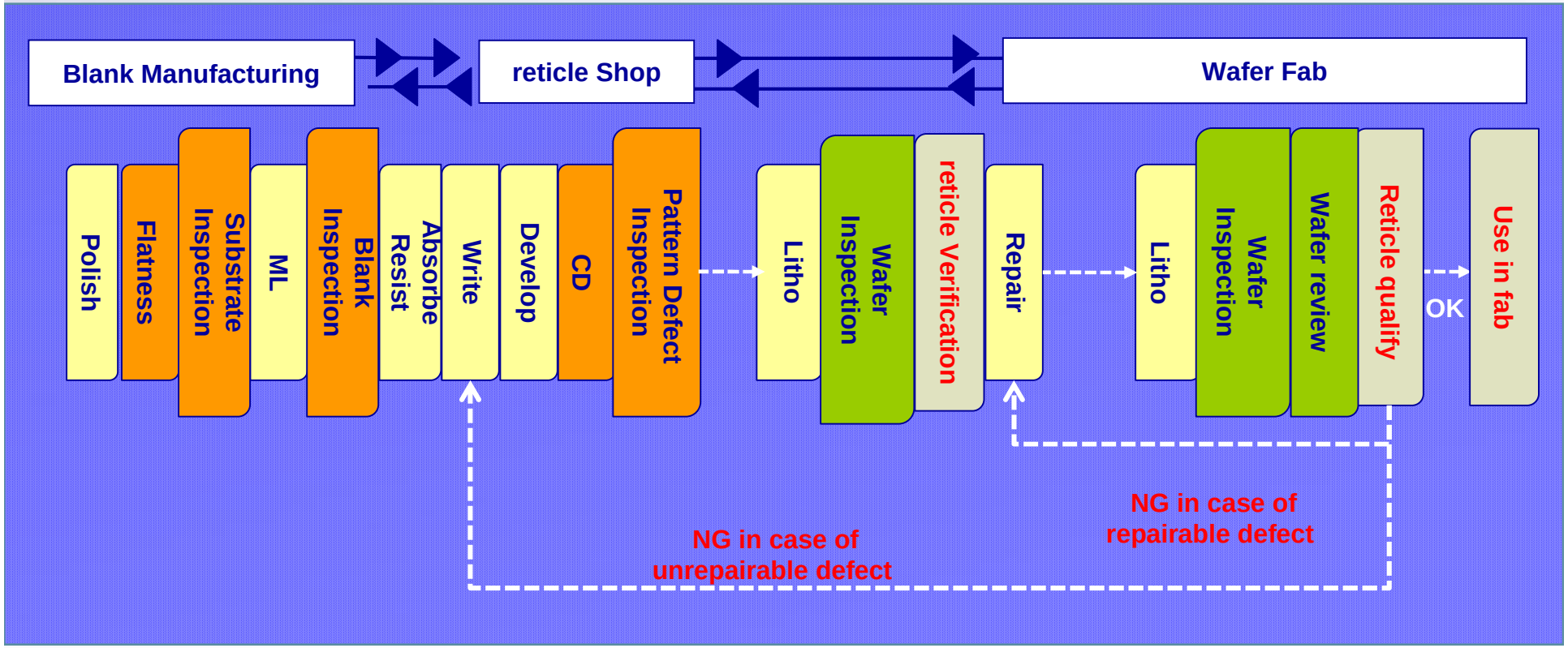
Required Blank Inspection Tool



- Currently blank inspection tool can detect the printable defect based on current resist and 35nm half pitch L/S pattern.
- But, we need blank inspection tool with better sensitivity when we have better resist in the future.

* KT Teron : Joshua Glasser, et. al, KLA Tencor, Proc. of SPIE Vol. Vol. 7748, 774808
** M7360 : Andy Ma, et. al, Intel Corp. Proc. of SPIE Vol. 7379, 73790I
*** SELETE : Takeshi Yamane, et. Al Proc. SPIE Vol. 7488, 74881B

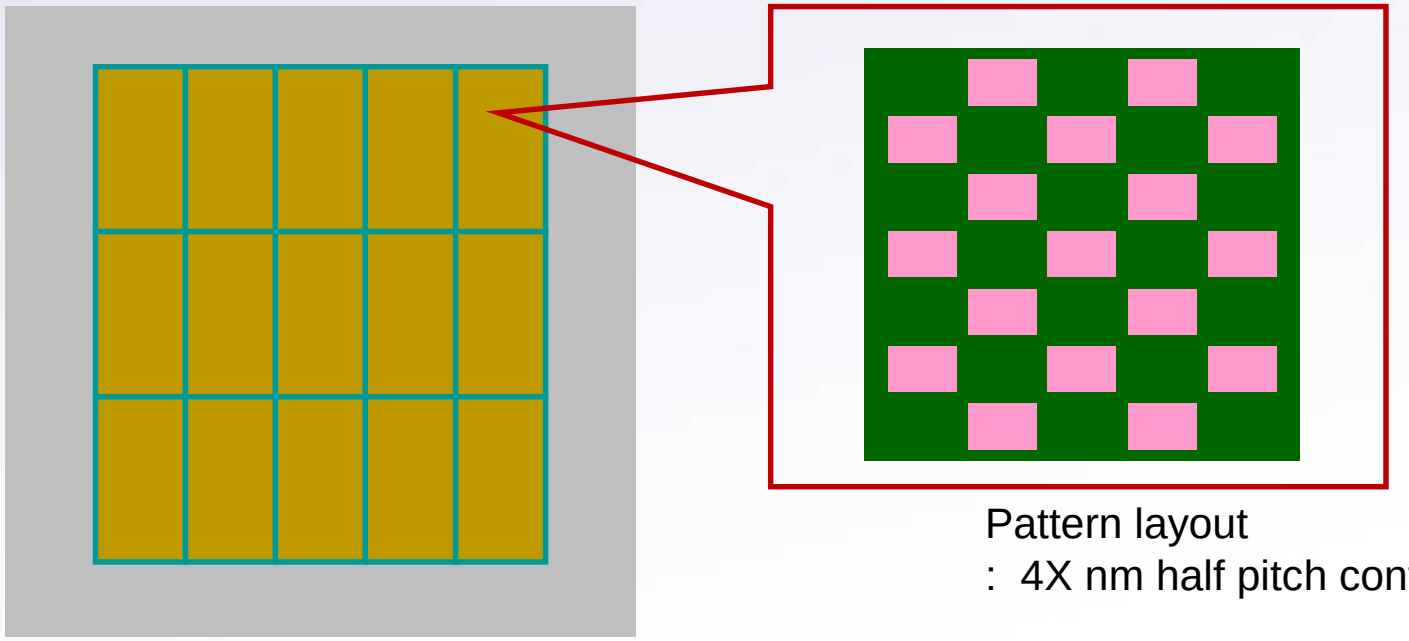
2) Defect Verification Methods



- Because we don't have enough infra-structure for blank inspection and defect verification at this time, we need to take advantage of wafer inspection and defect review for defect verification.
- We evaluated if wafer inspection can be used instead of EUV AIMS™.

Defect Printability using Real Defect

Full field EUV Mask



Pattern layout
: 4X nm half pitch contact array

- Full field EUV mask with 4Xnm half pitch contact array was used to evaluate the sensitivity of wafer inspection tool.
  - 4Xnm half pitch : minimize resist effect such as resolution and LWR.
  - Contact array : evaluate the sensitivity of inspection tool. And most of study is based on L&S pattern.
  - We used wafer inspection after dry etched wafer for better sensitivity

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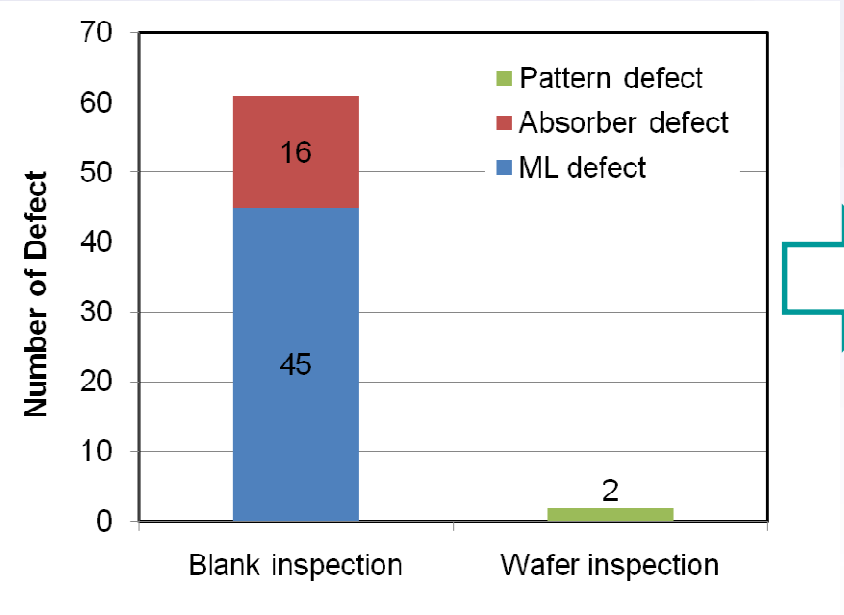
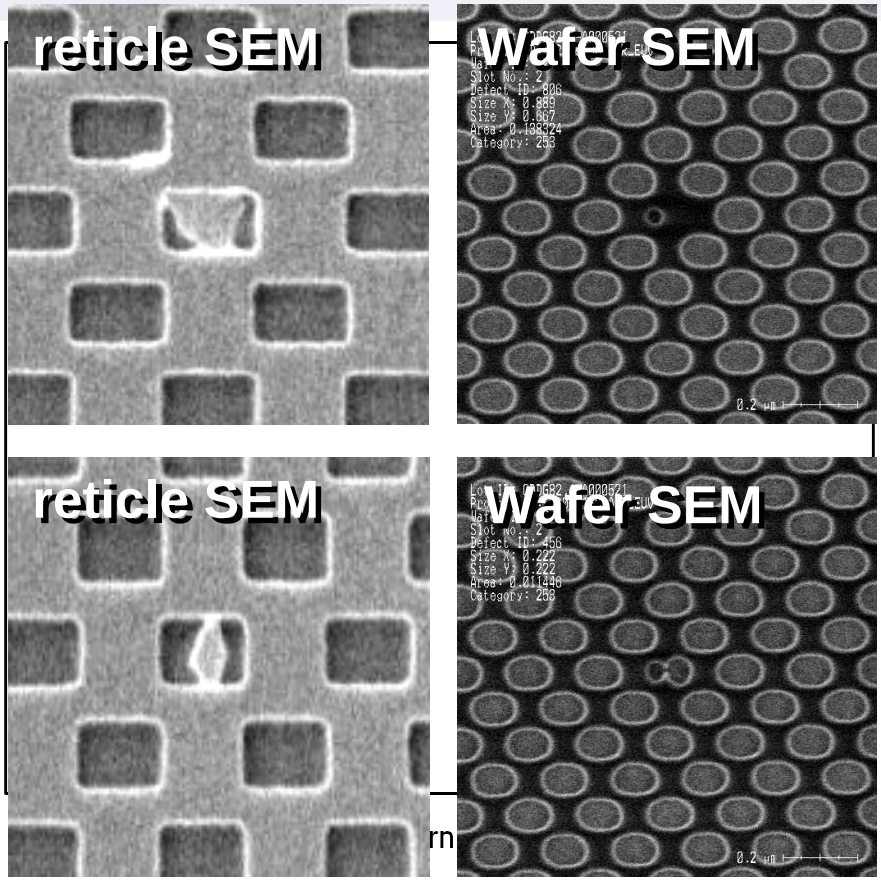
Classification and Detected Defect by Wafer Inspection



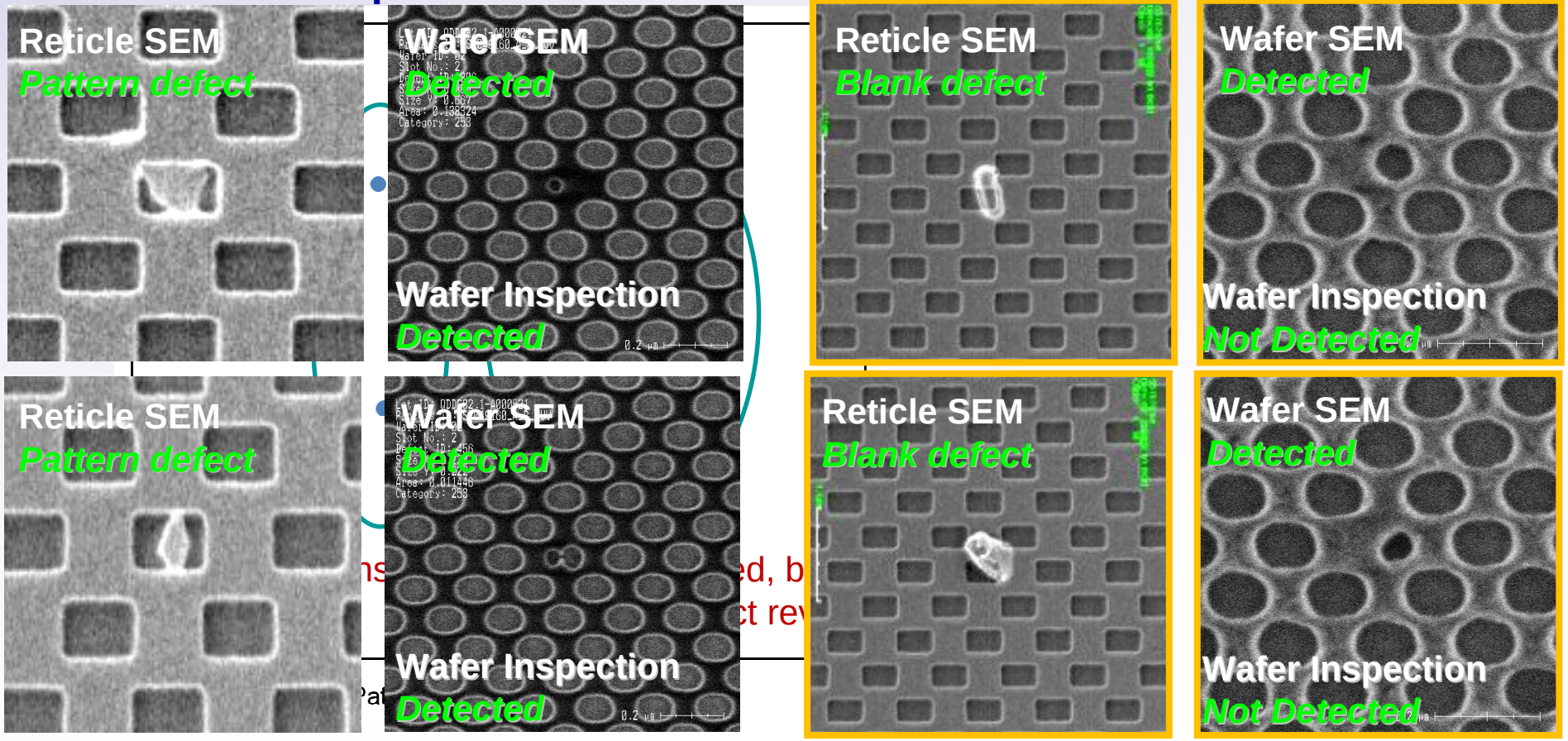
Repeater analysis with wafer inspection



- 2 pattern defects are inspected with wafer inspection tool.

  And No blank defects are not inspected with wafer inspection tool.
- After wafer inspection, we reviewed all defects based on pattern inspection and blank inspection data to evaluate sensitivity of wafer inspection is enough or not.

Defect Review Based on Blank & Pattern reticle Inspection Results



- 2 ML defects are printed on the wafer with change of contact area. However, those defects are not detected by wafer inspection tool.
- This means that wafer inspection itself can't replace EUV AIMS™.
- Wafer inspection and review based on blank defect map should be done for defect verification method or EUV AIMS™ should be ready on time.

Summary

- Programmed pit defect reticle is used to evaluate the required specification on blank inspection tool.
  - Printability of phase defects strongly relies on their locations. Most printable when the defect is located by absorber sidewall.
  - According to AIT results with 35 nm hp L/S, minimum printable size of pits could be 17 nm of SEVD. However 23.1nm in SEVD is printable from the EUV ADT.
- 4X nm half pitch contact array pattern is used to see if wafer inspection can replace the EUV AIMS™.
  - 2 pattern defects are inspected with wafer inspection tool.
  - 2 ML defects are reviewed by wafer review. However, those defects are not inspected by wafer inspection tool.
- Wafer inspection itself can't be used instead of EUV AIMS™. Wafer inspection and review should be done for defect verification method.

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The authors would like to thank for ...

- Photomask team in Samsung for reticle fabrication & evaluation
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- Technical staffs at SEMATECH and ASML in Albany for EUV ADT exposure
  - SEMATECH : Dominic Ashworth and Warren Montgomery
  - ASML : Sang-In Han

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