Accelerating the next technology revolution

Demonstration of CDU and LWR Performance Improvement Techniques on a Full-Field EUV Exposure Tool

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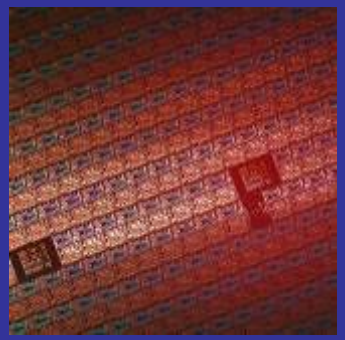

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Outline

- EUV CDU/LWR Requirements
- Demonstrated CDU Performance
  - Within-wafer CDU at ADI
  - Within-wafer CDU post-etch
  - Slit CDU at ADI
  - CD and CDU stability
- Demonstrated LWR Performance
  - LWR improvement from etch process
  - Full wafer LWR performance at ADI
  - Full wafer LWR performance post-etch
- Demonstration of Techniques CDU/LWR Improvement
  - Slit CDU Improvement
- Conclusions

EUV CDU/LWR Requirements

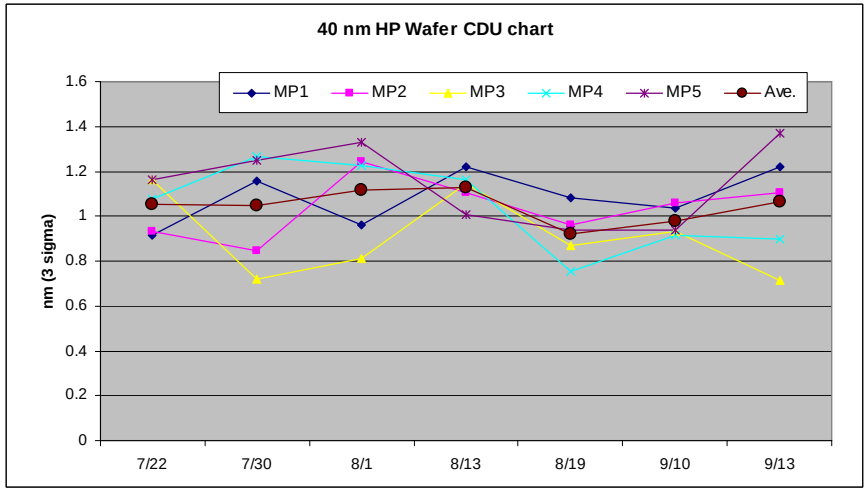
Year of Production	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*
DRAM ½ pitch (nm) (contacted)	*52*	*45*	*40*	*36*	*32*	*28*
Flash ½ pitch (nm) (un-contacted poly)	*37.8*	*31.8*	*28.3*	*25.3*	*22.5*	*20.0*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*54*	*45*	*38*	*32*	*27*	*24*
MPU physical gate length (nm) [after etch]	*29*	*27*	*24*	*22*	*20*	*18*
MPU gate in resist length (nm)	*47*	*41*	*35*	*31*	*28*	*25*
*Resist meets requirements for gate resolution and gate CD control (nm, 3 sigma) **†*	**3.0**	**2.8**	**2.5**	**2.3**	**2.1**	**1.9**
*Low frequency line width roughness: (nm, 3 sigma) <8% of CD ******	**3.7**	**3.2**	**2.8**	**2.5**	**2.2**	**2.0**

Source: 2009 ITRS

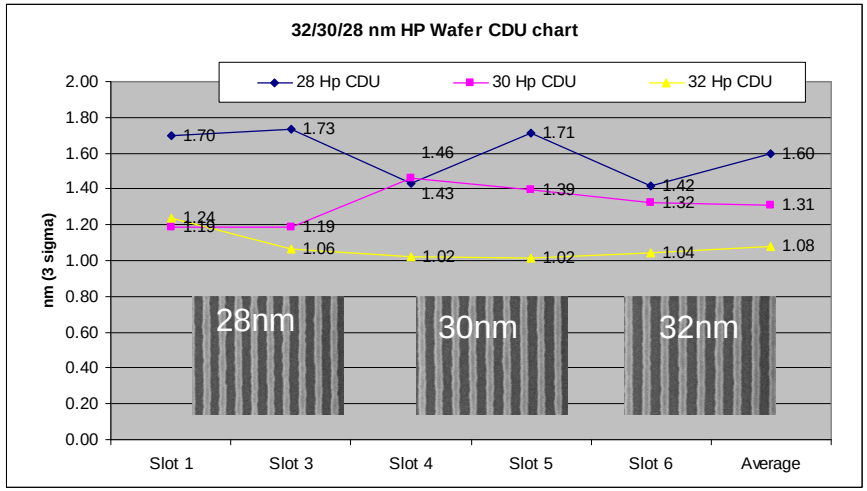
- To meet the production requirement, CDU and LWR of 300 mm full wafers need to meet the ITRS requirement
  - CDU requirement for 2013, 32 nm HP, is 2.1 nm (3 sig.)
  - LWR requirement for 2013, 32 nm HP, is 2.2 nm
  - CDU requirement for 2014, 28 nm HP, is 1.9 nm (3 sig.)
  - LWR requirement for 2014, 28 nm HP, is 2.0 nm

Demonstrated Within-Wafer CDU Performance - ADI

- CDU 40 nm HP trend chart
  - 1.04 nm (3 sigma) as wafer CDU demonstrated at 40 nm HP features
  - Stays stable for 8 weeks



- 32/30/28 nm HP CDU status
  - 32 nm CDU is 1.08 nm (3 sig.)
  - 30 nm CDU is 1.31 nm (3 sig.)
  - 28 nm CDU is 1.6 nm (3 sig.)
- Excellent ADI wafer CDU demonstrated on ADT+ ACT12

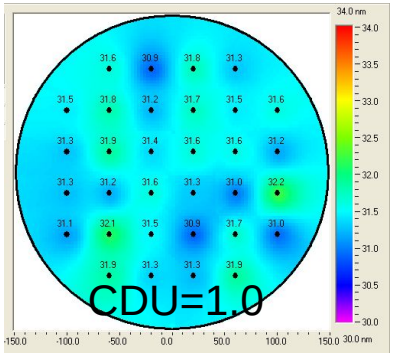


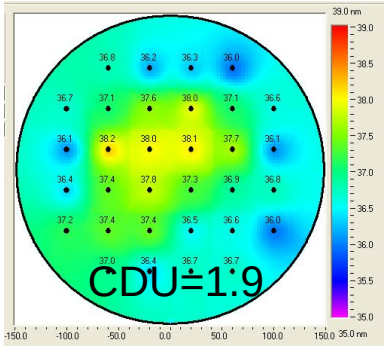
Demonstrated Within the Wafer CDU Performance – Post-Etch

Post-Develop

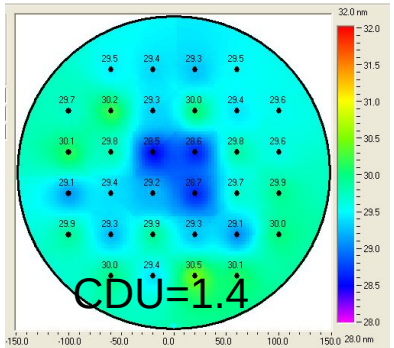
Post-etch

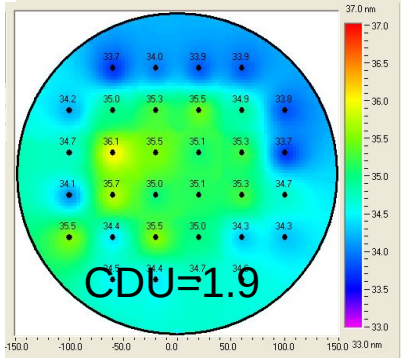
32 nm HP



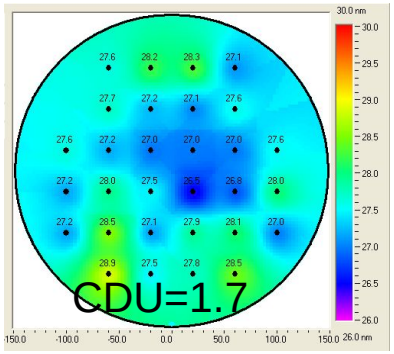


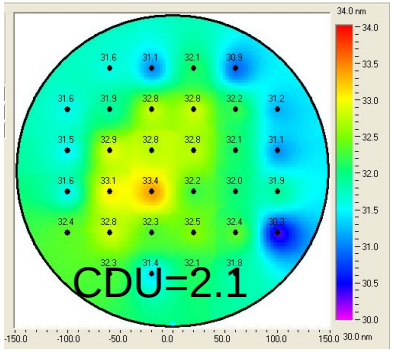
30 nm HP





28 nm HP

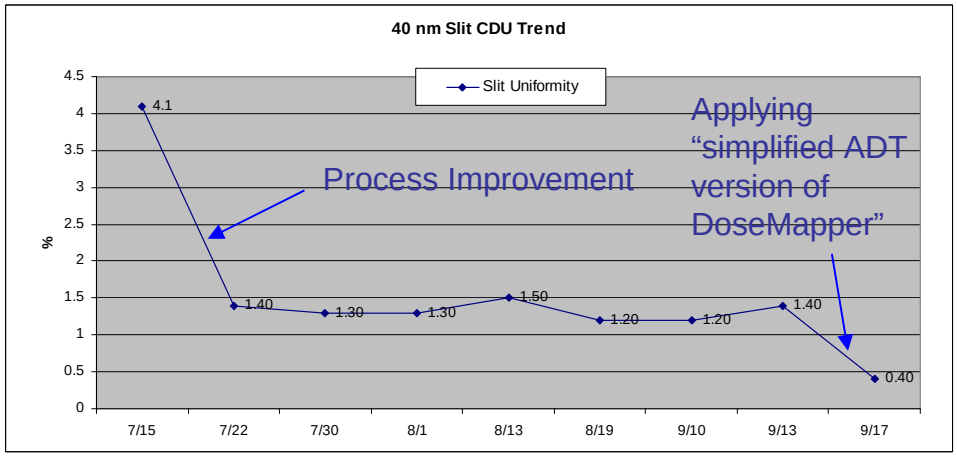




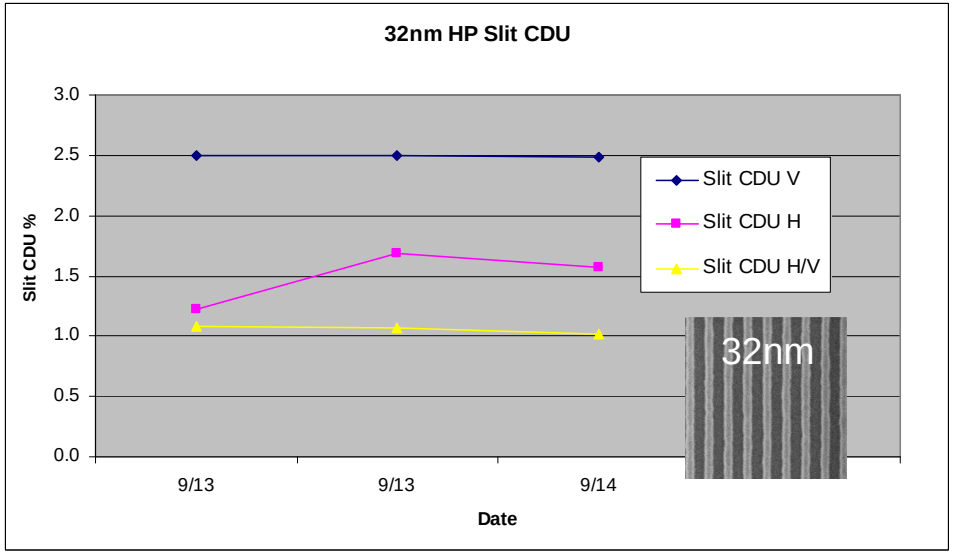
- Good full wafer CDU demonstrated on 32 nm/30 nm/28 nm HP features
- 1.9 nm CDU demonstrated at both 32 nm and 30 nm HP features while CDU at 28 nm feature is 2.1 nm
- Further improvement can be made by finetuning etch recipe

Demonstrated Slit CDU Performance - ADI

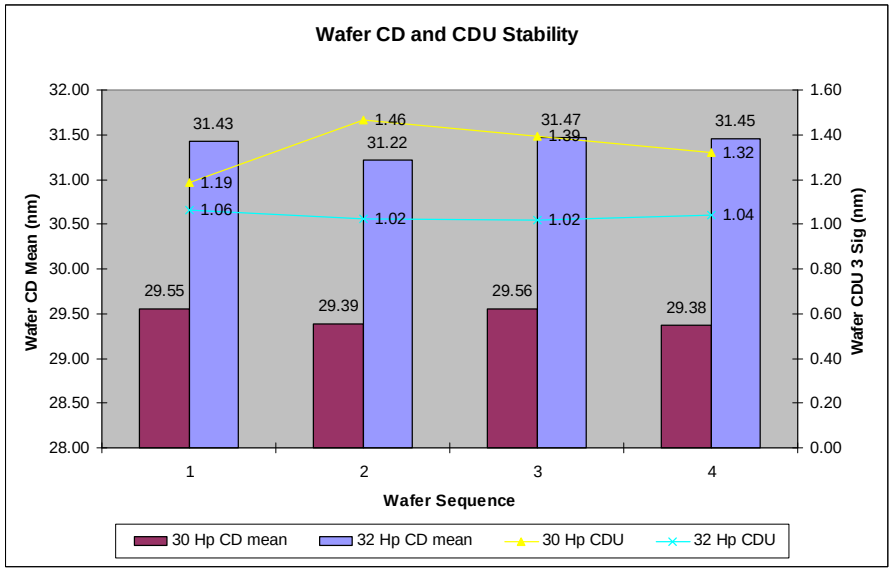
- 40 nm slit CDU trend
  - Slit CDU improved from 4.1% to 1.33% by migrating to new process
  - Further improvement to 0.4% after applying “simplified ADT version of DoseMapper”

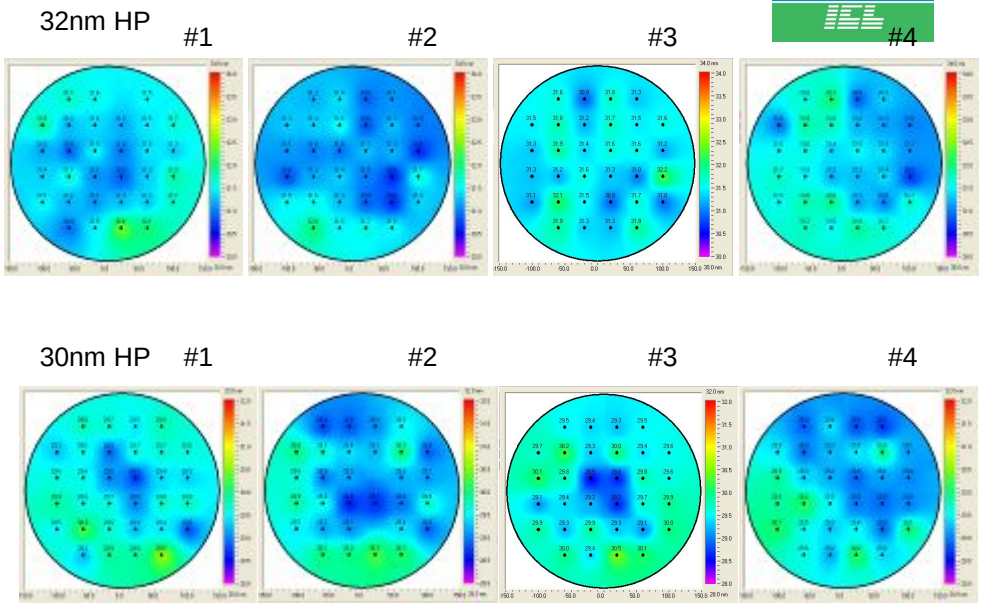


- 32 nm slit CDU status
  - First slit CDU data points demonstrate slit CDU as 1.1%, which is even better than 40 nm slit CDU
  - Keep collecting long-term trends to confirm the stability



CD and CDU Stability



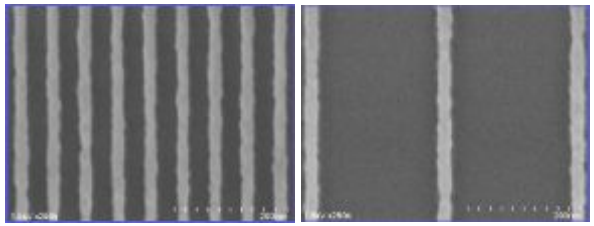


- On 4 wafers exposed in a row
  - Wafer-to-wafer mean CD variation less then 0.1 nm at 32 nm HP features
  - Wafer-to-wafer mean CD variation less then 0.2 nm at 30 nm HP features
  - Wafer CDU stays stable (1.02~1.04 nm, 3 Sig) at 32 nm HP features
  - Wafer CDU stays stable (1.19~1.46 nm, 3 Sig) at 30 nm HP features
  - Wafer CD signature stays stable

Demonstrated LWR Improvement from Etch Process

- 30 nm etching pattern transfer performance

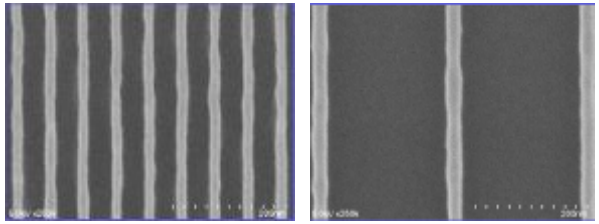
ADI



LWR=4.4 nm LWR=4.3 nm

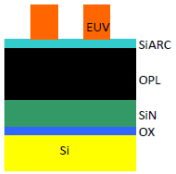
Etching

Post-Etch

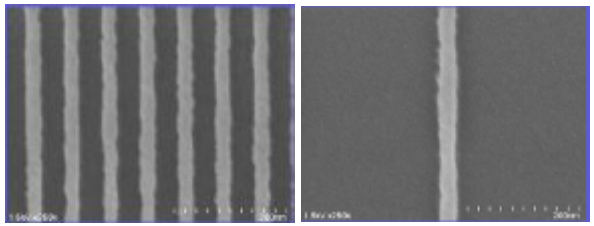


LWR=2.7 nm LWR=2.8 nm

- 35 nm etching pattern transfer performance



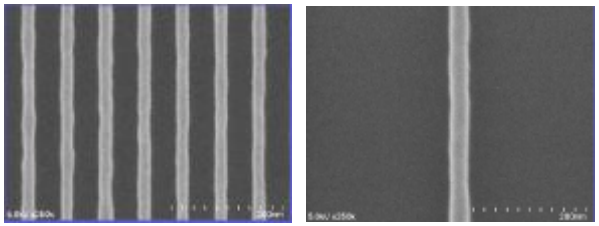
ADI



LWR=4.3 nm LWR=4.9 nm

Etching

Post-Etch

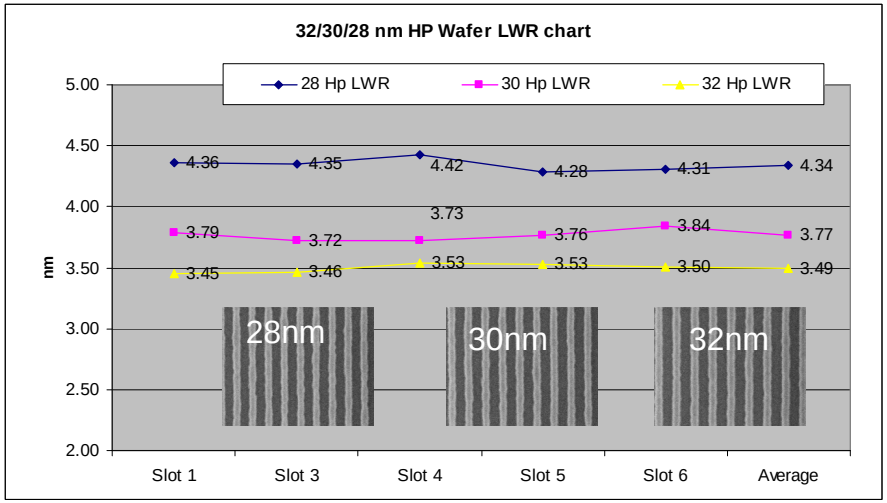


LWR=2.2 nm LWR=2.7 nm

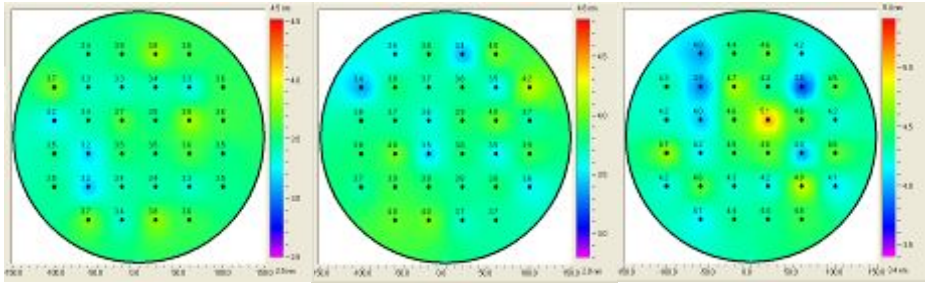
- 40%~50% LWR reduction achieved on 30 nm and 35 nm half-pitch features.

Demonstrated Full Wafer LWR Performance - ADI

- 32/30/28 nm LWR
  - 3.49 nm for 32 nm HP feature
  - 3.77 nm for 30 nm HP feature
  - 4.34 nm for 28 nm HP feature
- Process Tool
  - ASML ADT
  - TEL ACT12
- Process Film Stack
  - SEMATECH POR Resist
  - Silicon-Rich ARC
  - Organic Planarization Layer
  - SiN

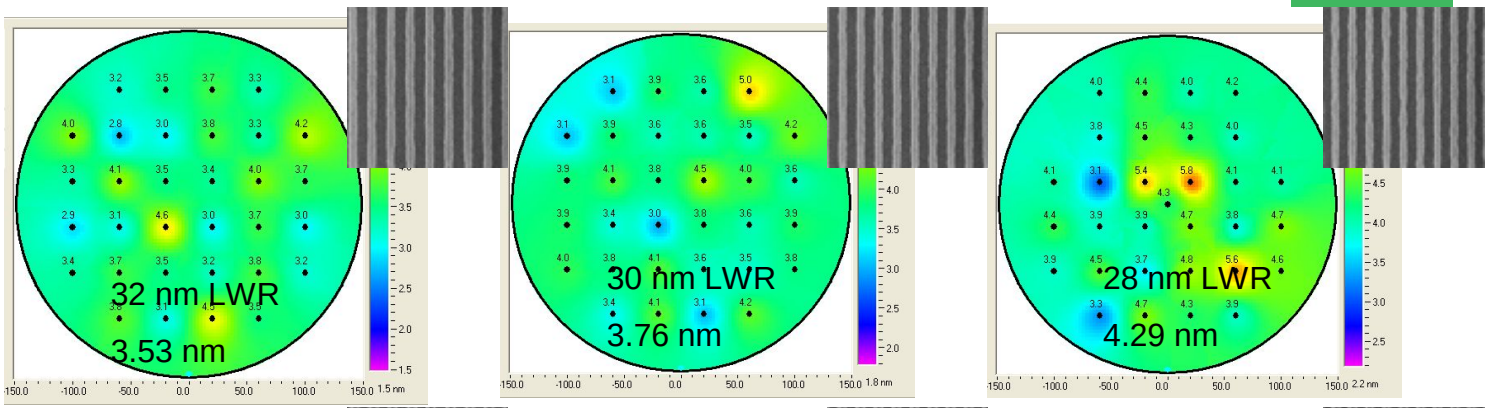


32 nm LWR	30 nm LWR	28 nm LWR
3.49 nm	3.77 nm	4.34 nm

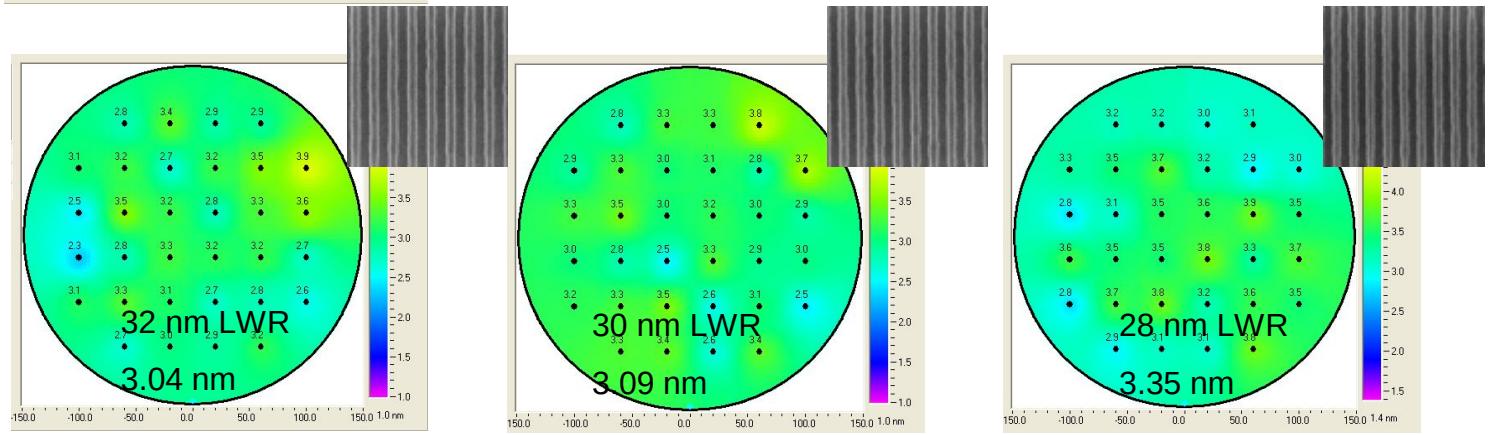


Demonstrated Full Wafer LWR Performance – Post-Etch

- Post-Develop



- Post-Etch

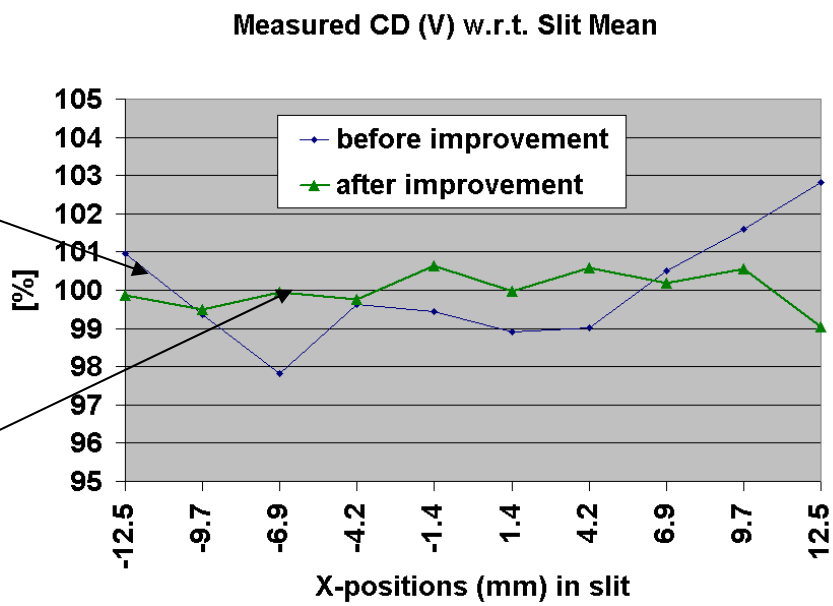


- Full wafer post-etch LWRs at 32/30/28 nm HP patterns are 3.04/3.09/3.35 nm, respectively.

Demonstration of Techniques for Slit CDU Improvement – Simplified ADT version of DoseMapper

Slit CDU = 2.5%
@ 32 nm HP Vertical Features

Slit CDU = 0.8%
@ 32 nm HP Vertical Features after applying "simplified ADT version of DoseMapper"



- "Simplified ADT version of DoseMapper" brings the slit CDU from 2.5% to 0.8% on a mask without CD shadowing effect correction.
- This function is proven to correct mask- or tool-induced slit non-uniformity.

Conclusion

- Capability of full-wafer CDU on an EUV tool set is demonstrated. Full-wafer CDUs are 1.0 nm (ADI), and 1.9 nm (post-etching), which can meet the ITRS requirement for 32 nm HP.
- Technique for further CDU improvement is demonstrated that bring the slit CDU down to 0.8 nm and wafer at 30 nm HP features.
- Etching capability to improve the LWR is demonstrated on a TEL etcher, which can reduce the LWR by 40% at 30 nm HP features.
- Integrated full-wafer ADI and etch process capability in an EUV process is demonstrated, for which CDU=1.9 nm meets the 32 nm HP node requirements while LWR=3.04 nm is close to the ITRS.
- Future improvement of the resist material, rinse material, novel smoothing process, and etch process is expected to close the LWR gap.

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