EUV Enabling Research and Development at the College of Nanoscale Science and Engineering

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Introduction:

Over the years, the College of Nanoscale Science and Engineering, has been a leader in the field of advanced lithography. CNSE's leadership has been manifested through strategic alliances with many of the major semiconductors industry leaders. In the area of 193 nm, CNSE had one of the earliest immersion systems. Companies, working through the INVENT Program, developed defect learning, imaging characterization and tool design (the print head development activities) that have facilitated much of the work needed to enable 193 nm manufacturing.

And now, as the semiconductor industry is in the midst of deciding whether to extend double patterning lithography or develop EUV lithography, CNSE is again amongst the main facilitators of technological learning. CNSE, working with SEMATECH, houses 2 of the primary imaging tools to enable EUV development (the Alpha Demo Tool from ASML and the Albany MET from Exitech). Also resident, as part of SEMATECH, is the Mask Blank Development Center (MBDC). In the MBDC, SEMATECH and Asahi Glass Corporation are developing advanced defect characterization with help from CNSE through its membership in SEMATECH.

Immersion Infrastructure

- In 2002, the Semiconductor industry researchers began to seriously consider the utilizing immersion to do semiconductor lithography. Two years later, the industry saw its first shipment of an immersion capable system with the ASML TWINSCAN AT:1150i; CNSE received that immersion. By late 2004 more than 16 chipmakers had used the 1150i to run some 10,000 test wafers.
- CNSE also purchased an ASML Twinscan AT 1200B
- TWINSCAN XT:1700i in Q3, 2006.

- Completing its immersion infrastructure CNSE received TWINSCAN XT :1950i (2009)

EUV imaging Tools at CNSE

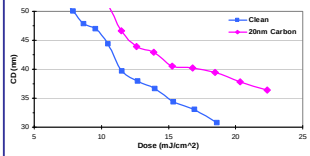
- CNSE takes delivery of world's first EUV R&D lithography tool (August 2006)
- CNSE has access to SEMATECH's Resist Materials Development Center (RMDC) Tool set with contains:
  - Berkeley MET exposure system (LBNL MET)
  - Albany MET (eMET)

** Many of these tools were purchase as part of the INVENT Program: The International Venture for Nanolithography (INVENT) initiative was a first-of-its-kind, global industry-university consortium for research and development, education and technology deployment for future generations of nanolithography applications at the College of Nanoscale Science and Engineering (A short list of papers generated by INVENT are listed below).

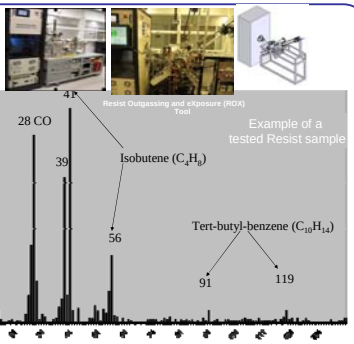
- INVENT EUV lithography program update
2007 International EUVL Symposium - October 28-31, 2007
- Initial experience establishing an EUV baseline lithography process for manufacturability assessment Emerging Lithographic Technologies XI, Proc. of SPIE Vol. 6517, 6517OU-1, (2007)
- Are EUV Resists Ready for the 32nm Mode? 51st EIPBN (Electron, Ion, and Photon Beam Technology and Nanofabrication) Conference - May 29-June 1, 2007
- Trends in the Cost of Photolithography Development and an Outlook for the Future
- Infineon Development at Albany 2005 International Symposium on Extreme Ultraviolet Lithography - November 7, 2005
- Imaging with Immersion Technology at Albany NanoTech September 12, 2005

Outgassing Focus at CNSE:

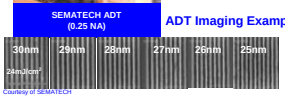
Printing results on Berkely METEUV MET
–contamination has larger effect on dose than predicted by reflectivity change



- Target CD of 40 nm features were printed and measured for both clean and contaminated fields on the mask
- Approximately 3x larger increase in dose required to print feature than was predicted by reflectivity loss of contamination on mask!



Advanced EUV Process work Taking place at CNSE (Examples)



ADT Imaging Example

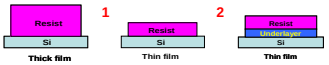
Courtesy of SEMATECH

Early ADT papers:
•INVENT EUV lithography program update 2007 International EUVL Symposium - October 28-31, 2007
•Initial experience establishing an EUV baseline lithography process for manufacturability assessment
•Emerging Lithographic Technologies XI, Proc. of SPIE Vol. 6517, 6517OU-1, (2007)

Fundamental Materials Research

Funded by SEMATECH

I. Ultra-thin EUV Resist and Underlayer Fundamentals

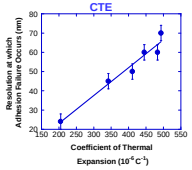


Underlayer UL8

CTE varied by changing crosslinker and TAG level

Better adhesion observed at lower CTE

Resist Adhesion vs. Underlayer CTE



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** Please see the talk 'Understanding Underlayer Physical Properties and its Effect on EUV Resist'

CNSE Alliance Mode has allowed CNSE to partner in a number of technological fields:
- •3D interconnect
- •Advanced Equipment testing
- •EUV mask defect learning
- •Device development
- •Nano imprint development (templates)
- •E-beam lithography

VB300 E-beam Litho
Minimum CD, 15 nm +/- 10% at 100 um field

Future plans:

- CNSE will continue to partner with new and existing companies
- •Advanced processing tool and facilities (located at CNSE) will continue provide a venue for innovation
- •Student growth and development will remain a core focus area
- •CNSE will continue to leverage its partnerships to provide valuable information to industry