22nm node imaging and beyond: When will EUV take over?

ASML: Eelco van Setten, Orion Mouraille, Friso Wittebrood, Mircea Dusa, Koen van Ingen-Schenau, Jo Finders, Kees Feenstra

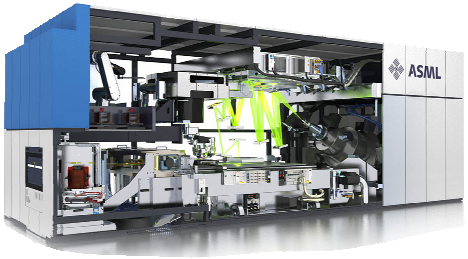
IMEC: Joost Bekaert, Bart Laenens, Vicky Philipsen, Monique Ercken, Eric Hendrickx, Geert Vandenberghe

Presentation outline

- Introduction
- Towards a working SRAM
- Scaling
- When will EUV take over?

Litho solutions at the 22nm node

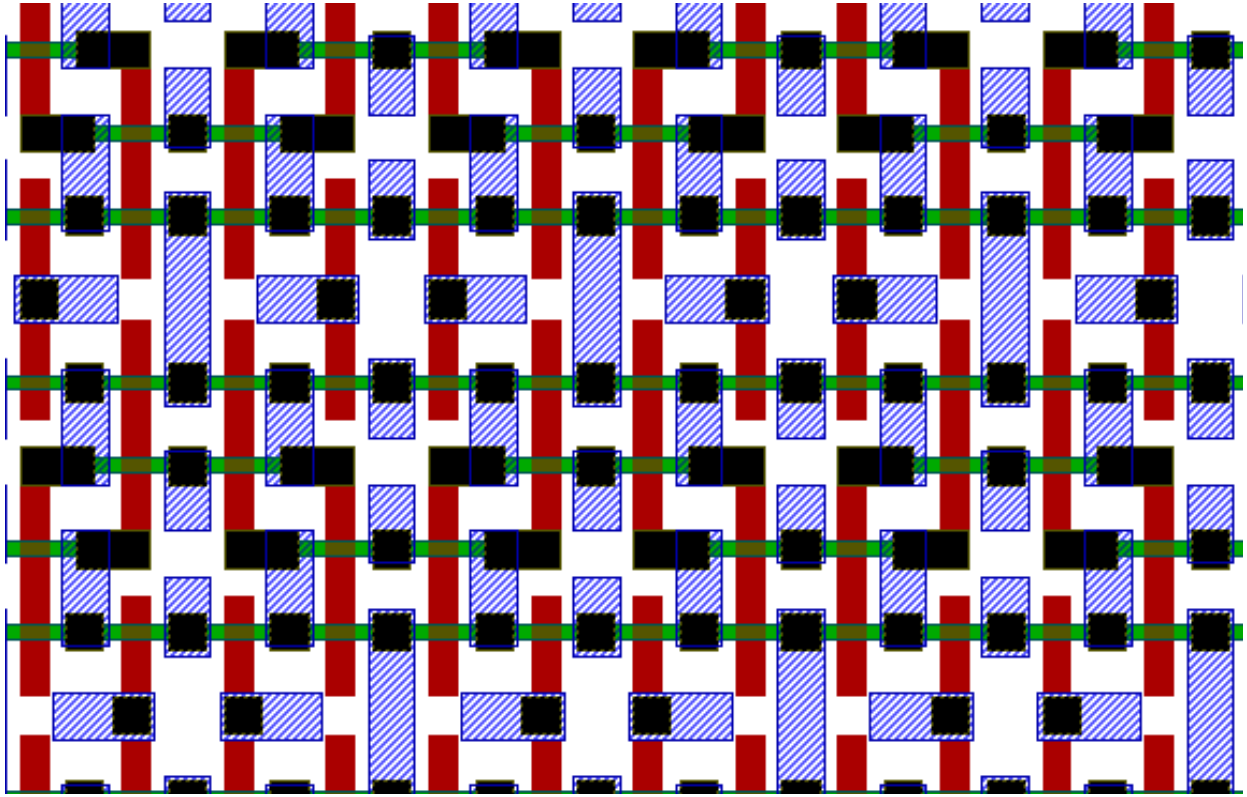
- 22nm node options:
  - Scale down 32nm node process using ArF immersion
  - Switch to new technology: EUV



	ArF immersion	EUV
Technology	Established, in HVM	1st pre-production system shipped
Enhancement products	Extensive portfolio (eg. Flexray, DoseMapper)	Being developed
Infra-structure (process, reticles)	Well-developed	Maturing
Imaging	Very low k1, double patterning required	High k1, single exposure

EUV is compared to ArF immersion for 22nm node SRAM back-end layers

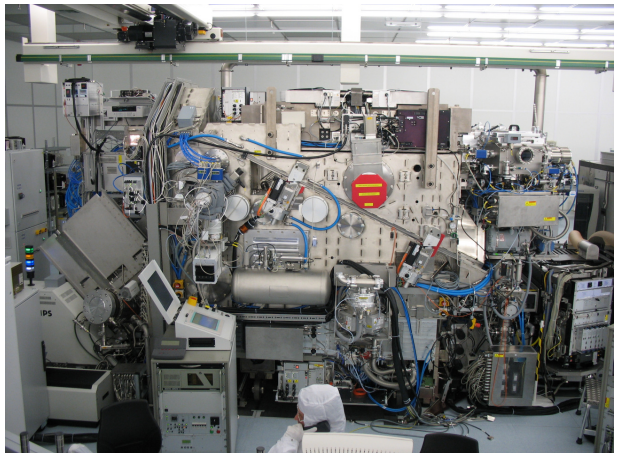
- 1:1 comparison for 22nm node FinFET type SRAM cell => identical clips on ArFi double patterning mask and reflective EUV mask



EUV is compared to ArF immersion for 22nm node SRAM back-end layers

- 1:1 comparison for 22nm node FinFET type SRAM cell => identical clips on ArFi double patterning mask and reflective EUV mask
  - EUV: Alpha Demo Tool at IMEC => NA = 0.25, σ = 0.50
  - ArFi: XT:1950Hi with Flexray => NA = 1.35, free-form source, XY-polarization

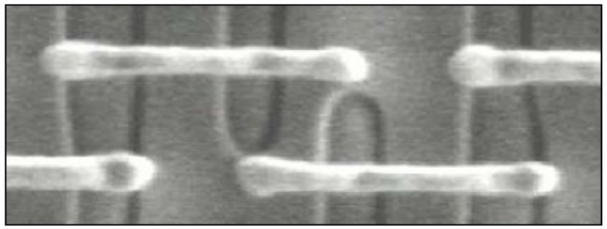
- Compare imaging performance, identify critical areas for HVM



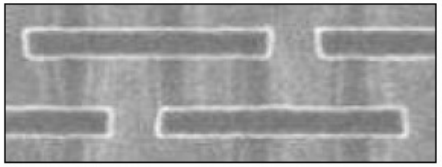
SRAM roadmap shows ~50% bit-cell size reduction per node

- Nodes evaluated:
  - CDU: 22nm node ArFi and EUV
  - Resolution: 16nm node EUV

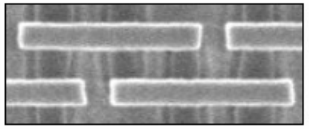
Node [nm]	Half Pitch [nm]	Cell size [µm2]	Cell size shrink
65	110	0.570	
45	80	0.346	40%
32	56	0.171	51%
22	**40**	**0.078**	**54%**
16	28	0.038	51%



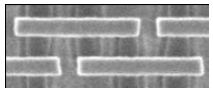
65 nm, 0.570 um^2



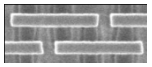
45 nm, 0.346 um^2



32 nm, 0.171 um^2



22nm, 0.078 um^2



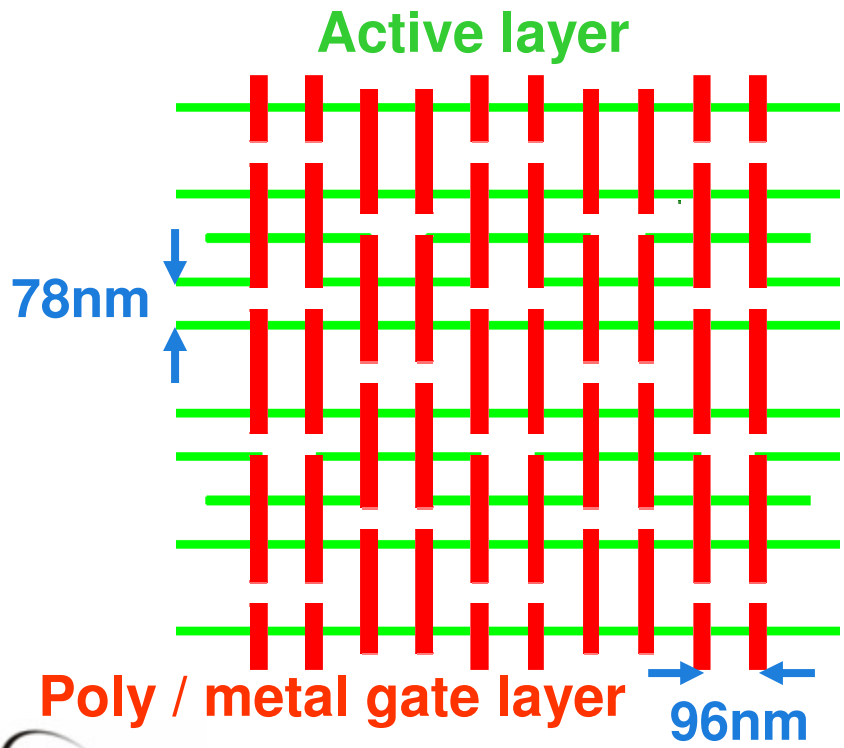
16nm, 0.038 um^2

NOTE, 22 and 16nm data is scaled 32nm picture to illustrate cell-size reduction

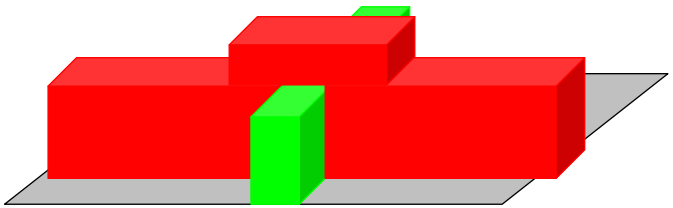
Intel Corporation – IDF 2009

Critical layers of 22 nm node FinFET SRAM design

- Critical layers of FinFET SRAM:
  - Active layer patterned as fins in Si
  - Poly or metal gate layer
  - Contact hole layer
  - Metal-1 layer
- Bit-cell size = 2 x 0.096 x 5 x 0.078 = 0.075µm²



Poly/metal gate wrapped around fin



Active fin

Critical layers of 22 nm node FinFET SRAM design

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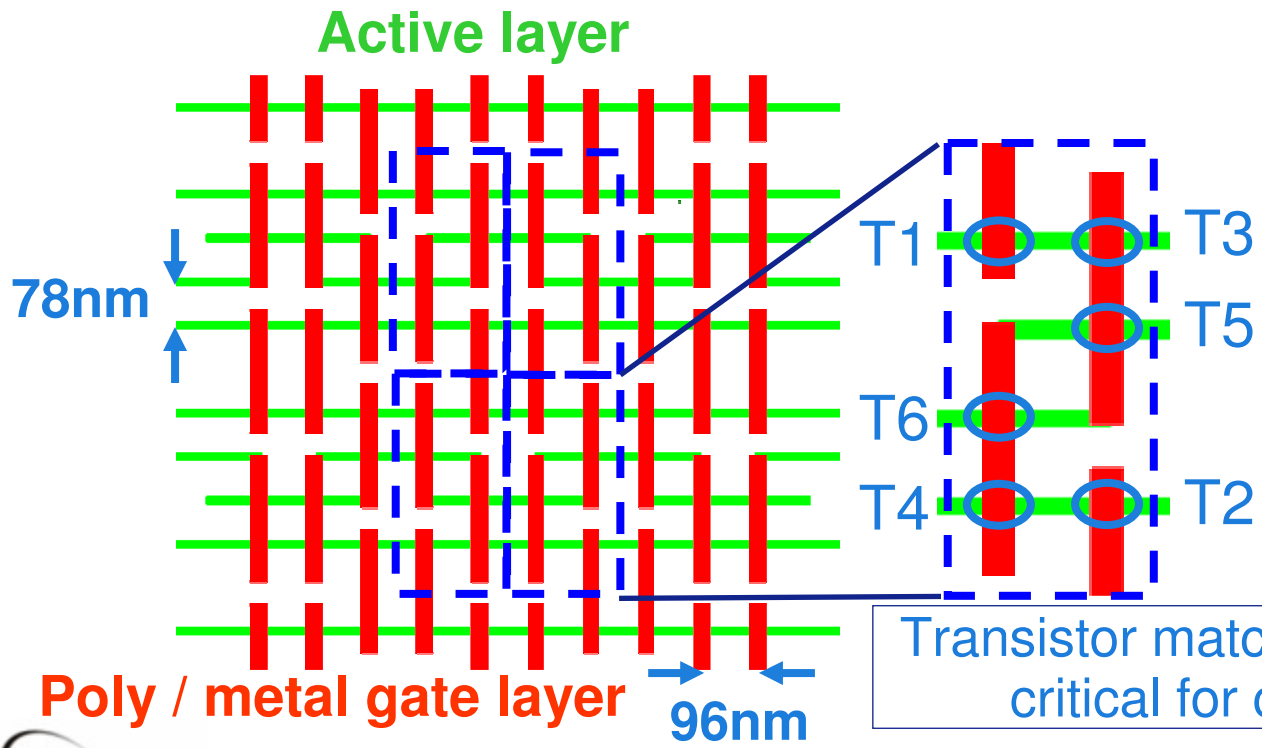
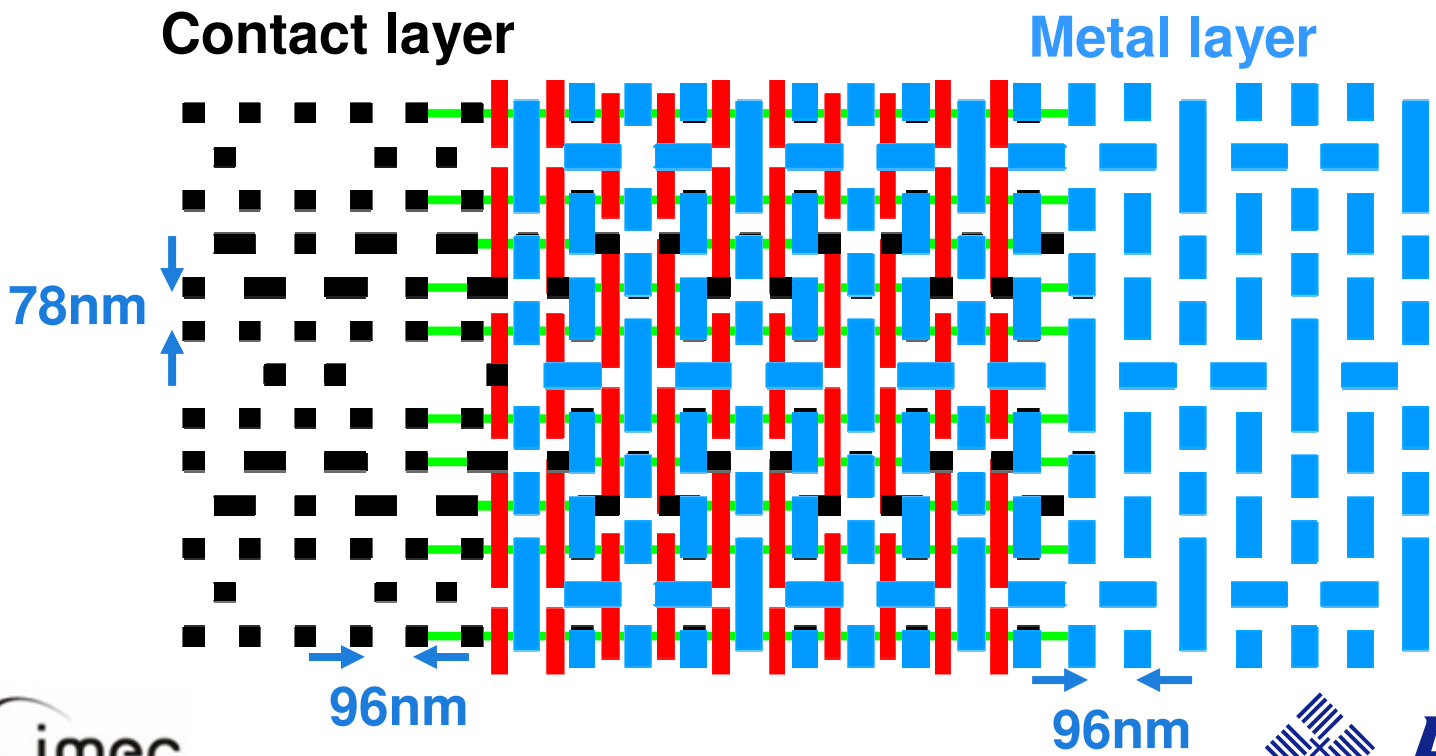


6-Transistor 1-bit cell:
High speed, low power consumption at expense of silicon area (~150F²) => Bit-density is ~25 x smaller than DRAM (6F²)

Transistor matching = CD control critical for cell operation

FinFET SRAM contact and metal-1 layers have complex 2D lay-out at gate/active pitch

- 22nm node Contact hole and Metal-1 layer patterning requires:
  - Design split to relax minimum pitch + double patterning (eg. Litho-Etch-Litho-Etch)
  - Single exposure EUV...



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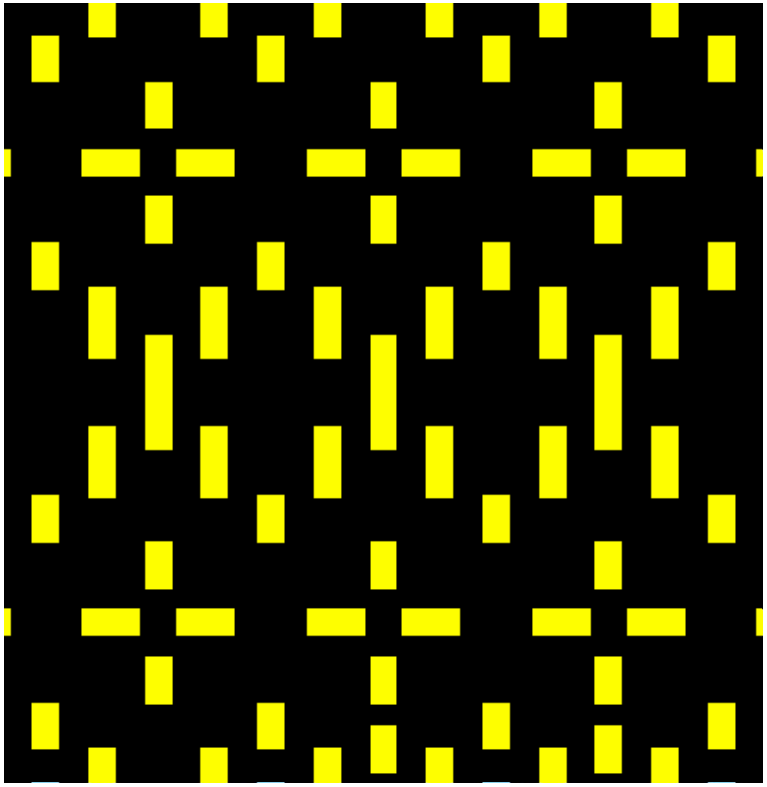
ArFi masks: Design split and Source Mask Optimization

- Complex OPC, simultaneously optimizing the mask and illumination pupil to benefit fully from the Flexray illuminator
  1. Split design in 2 identical layers for double patterning

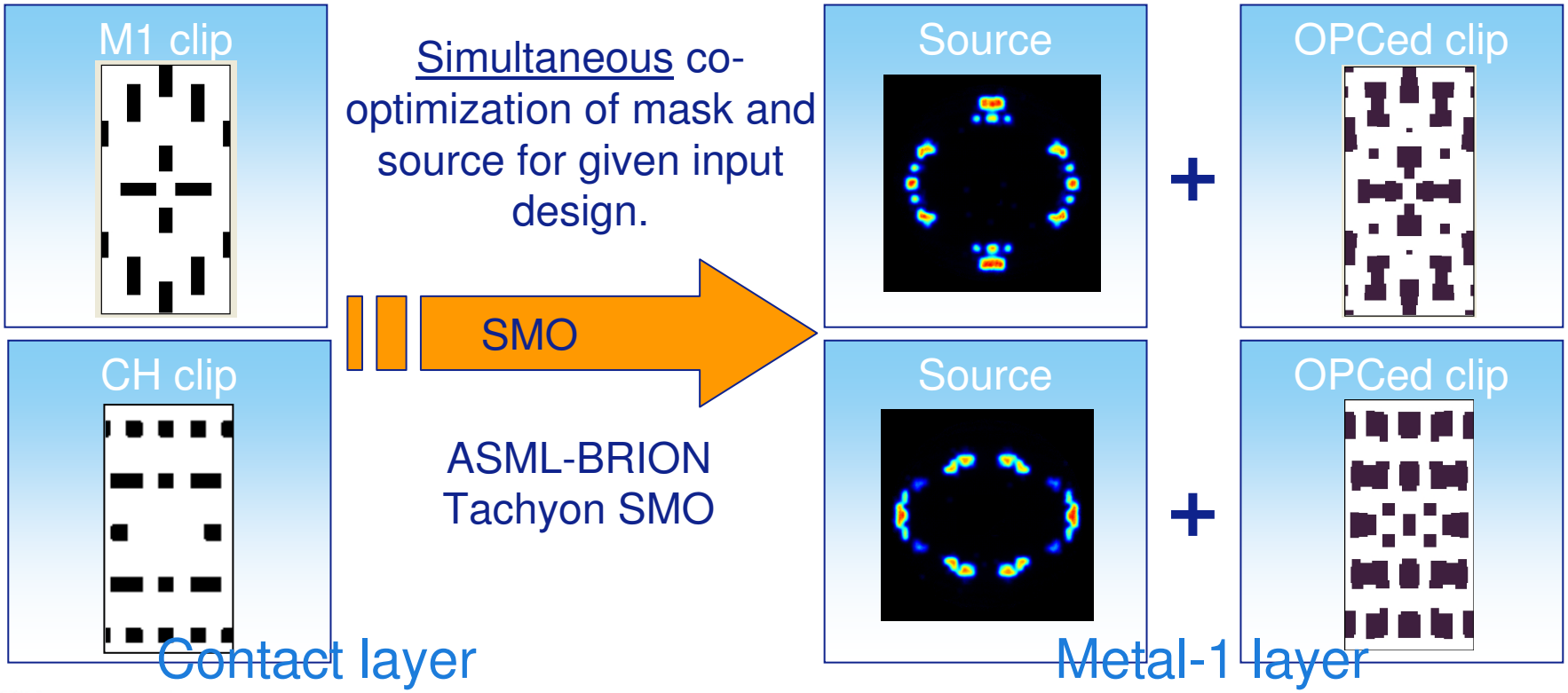
Contact layer



Metal-1 layer

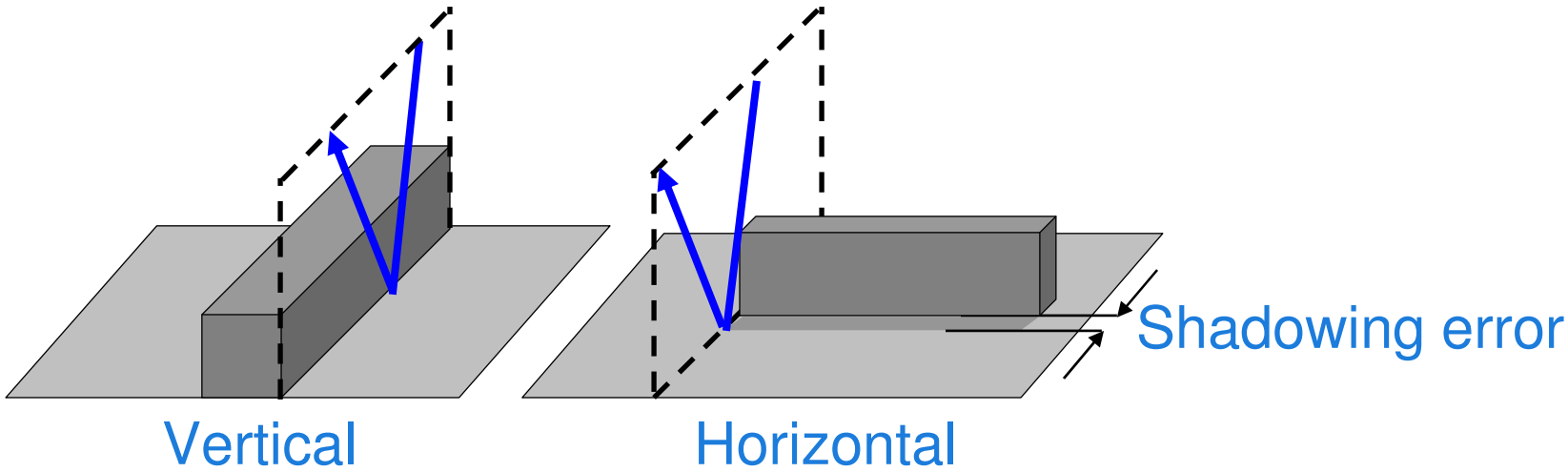
ArFi masks: Design split and Source Mask Optimization

- Complex OPC, simultaneously optimizing the mask and illumination pupil to benefit fully from the Flexray illuminator
  1. Split design in 2 identical layers for double patterning
  2. Apply Source Mask Optimization (SMO) on splitted design clips



EUV specific mask OPC: Shadowing and flare correction

- 6º angle of incidence: CD error on wafer level due to shadow from mask features => HV offset that changes across slit



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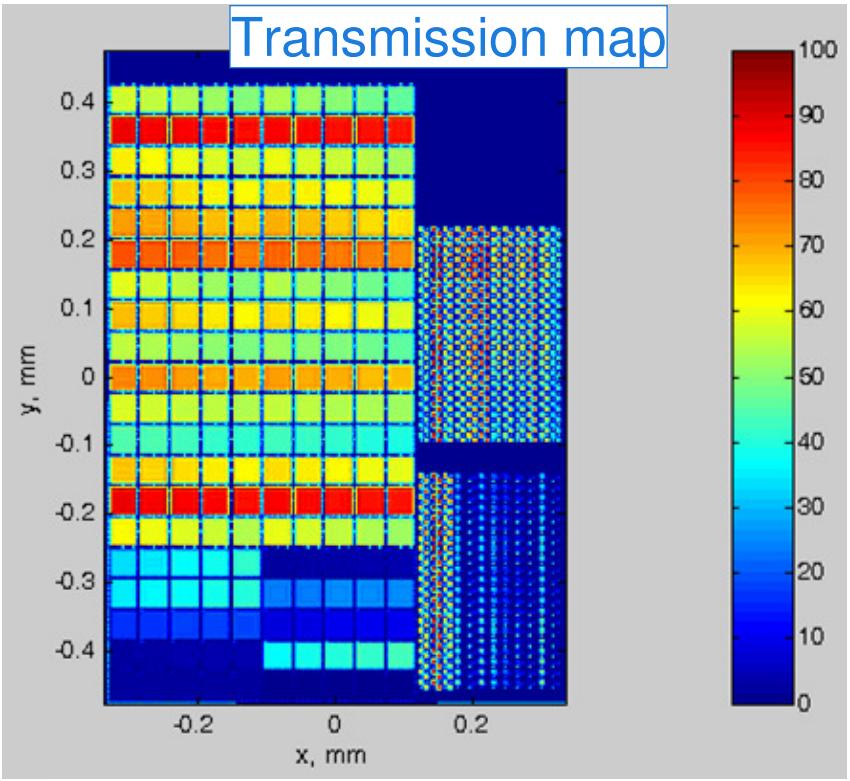
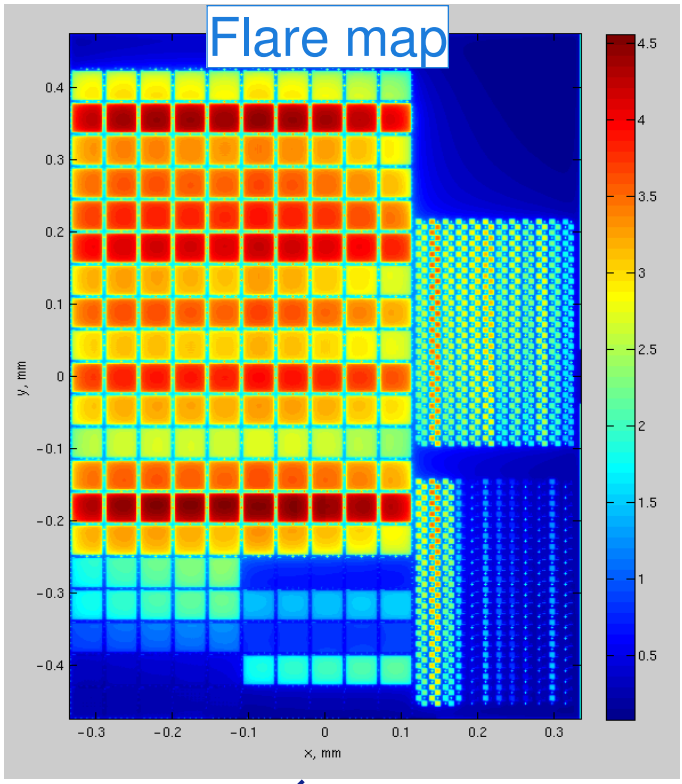
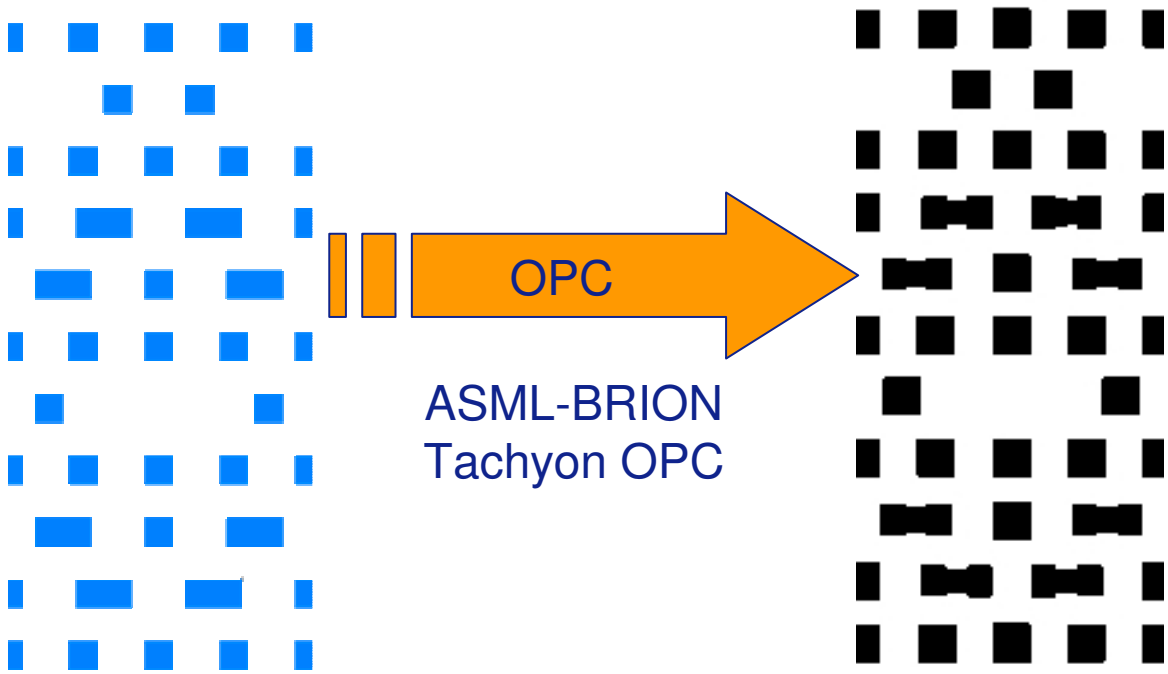
- Higher flare than ArF i system: Feature correction depending on feature density



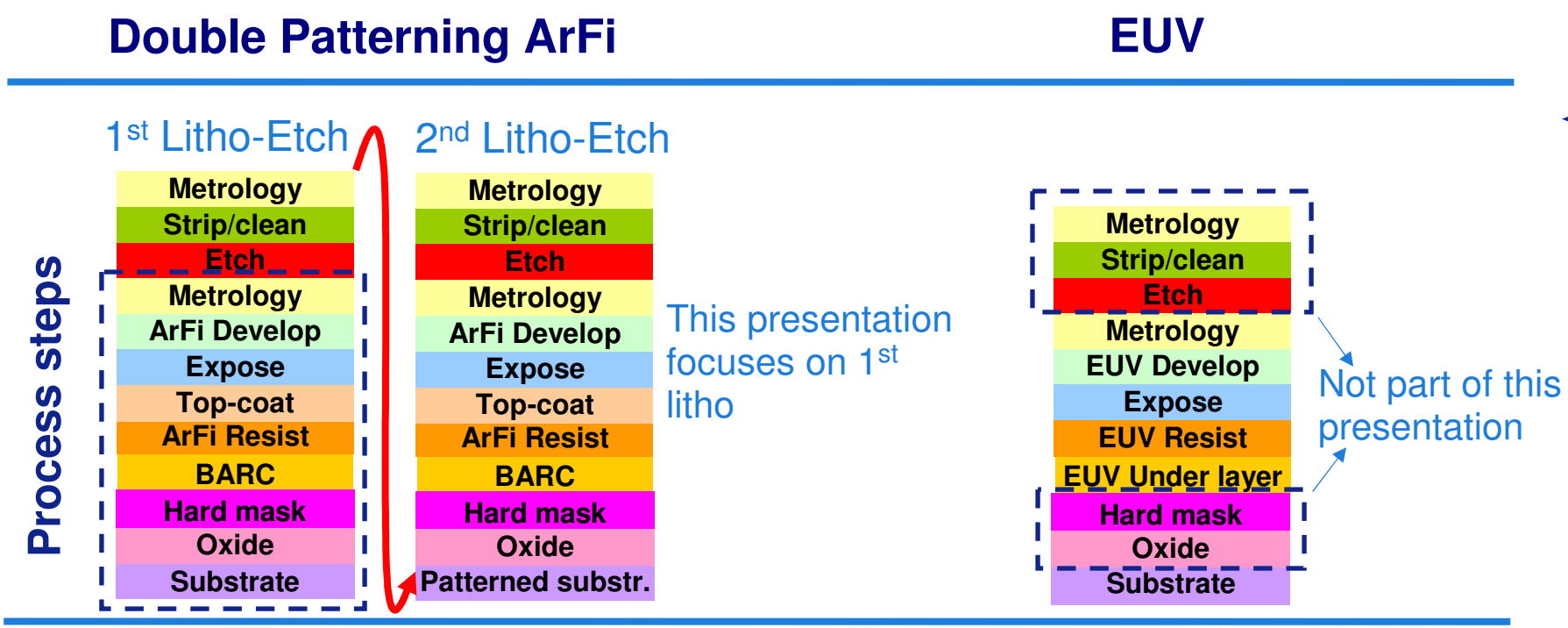


EUV specific mask OPC: Shadowing and flare correction

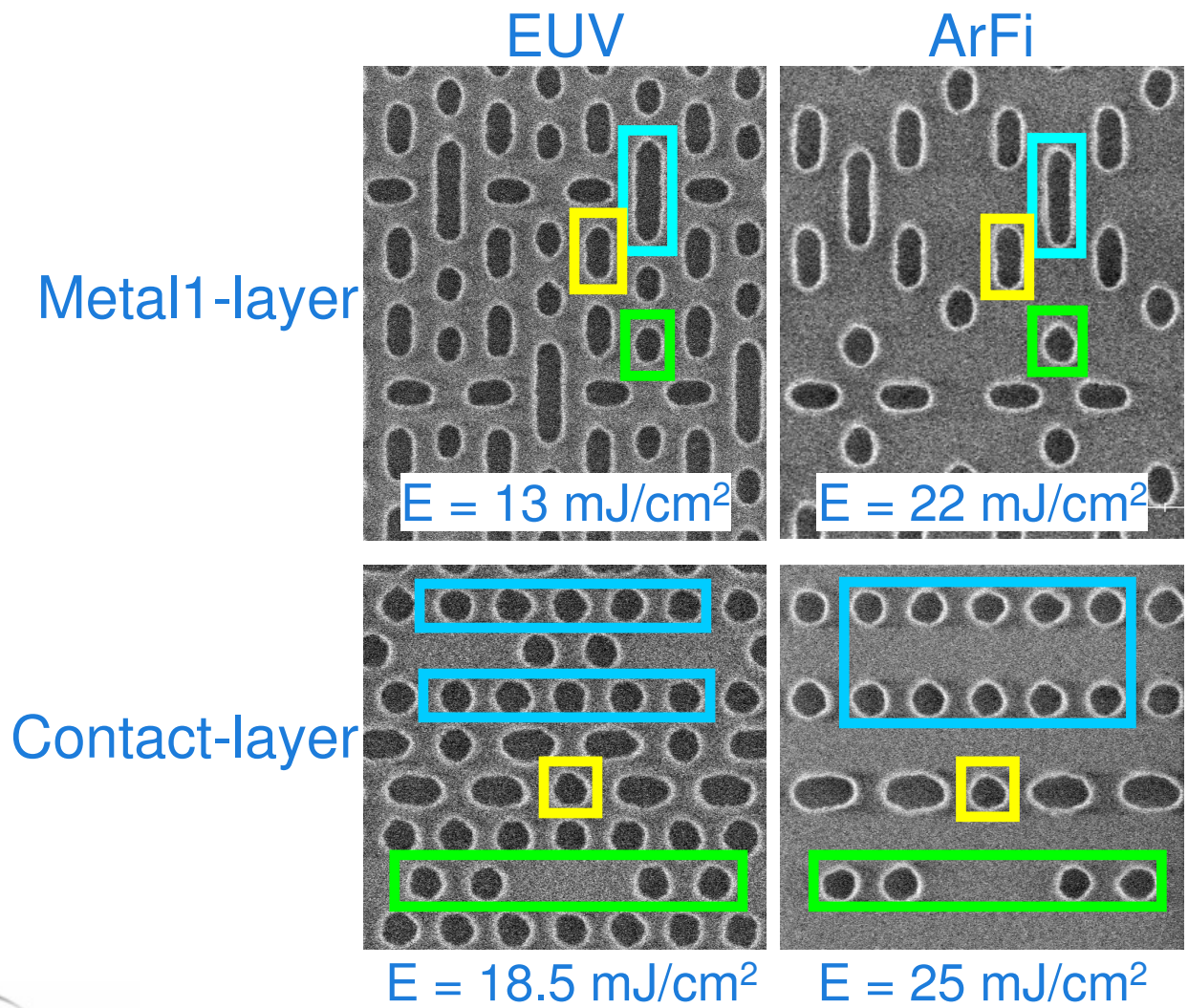
- 6º angle of incidence: CD error on wafer level due to shadow from mask features => HV offset that changes across slit
- Higher flare than ArF i system: Feature correction depending on feature density
- Here: Constant HV bias for shadowing, no flare correction. Regular OPC for CH layer



EUV exposures on bare Si, ArFi exposure on hard mask for etch



Process window analysis illustrates difference between high k1 and low k1 imaging



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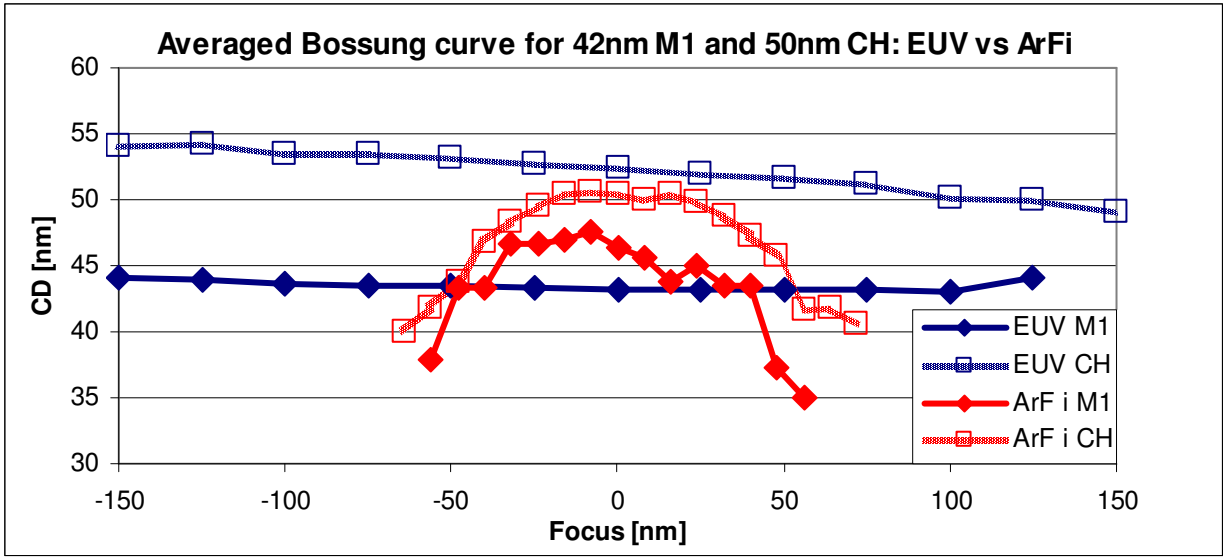
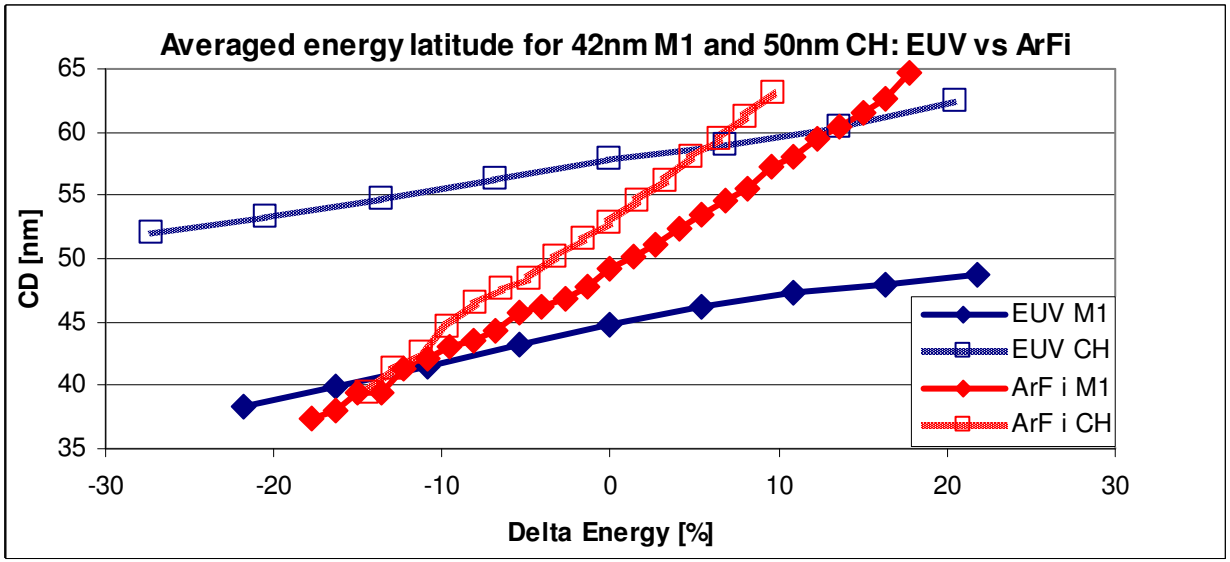


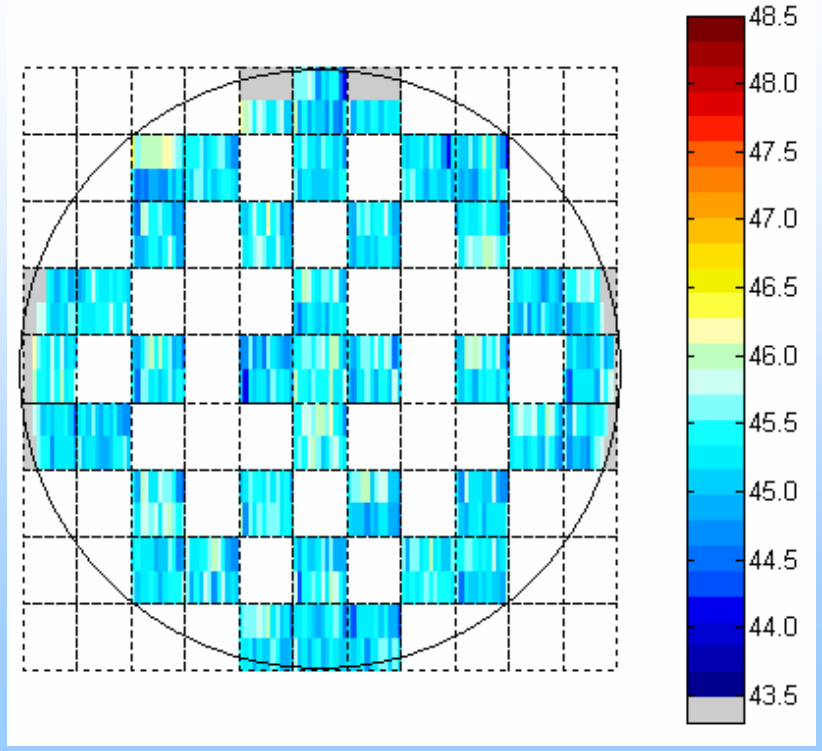
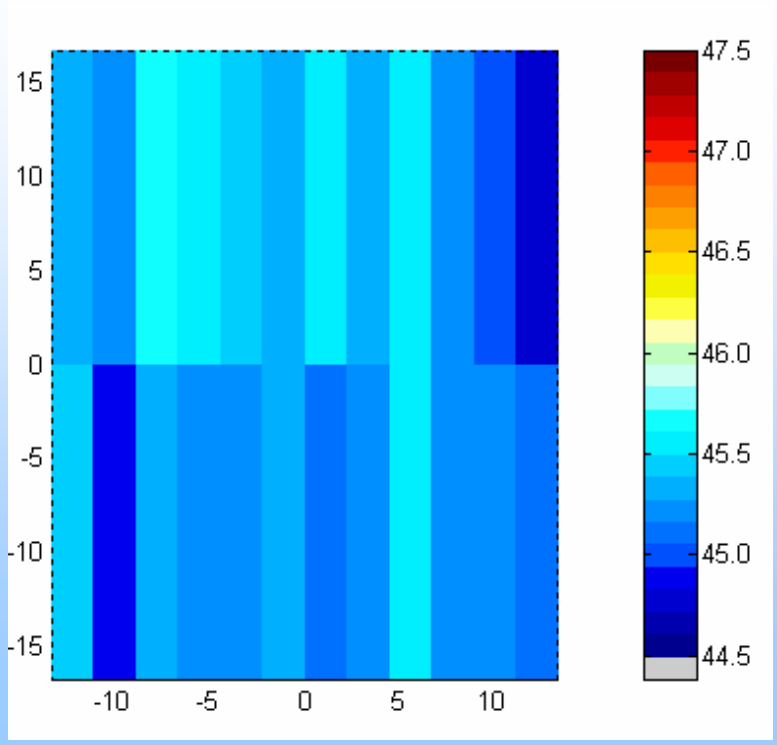
Process window analysis	EUV	ArF i
Depth of Focus – Metal-1 [nm]	>300	~100
Depth of Focus – Contact Hole [nm]	>300	~130

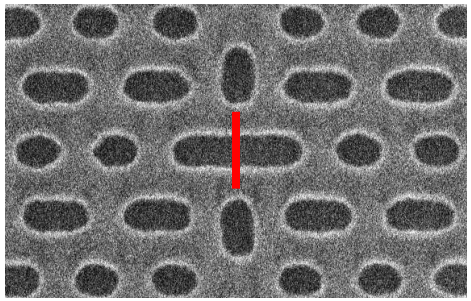
Process window analysis illustrates difference between high k1 and low k1 imaging



Process window analysis	EUV	ArF i
Dose sensitivity – Metal-1 [nm/%]	0.26	0.70
Dose sensitivity – Contact Hole [nm/%]	0.21	0.94
Exposure Latitude – Metal-1 [%]	32	12
Exposure Latitude – Contact Hole [%]	47	10

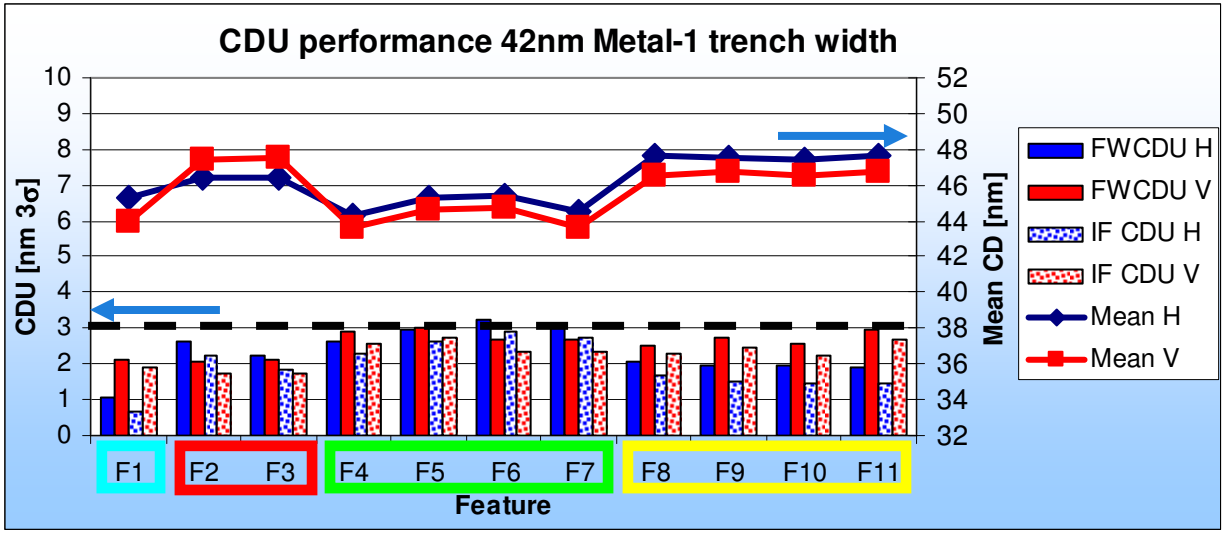
EUV CDU champion data for 42nm trench: 0.7nm 3σ

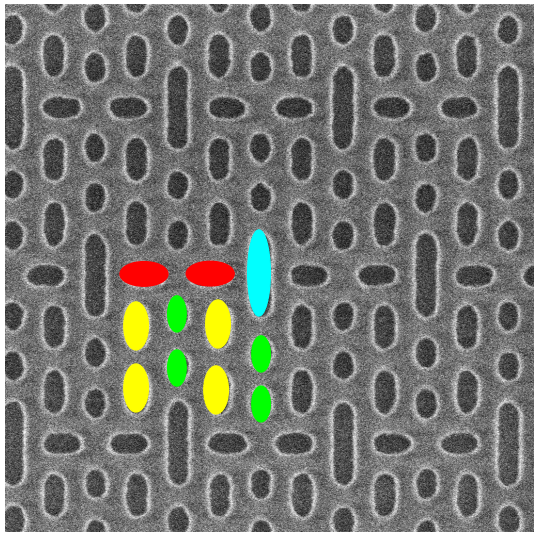
Full wafer CDU = 1.1nm 3σ	Intra Field CDU = 0.7nm 3σ
	



EUV Full wafer CDU 42nm Metal layer < 3.0nm

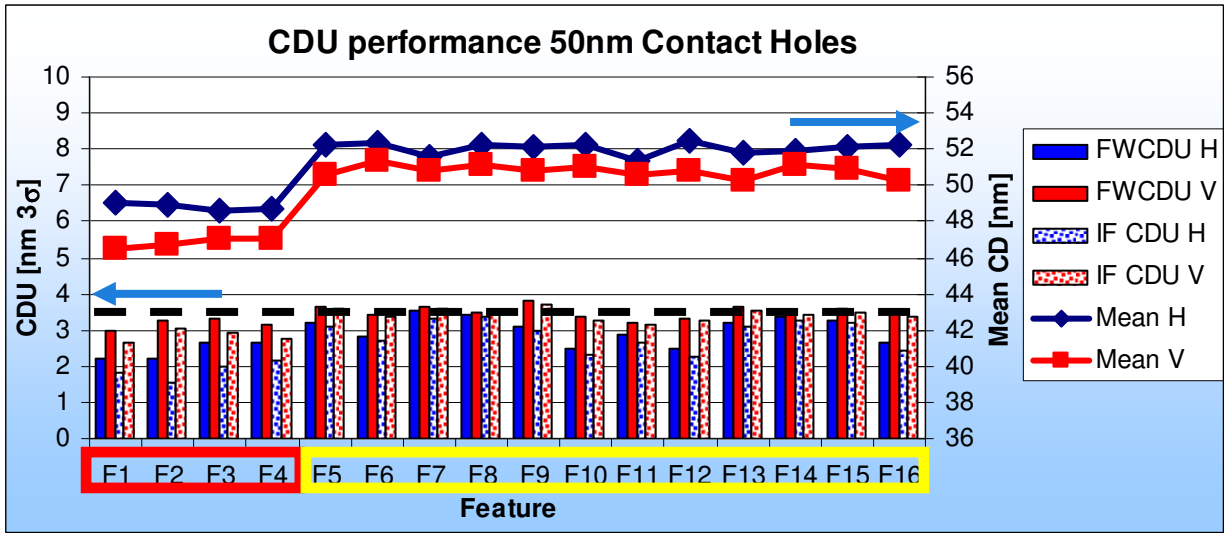
- Full wafer and intra field CDU for 42nm Metal layer:
  - All unique features in designs evaluated
  - Full wafer and intra field CDU < 3.0nm 3σ (7% of TargetCD) for both H and V lay out
  - Identical features in lay-out are within +/-0.6nm from average CD

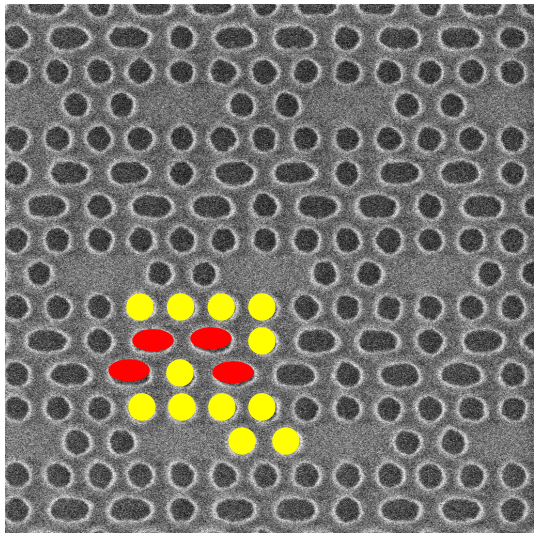




EUV Full wafer CDU 50nm Contact layer < 3.8nm

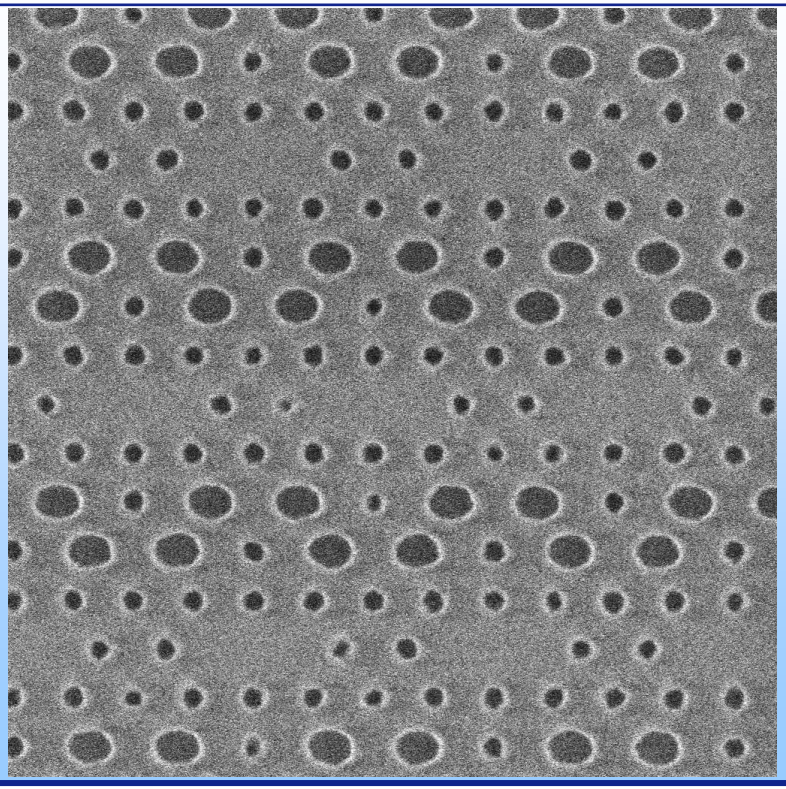
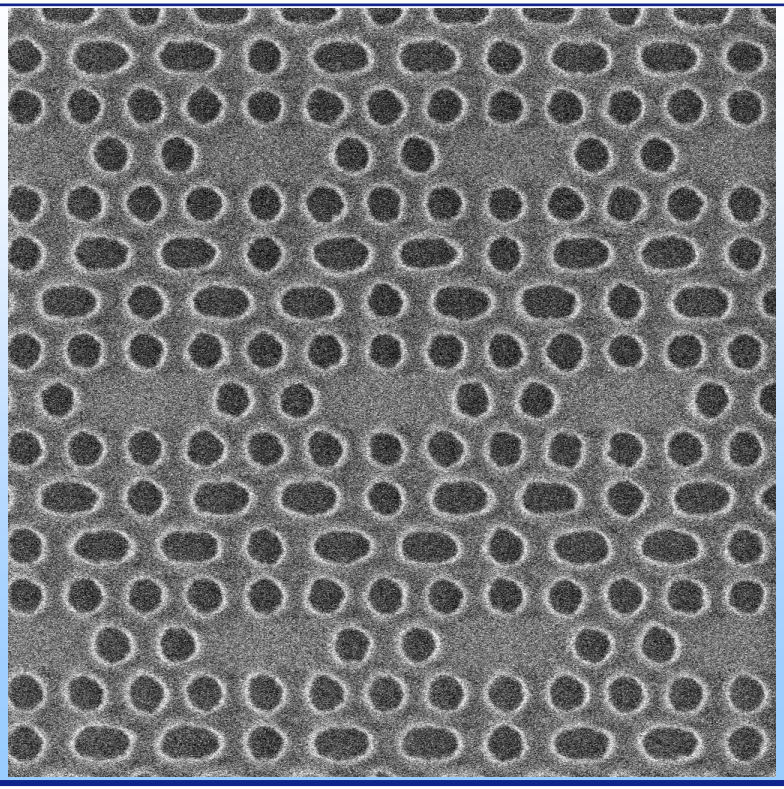
- Full wafer and intra field CDU for 50nm Contact Hole layer
  - All unique features in designs evaluated
  - Full wafer and intra field CDU < 3.8nm 3σ (7.5% of TargetCD) for both H and V lay out
  - Identical features in lay-out are within +/-0.5nm from average CD





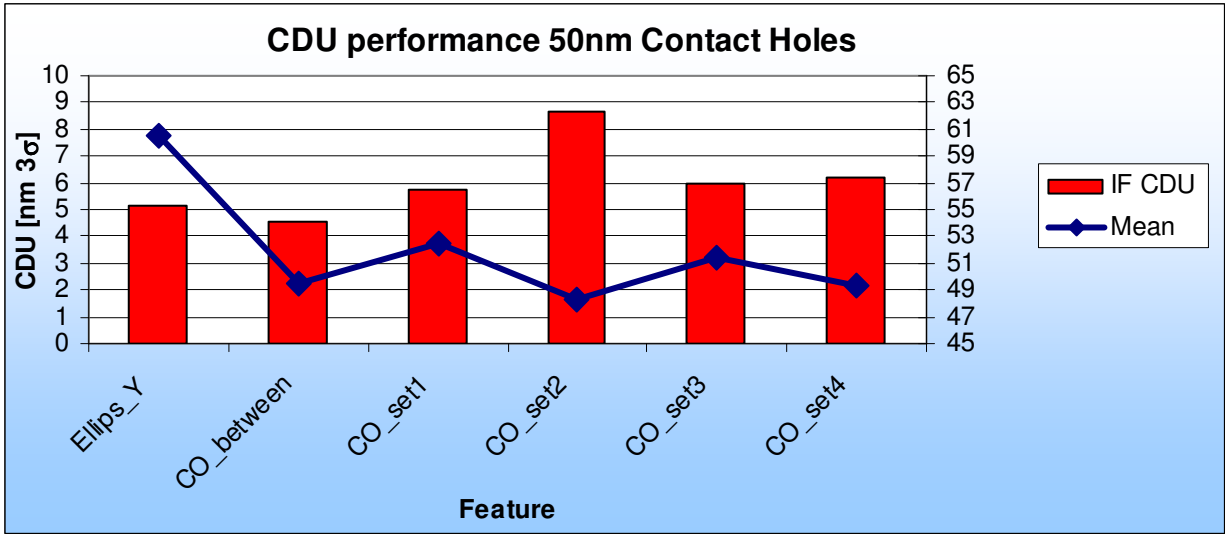
Tachyon OPC applied to Contact layer solved printing problem

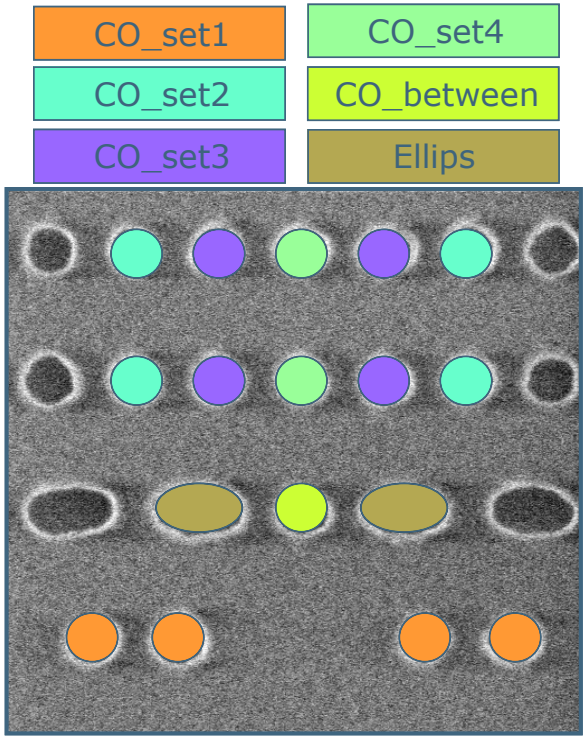
- First round of Tachyon OPC applied to print CHs at the same size as CH slot width

Before OPC	After OPC
	

ArFi Intra field CDU 50nm Contact layer ~ 6.0nm

- 6 features in splitted design evaluated (for symmetry reasons)
- Intra field CDU is between 4.5 and 8.7nm 3σ
- Evaluated contacts print within +/-2nm of average CD





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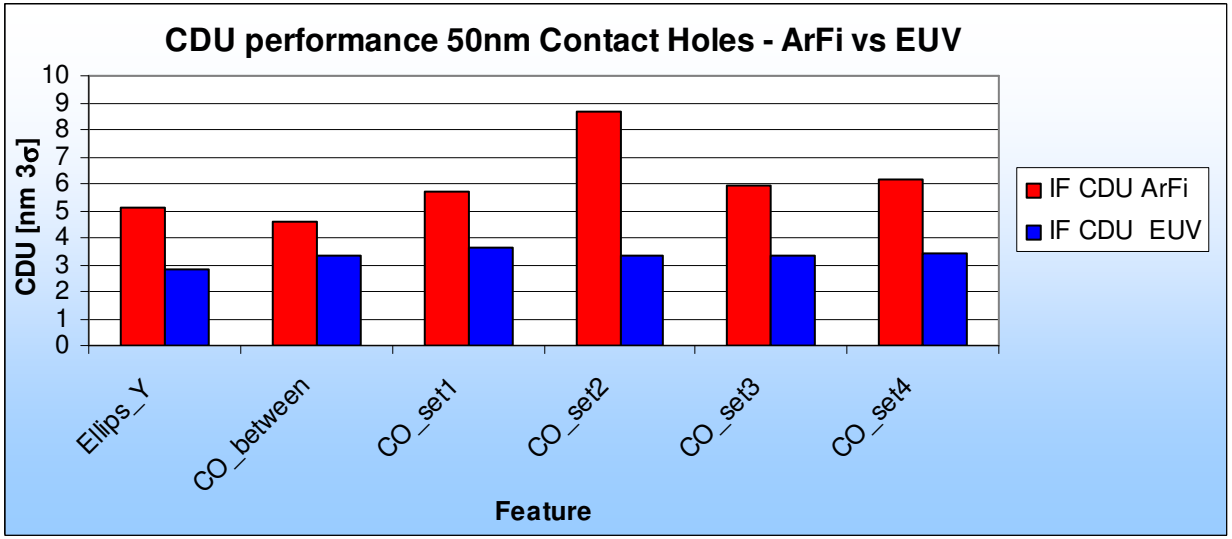
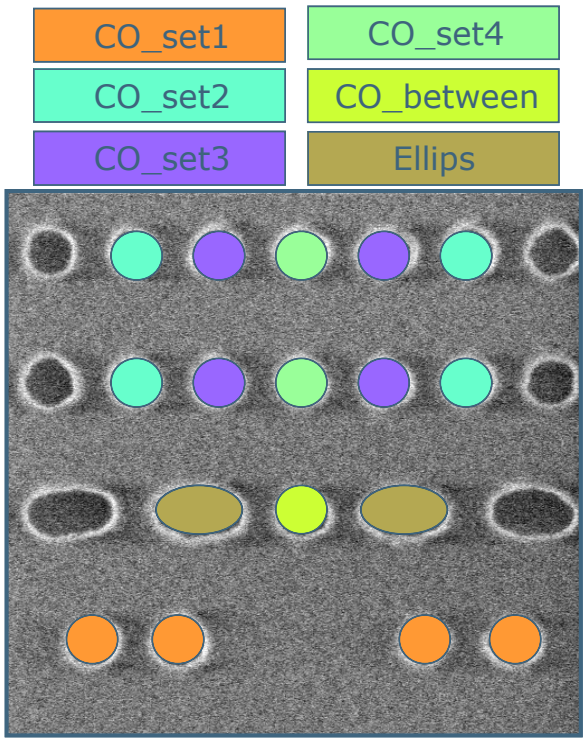
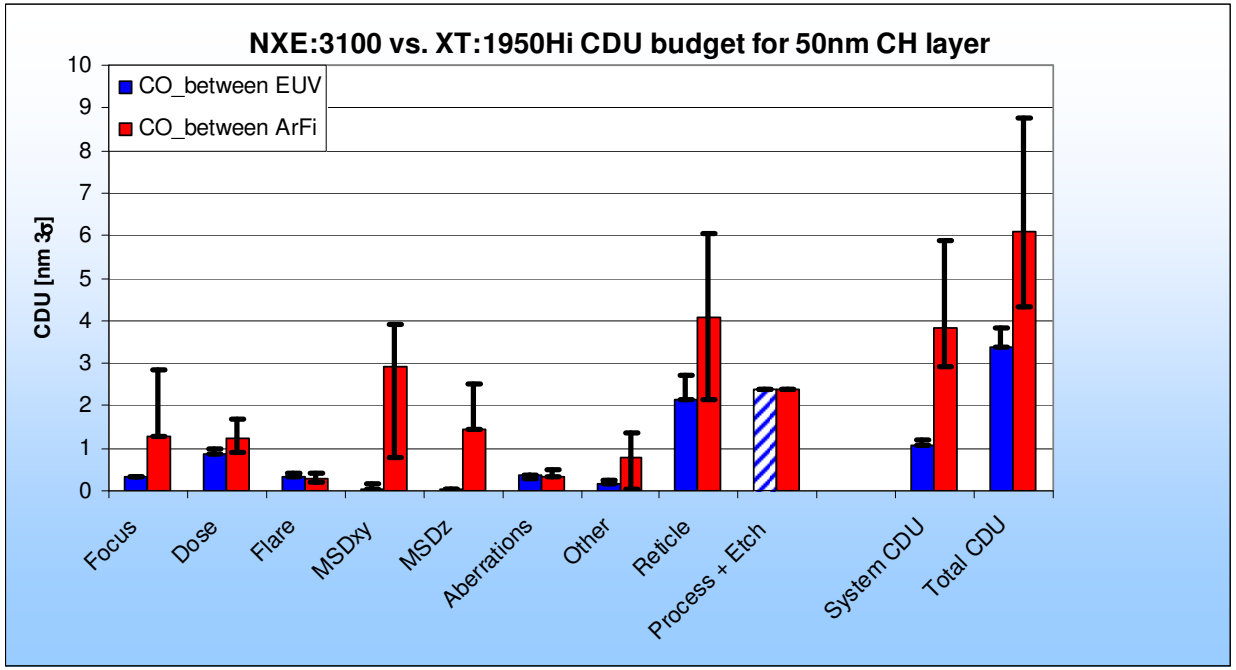
- 6 features in splitted design evaluated (for symmetry reasons)
- Intra field CDU is between 4.5 and 8.7nm 3σ
- Evaluated contacts print within +/-2nm of average CD
- EUV gives better CDU and shows less variation between holes => benefit of high k1 imaging

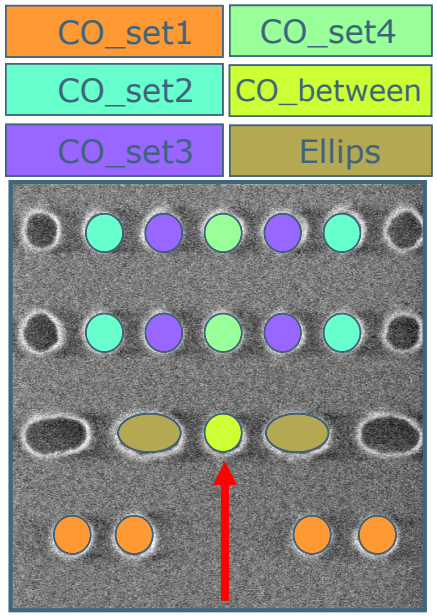




Simulated CDU budget for 50nm Contacts supports experimental data

- Main contributors:
  - EUV: Reticle and process + etch (to be verified), same CDU for all features
  - ArFi: MSDxy and reticle, large CDU differences between features

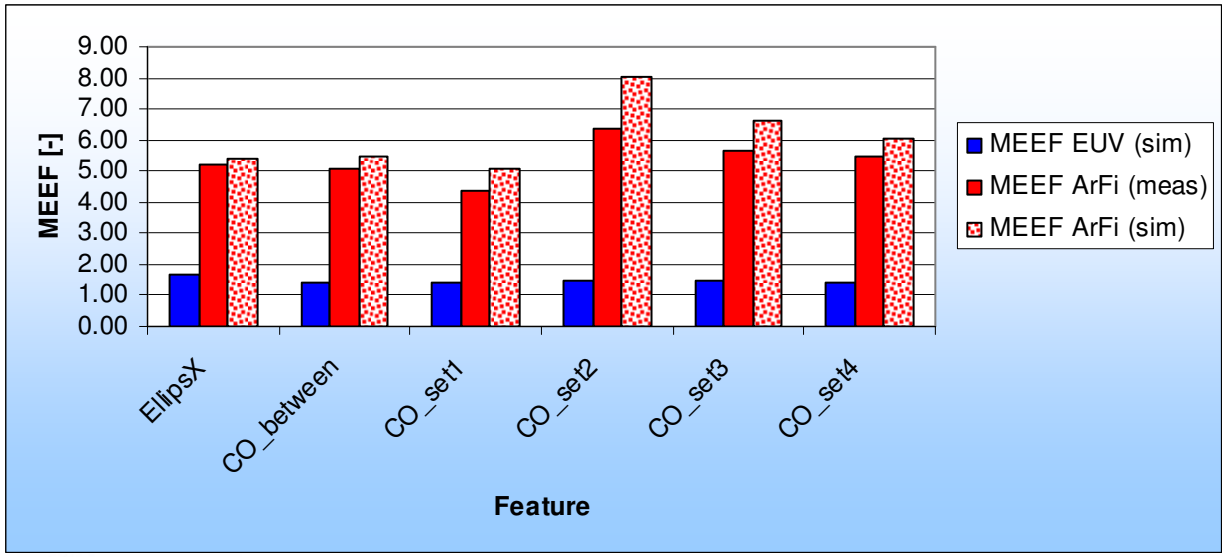


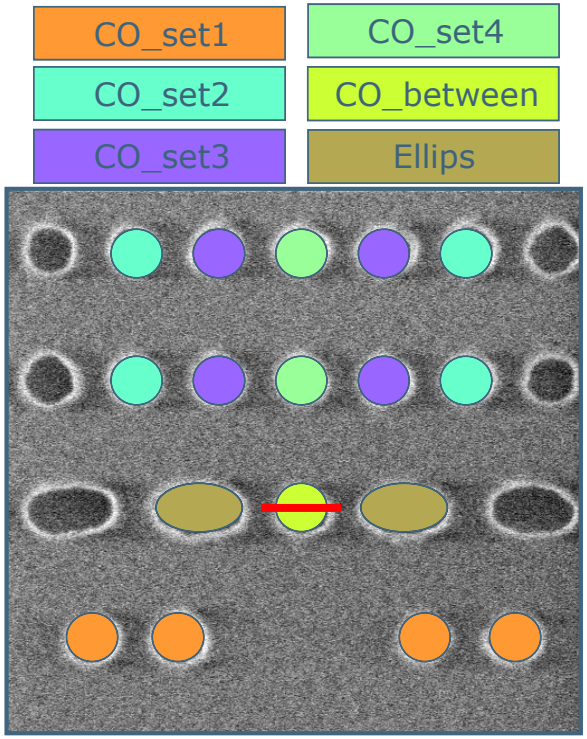


CDU budget analysis	EUV	ArF i
System CDU [nm; 3σ]	~1.0	~3.0-6.0
Total CDU [nm; 3σ]	~3.5	~4.3-8.8

Contact hole MEEF is ~1.5 for EUV and ~5 for ArFi

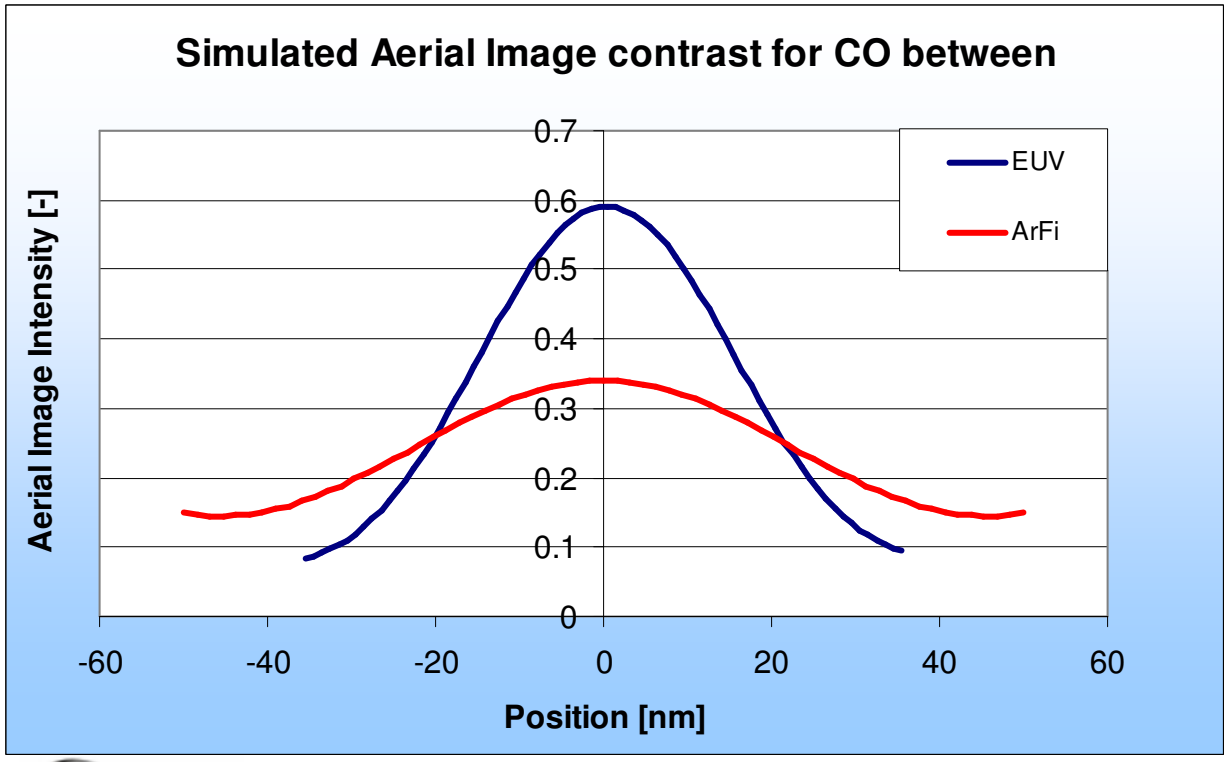
- Mask Error Enhancement Factor (MEEF) is major contributor to ArFi CDU budget
  - EUV MEEF ~ 1.5 (simulated)
  - ArFi MEEF = 4.4 - 6.4 (measured)

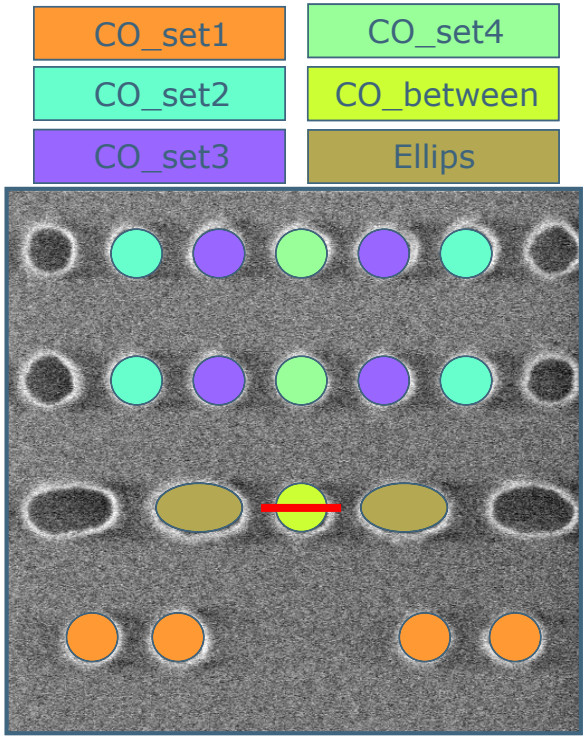




Contact hole MEEF is ~1.5 for EUV and ~5 for ArFi

- Mask Error Enhancement Factor (MEEF) is major contributor to ArFi CDU budget
  - EUV MEEF ~ 1.5 (simulated)
  - ArFi MEEF = 4.4 - 6.4 (measured)
- Aerial image contrast shows:
  - EUV: High contrast and steep slope => low MEEF
  - ArFi: Low contrast and shallow slope => high MEEF + MSDxy sensitivity





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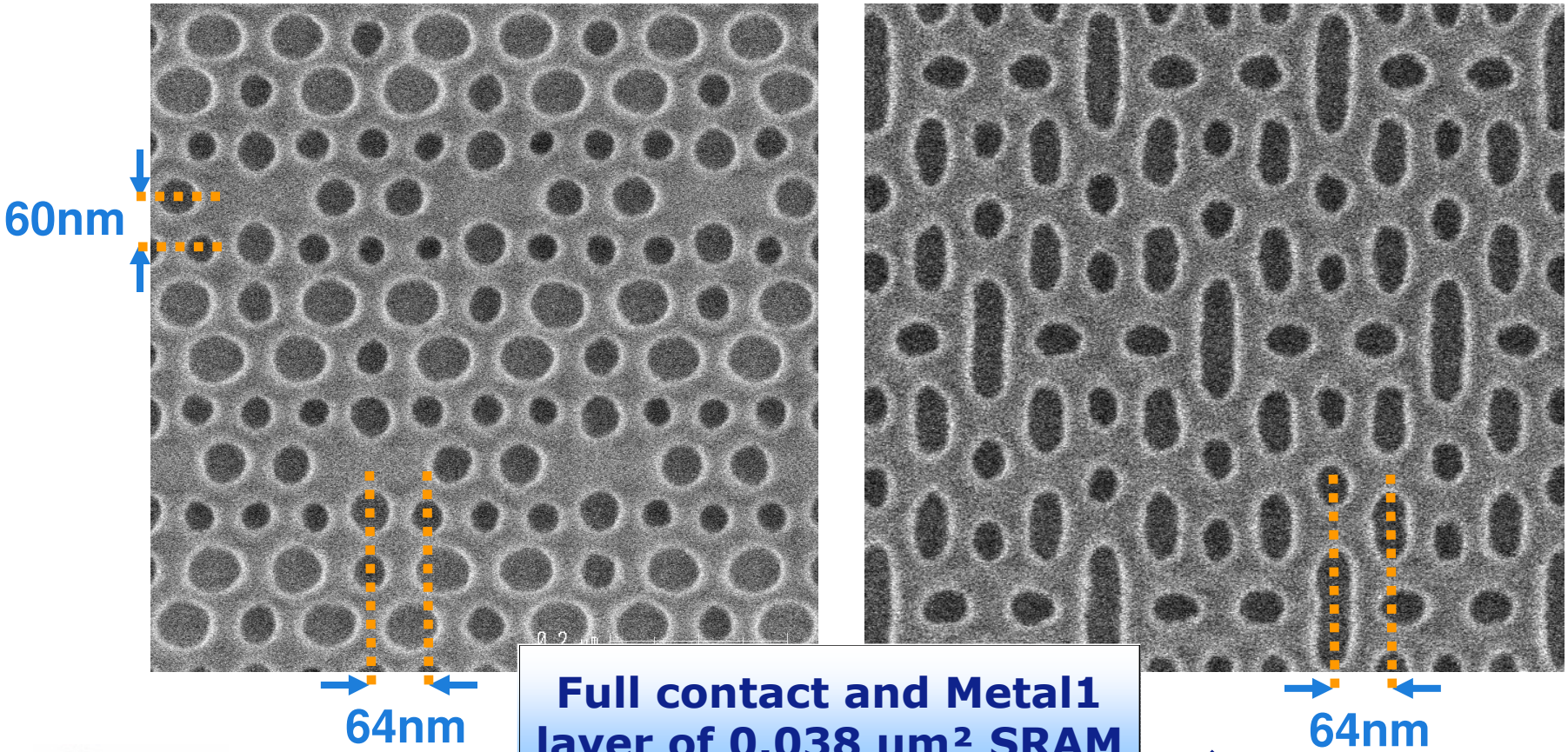
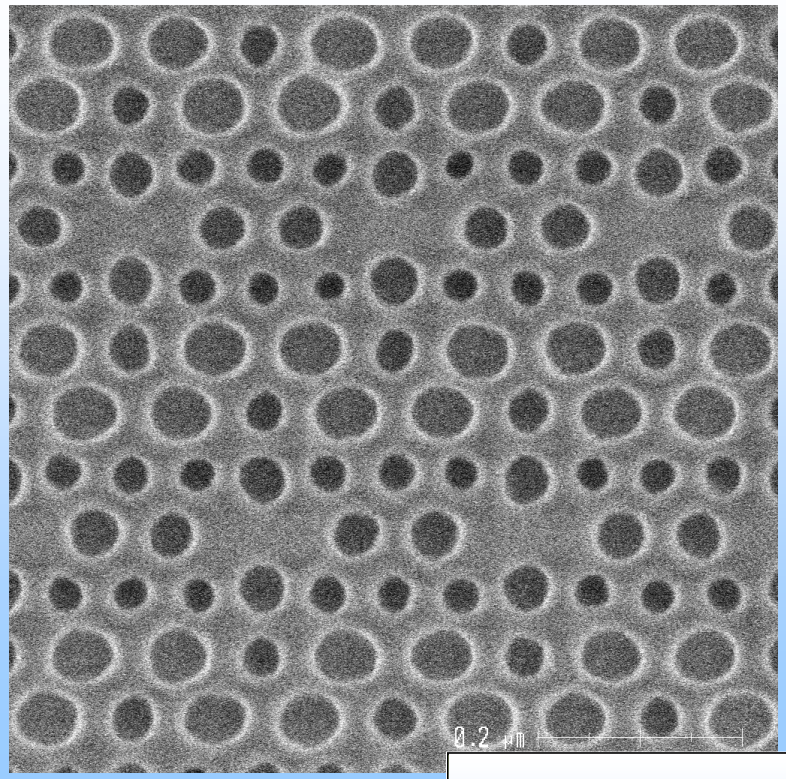
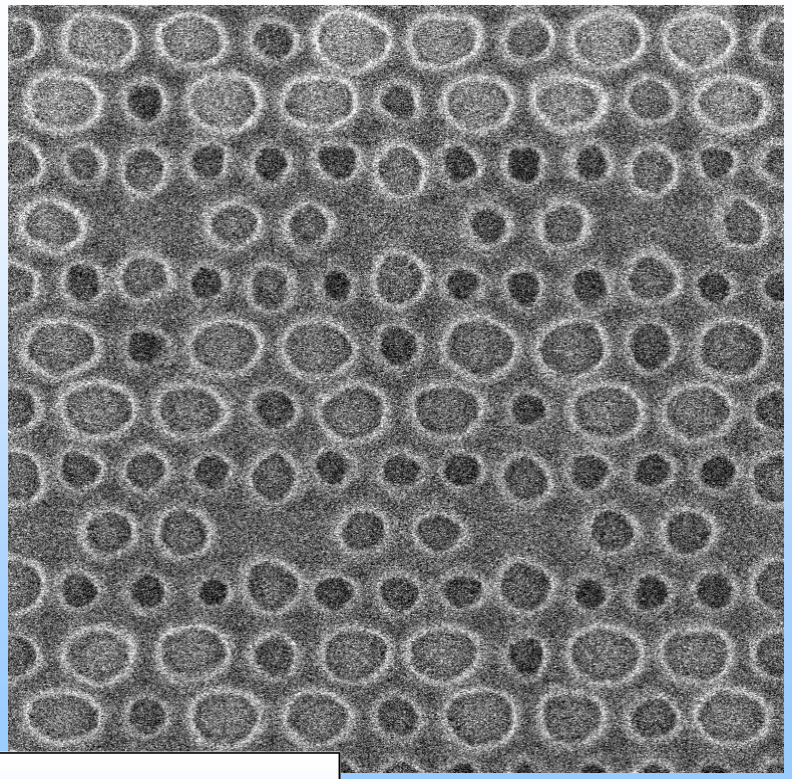
SRAM scaling down to 16nm node using 0.25 NA EUV

- Contact and M1 layer of aggressive 16nm node cell-size (0.038µm^2) resolved at first try
- SEM-images show that OPC needs to be optimized further



Full contact and Metal1 layer of 0.038 µm² SRAM

16nm node SRAM contact layer exposed on the NXE:3100

0.25 NA alpha system	NXE:3100
	

Full contact layer of 0.038 µm² SRAM

OPC and process to be optimized

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- Dark field back-end layers (as demonstrated here) show superior CDU performance with EUV lithography =>
  - Benefit of high k1 imaging
- Main challenges for ArFi double patterning:
  - Imaging at decreasing contrast levels =>
  - Stringent system specs, eg. on MSDxy, focus and overlay, to meet total CDU performance
  - Tight specification on masks due to high MEEF and reduced tolerance for registration errors
- CDU requirements were met on 0.25 NA alpha system for contact and metal layer
- First round OPC solved problems with contact printing

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