EUV resist materials and processing at Selete

Kentaro Matsunaga, Hiroaki Oizumi, Koji Kaneyama,
Gousuke Shiraishi, Kazuyuki Matsumaro, Julius Joseph Santillian and Toshiro Itani

Selete
Semiconductor Leading Edge Technologies, Inc.

2009 International Symposium on Extreme Ultraviolet Lithography October 21, 2009

Outline

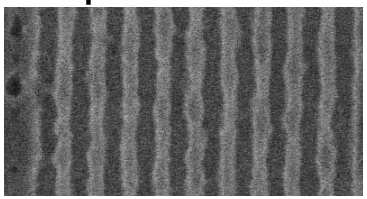
- Requirements for hp 2x-nm and current status

- Resist Materials
  - Lithography performance of 4th and 5th Selete Standard Resist (SSR4 & SSR5)

- Resist Processes
  - Prevention of pattern collapse
  - Reduction of LWR

- Summary

Requirements for hp-2xnm and current status

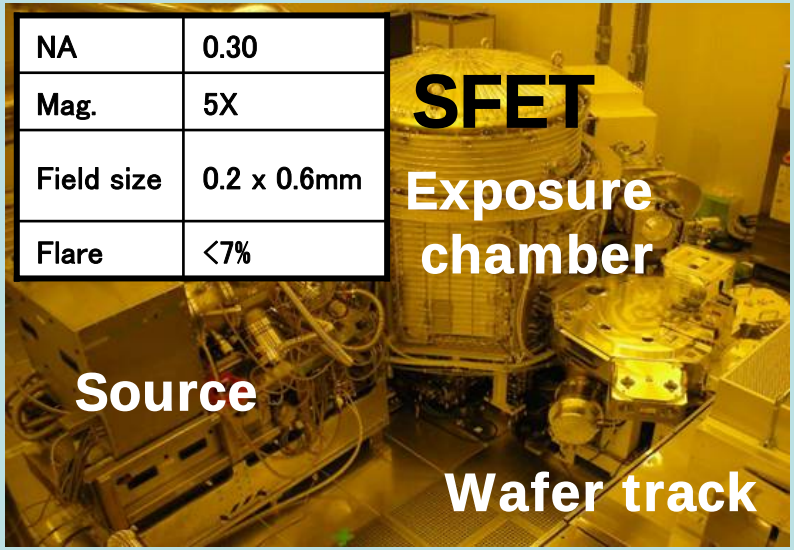
	Target	SSR3(*1)	Our previous report of resist process
Resolution	2x nm	hp 24nm (*2) 	•**Thinner resist thickness (H. Oizumi, SPIE2009)** *Reso. Limit 25nm@Tr60nm→ 24nm@Tr50nm*
Sensitivity	< 10 mJ/cm2	13.8mJ/cm2 @hp26nm	
LWR (Short range)	<2.xnm (1/10 hp)	6.7nm @hp32nm	•**Post development rinse (T.Itani, ICPST2009)** *LWR: 45% improvement @ hp45nm* •**Developer solution (J.J. Santillian, EIPBN2009)** *LWR: 20% improvement @ hp32nm*

(*1)SSR : Selete Standard Resist
(*2)SFET Exposure, Illm: X-Slit

- Improvements of Sensitivity and LWR by resist material are required.
- Process optimization is required.

Development Scheme for EUV Resist and process

Selete

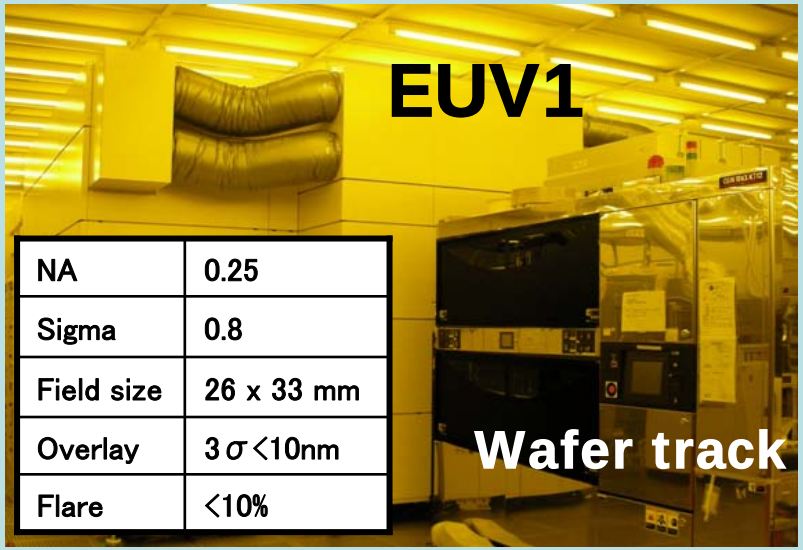


NA	0.30
Mag.	5X
Field size	0.2 x 0.6mm
Flare	<7%

Fundamental test

Improvement of resist materials
Early evaluation of resist process

Improved resist materials and processes



NA	0.25
Sigma	0.8
Field size	26 x 33 mm
Overlay	3σ<10nm
Flare	<10%

Productivity test

Test Chip evaluation
Productivity evaluation

Material

Feedback

Material supplier
- Resist maker
- Resin maker
- Under layer maker
- etc.

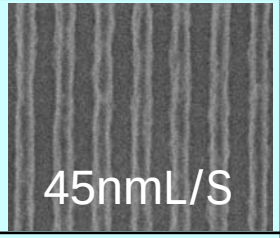
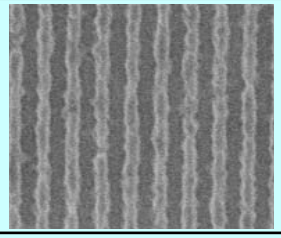
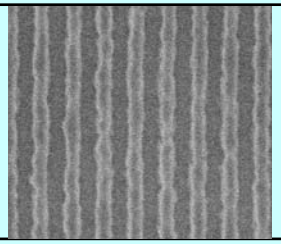
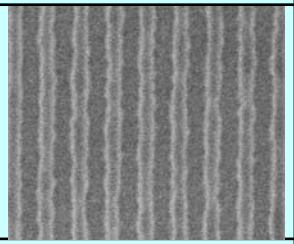
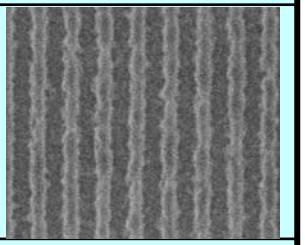
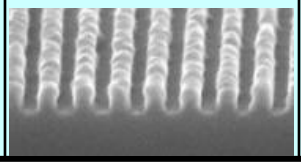
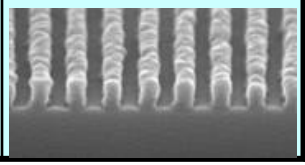
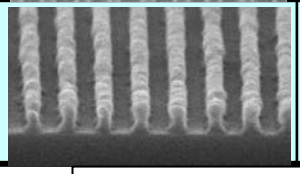
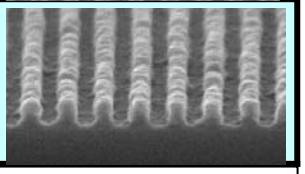
•Polymer based resist
•Low Mw based resist
•New concept resist

Resist materials for hp2x-nm

Selete

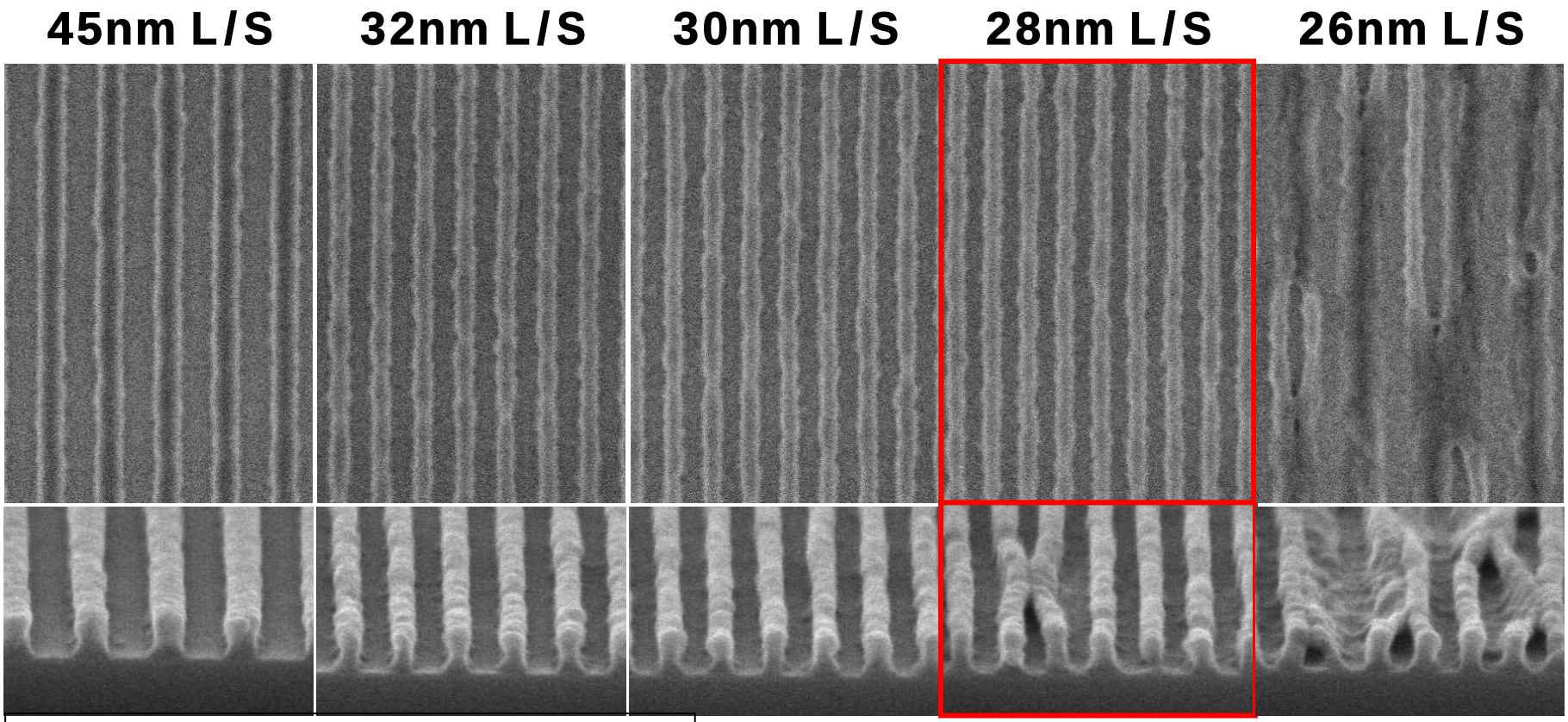
Semiconductor Leading Edge Technologies, Inc.

Newly Selete Standard Resists for hp2x-nm

Resist name	SSR1	SSR2	SSR3	SSR4	SSR5
Dose (mJ/cm^2) @hp32nm	13.4@ 45nmL/S	17.4	13.1	12.4	10.7
Resolution (nm L/S)	40	28	25	28	26
LWR (nm) @hp32nm	7.6 @45nmL/S	10.3	6.7	5.5	7.5
EL(%) @hp32nm	-	12.2	13.4	17.5	16.3
Out-gassing (moles./cm^2/s)	4.9×10^{16}	5.8×10^{16}	3.4×10^{17}	8.0×10^{16}	1.5×10^{17}
Top-down SEM (hp32nm)					
Cross-section SEM(hp32nm)					

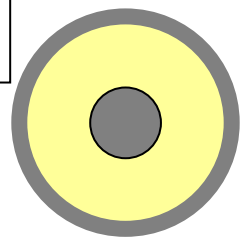
Exp. Tool :SFET
NA0.3, Annular (0.7/0.3)
Resist Thick. 60nm

Imaging performance of SSR4 (Annular)



hp32nm Dose: 12.4mJ/cm^2
LWR: 5.5nm
Exposure Latitude: 17.5%

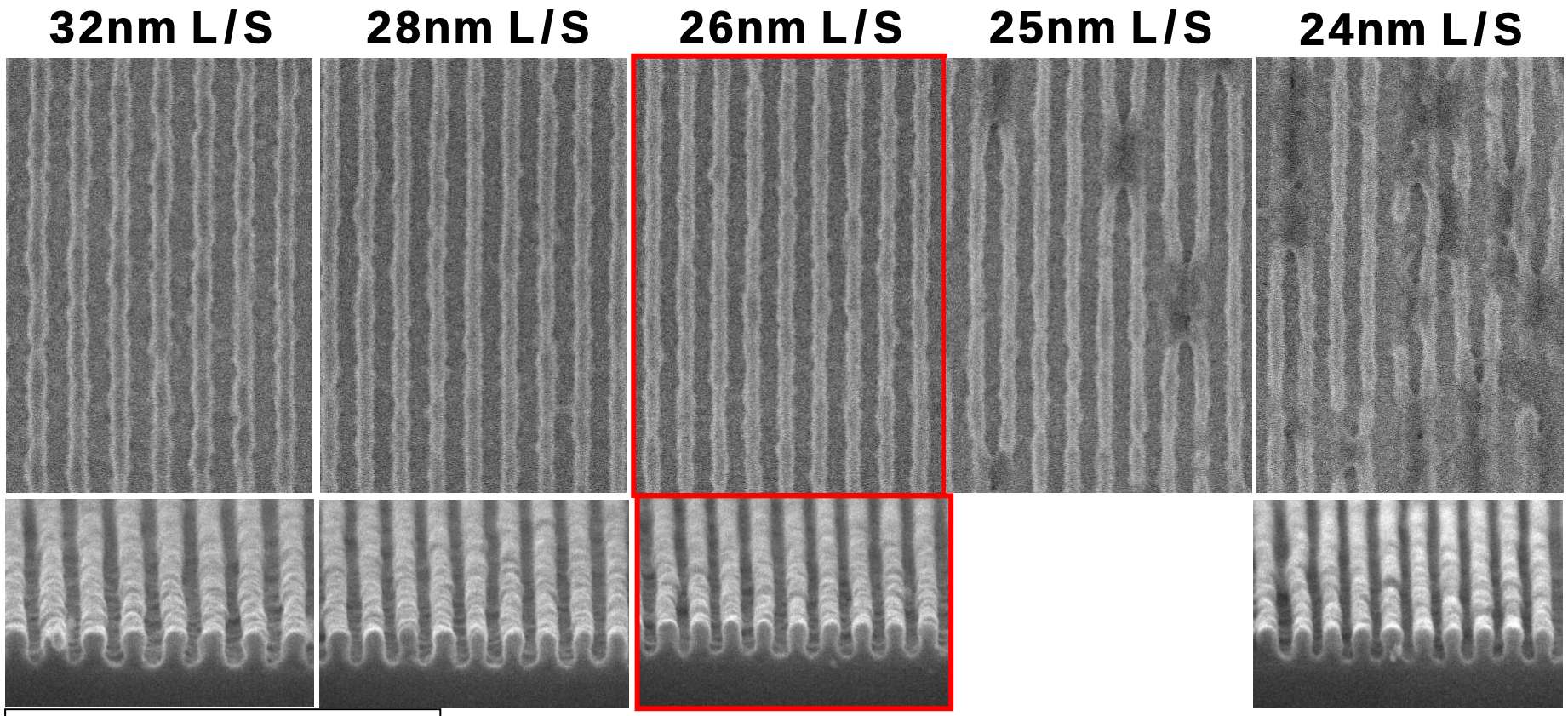
SFET NA0.3
Thick. : 60nm



Annular
(0.7/0.3)

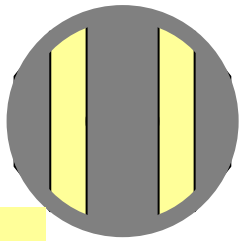
- LWR was improved.
- Sensitivity was improved with resist performance.
- Resolution was limited to hp28nm by pattern collapse.

Imaging performance of SSR4 (X-Slit)



hp28nm LWR: 5.8nm

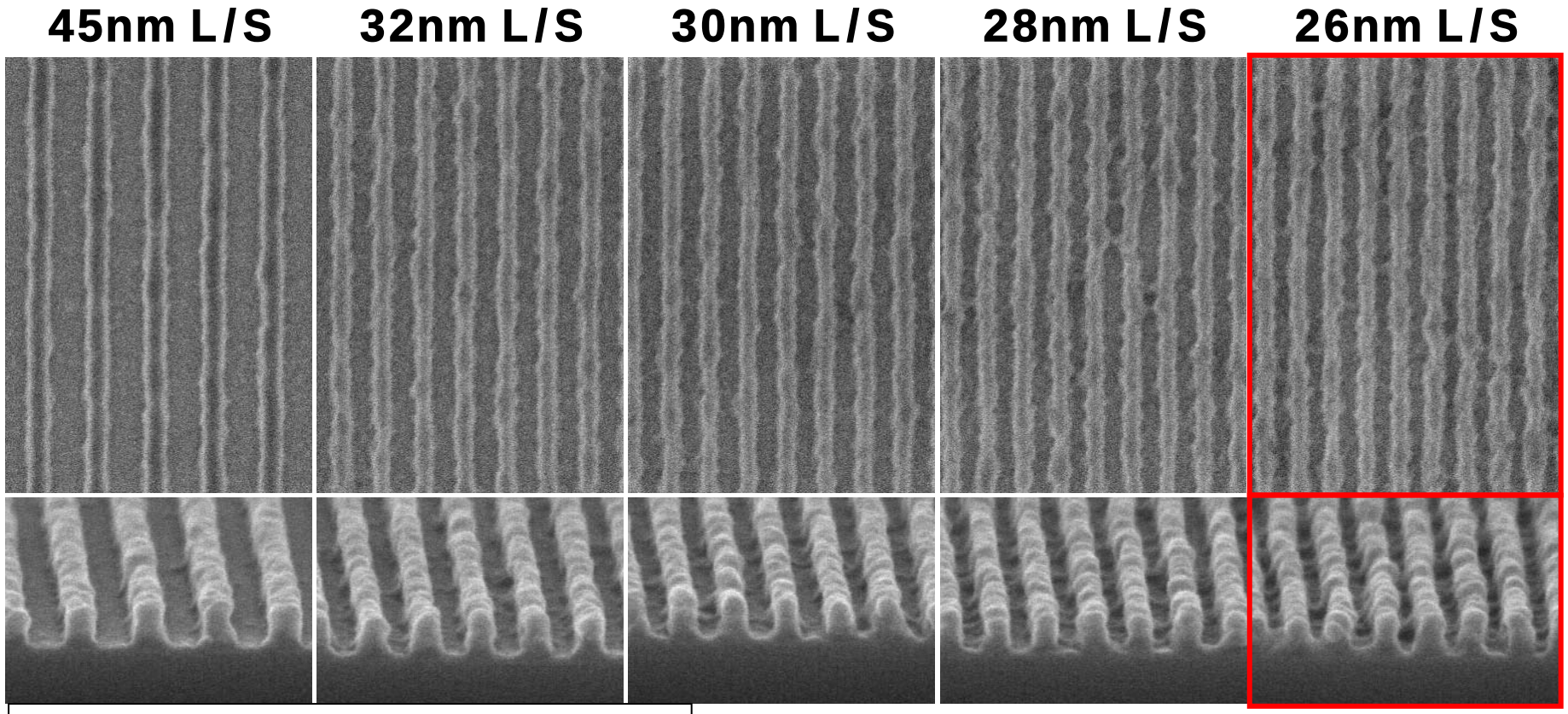
SFET NA0.3
Thick. : 50nm



X-slit

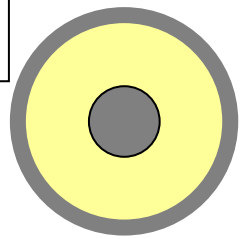
- Resolution was limited to hp26nm with 50nm thickness by pattern collapse.
- Prevention of pattern collapse is necessary.

Imaging performance of SSR5 (Annular)



hp32nm Dose: 10.7mJ/cm^2
LWR: 7.5nm
Exposure Latitude: 16.3%

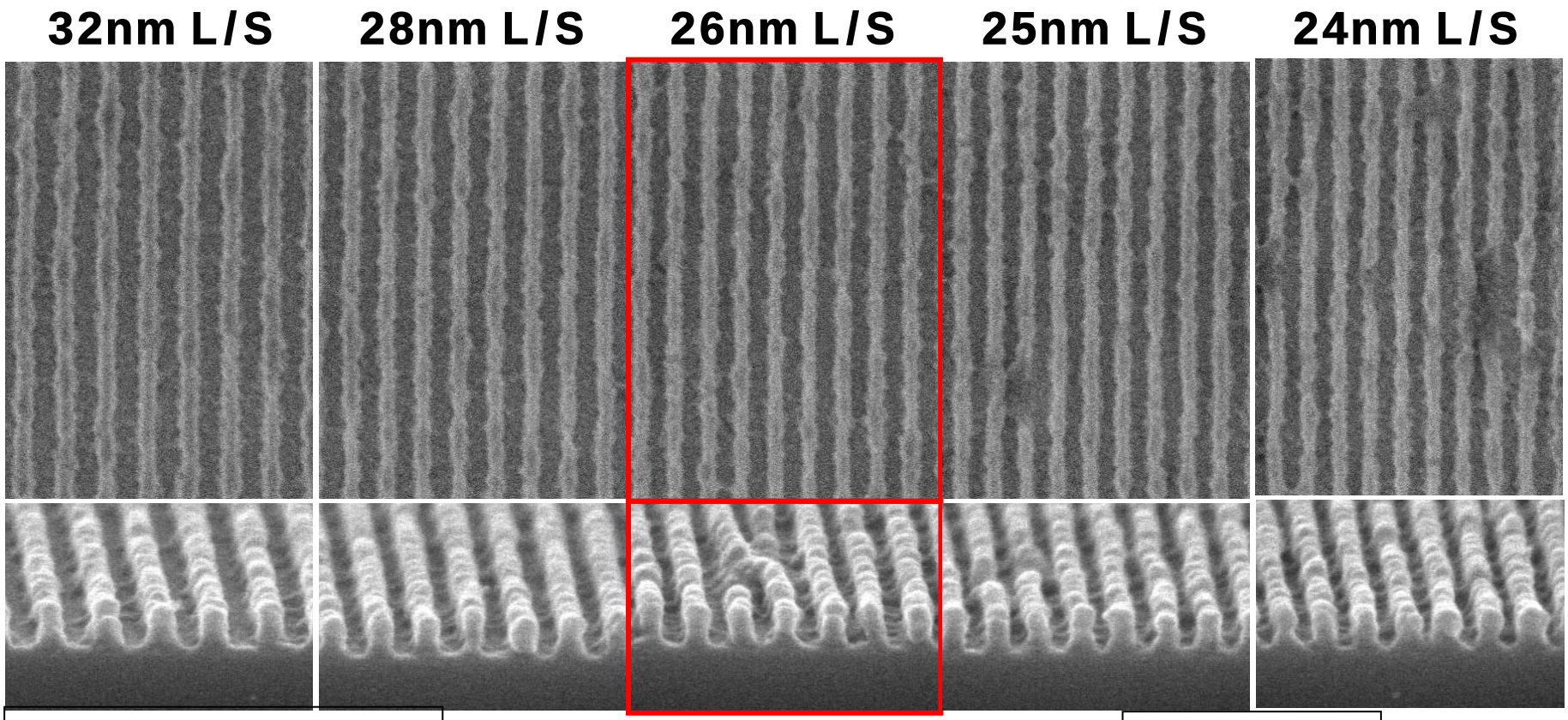
SFET NA0.3
Thick. : 60nm



Annular
(0.7/0.3)

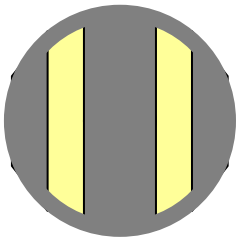
- Resolution achieved hp26nm without pattern collapse
- Sensitivity almost achieved the target.
- LWR was not improved.

Imaging performance of SSR5 (X-slit)



hp28nm LWR: 7.9nm

SFET NA0.3
Thick. : 60nm



X-slit

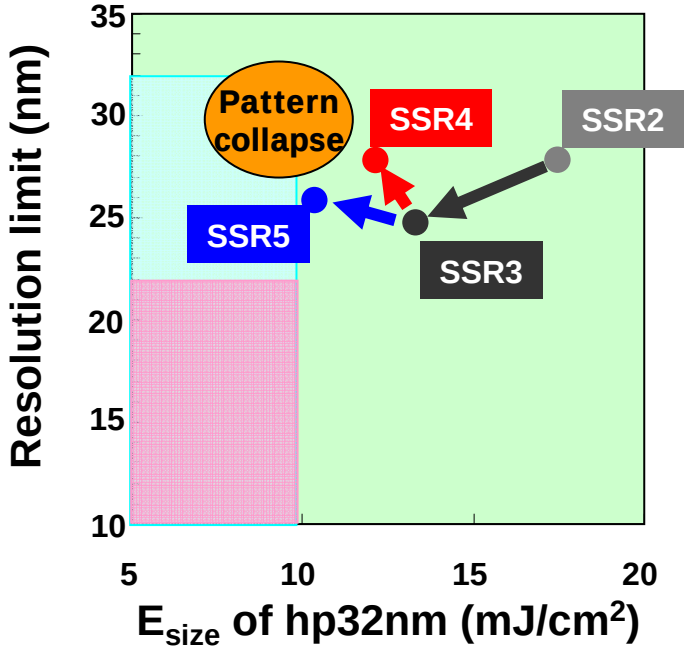
- Resolution was limited to hp26nm by pattern collapse
- Many scum was observed at the bottom.
- Improvements of scum & LWR are required.

Sensitivity vs Resolution & Sensitivity vs LWR

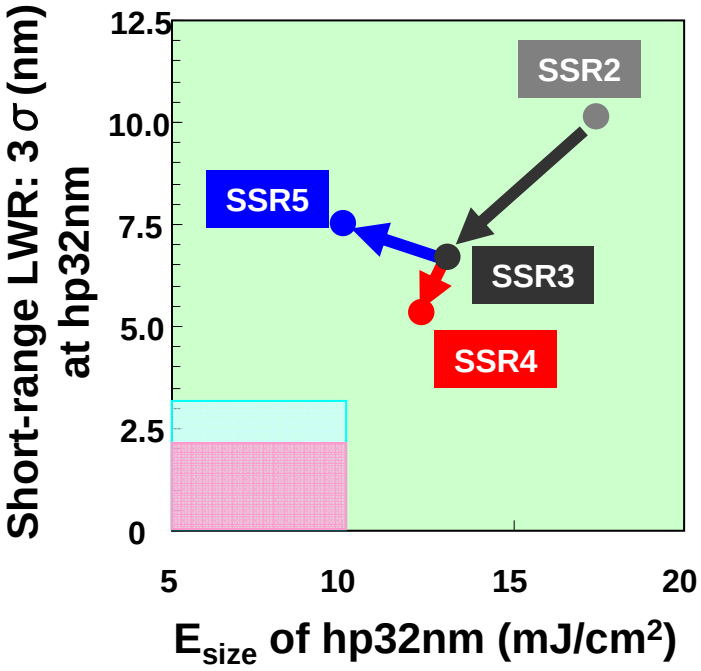
32nm

22nm

Targets: Sensitivity (E_{size}) : 10mJ/cm^2
Short-range LWR : hp x 10%

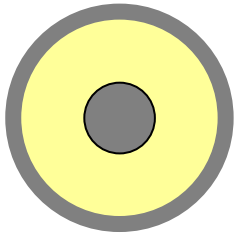


Sensitivity – Resolution



Sensitivity - LWR

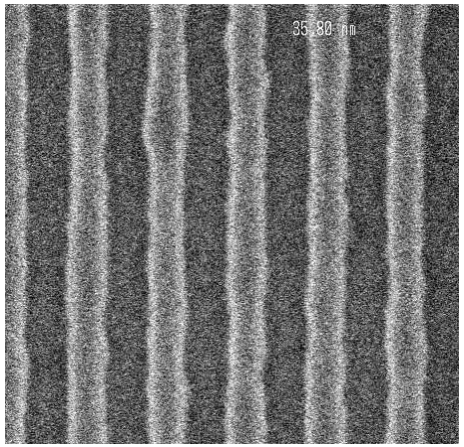
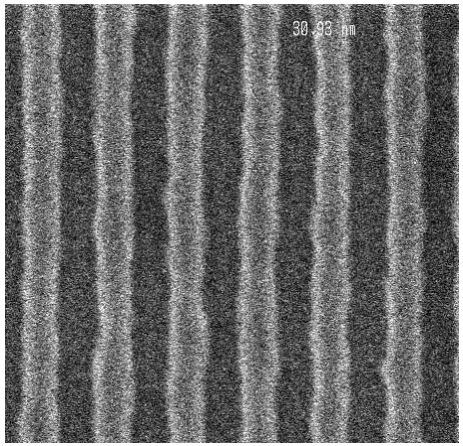
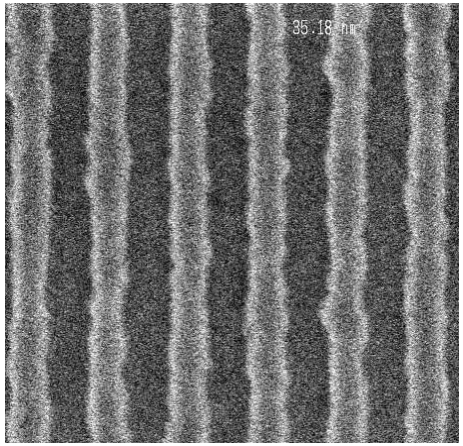
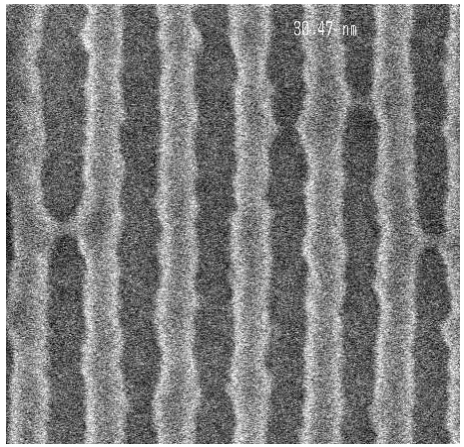
SFET NA0.3
Thick: 60nm



Annular
(0.7/0.3)

- Sensitivity of SSR5 almost achieved the target
- LWR of SSR4 was improved. But it is still far from target.
- Prevention of pattern collapse is necessary to improve resolution limit.

Pattern Profiles of SSR4 and SSR5 using EUV1 Exposure

	35nm L/S	32nm L/S
SSR4		
LWR (nm)	5.3	5.7
SSR5		
LWR (nm)	7.8	8.3

EUV1 NA0.25
Conv. Illm. σ 0.8
Thick. : 60nm
Substrate: Hardmask

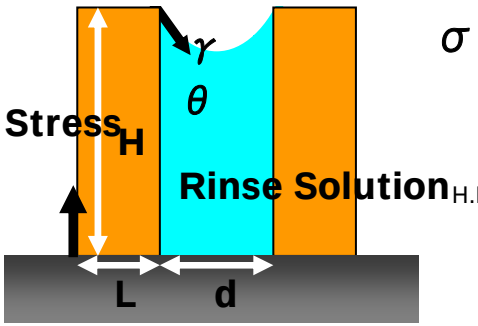
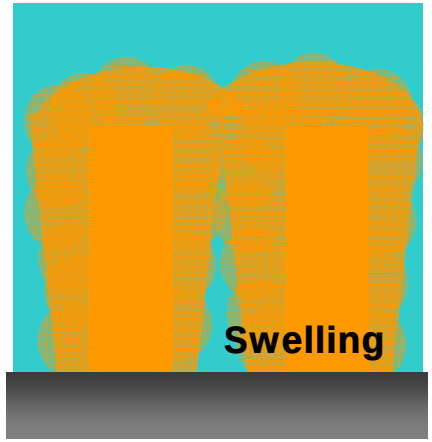
SSR4: Low LWR
SSR5: Micro bridge was induced by Line edge roughness?

Resist Process for hp2x-nm

Selete

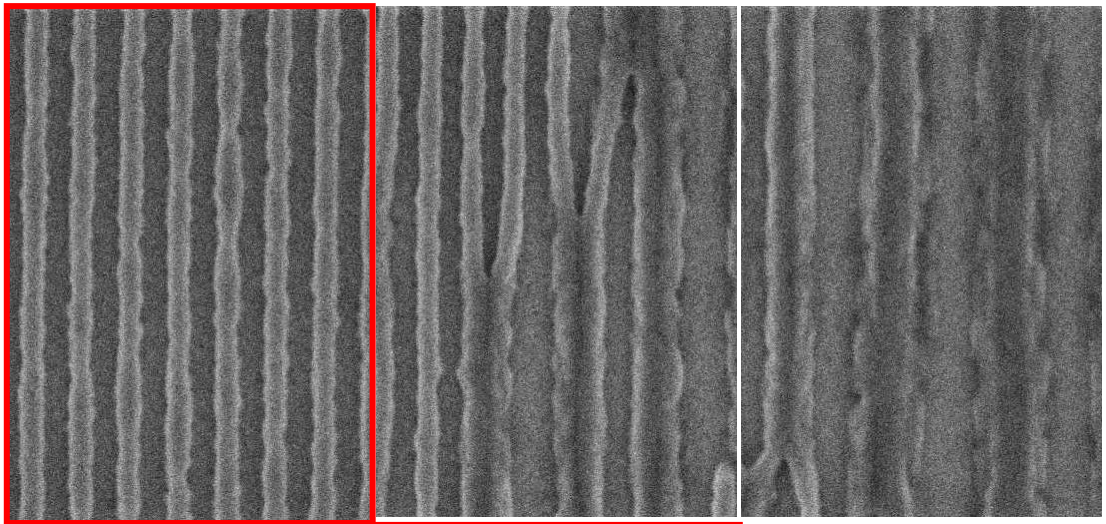
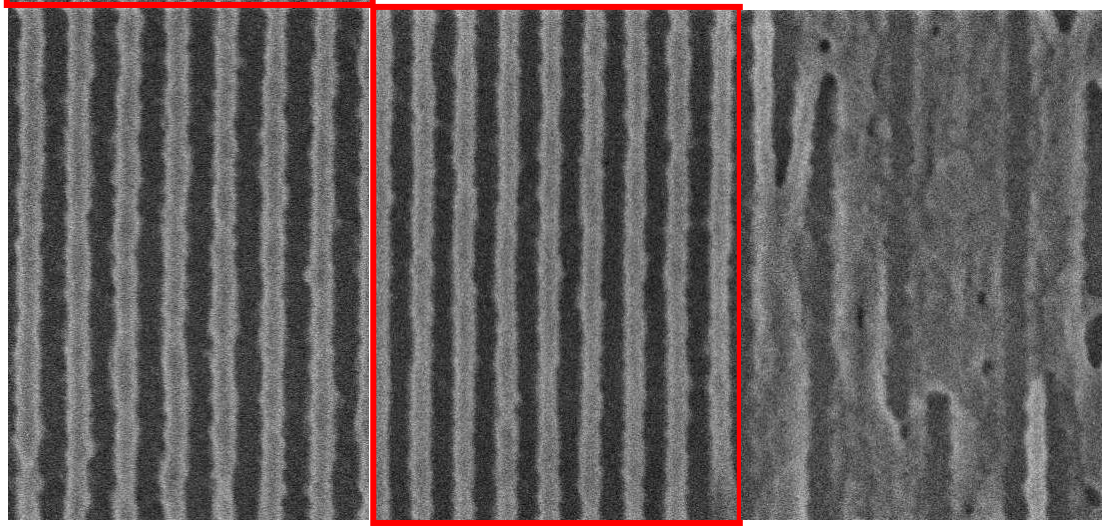
Semiconductor Leading Edge Technologies, Inc.

Improvement of Pattern Collapse by process

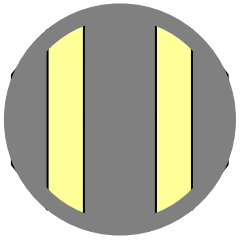
	Rinse process	Development process
Model	**Tensile Stress**  $\sigma = \frac{6\gamma\cos\theta}{d}\left(\frac{H}{L}\right)^2$ γ :Surface tension of rinse solution H.Namatsu, Appl. Phys. Lett. 66 (20), 1995	
	•High aspect ratio of resist pattern •Poor adhesion with substrate •High surface tension of rinse solution	•Swelling
Improvement by process	**•Additional under layer on substrate** **•Apply for rinse solution with low surface tension** **•Thinner resist thickness**	**•Bulky developer material** •Developer with surfactant •Developer concentration

Pattern Collapse evaluation using Under-layer

Selete

	32nm L/S	28nm L/S	26nm L/S
On Hard mask			
On Under-layer			

SFET NA0.3
Resist : SSR4
Thick. : 60nm
Developer :TMAH



X-slit

Pattern collapse was improved on under-layer

Pattern Collapse evaluation using Rinse solution

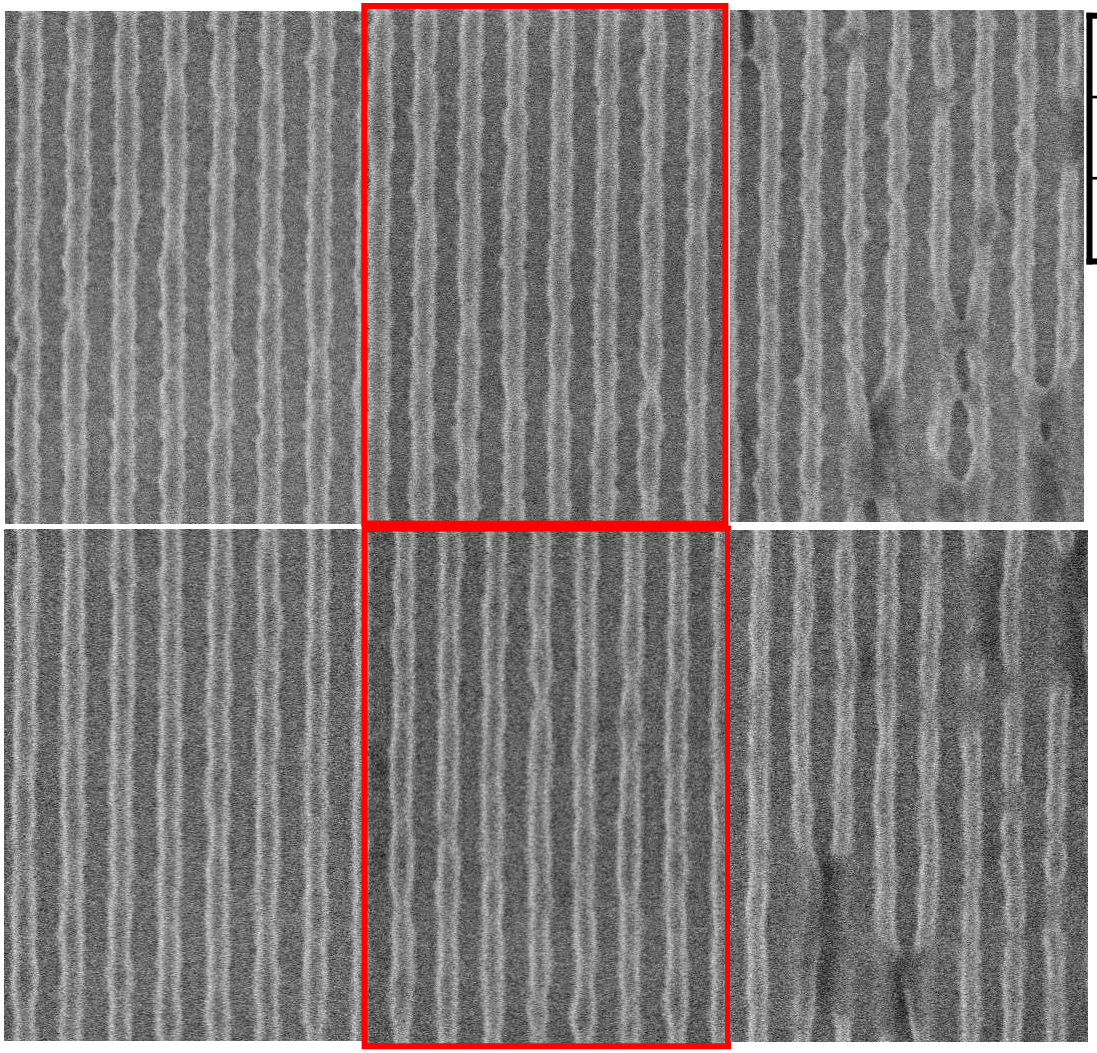
Selete

32nm L/S **30nm L/S** **28nm L/S**

Rinse

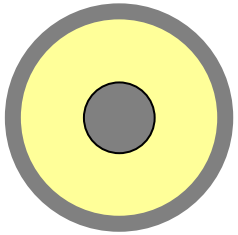
DIW

Rinse solution with low surface tension



L/S	32nm	30nm	28nm
DIW	6.2nm	7.0nm	7.8nm
Rinse Solution	5.1nm	6.1nm	7.0nm

SFET NA0.3
Resist : SSR4
Thick: 60nm
Developer: TMAH

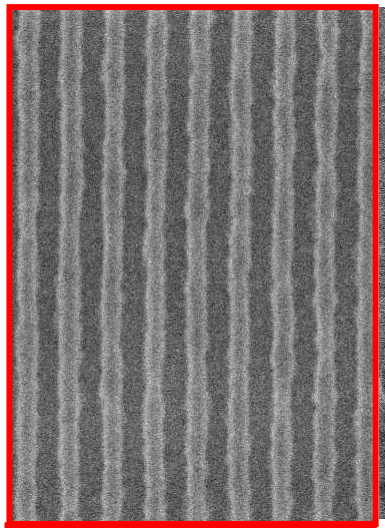
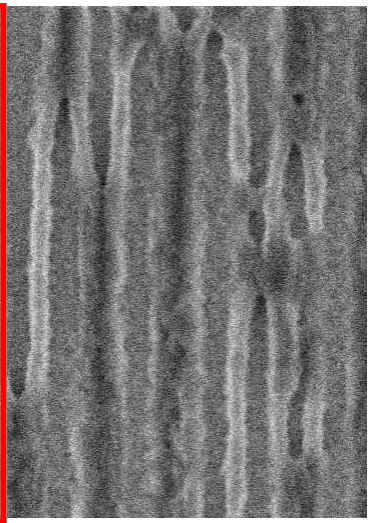
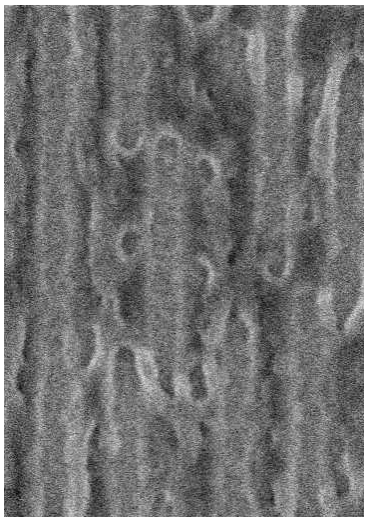
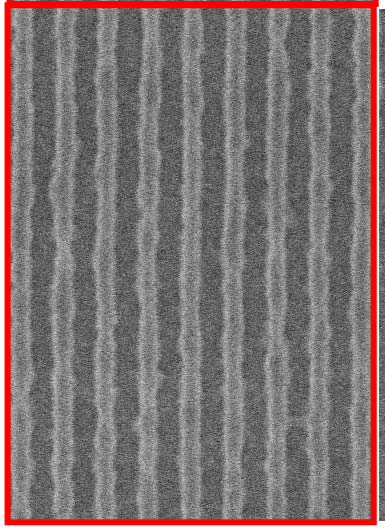
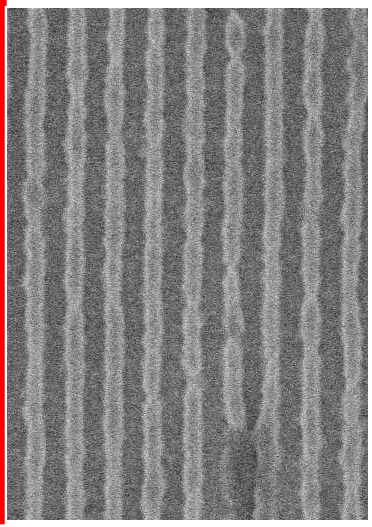
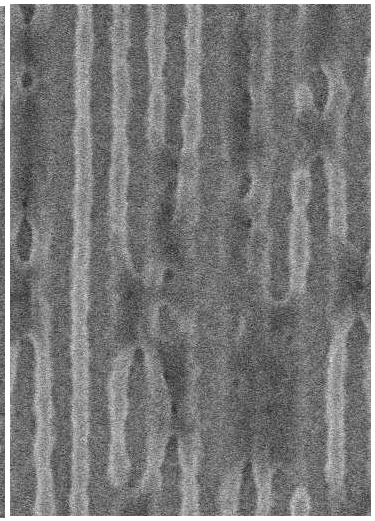


Annular
(0.7/0.3)

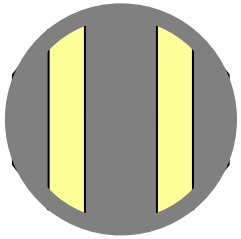
Pattern collapse was not improved by rinse solution

Pattern Collapse evaluation with thinner thickness

Selete

Resist Thickness	28nm L/S	26nm L/S	24nm L/S
60nm			
50nm			

SFET NA0.3
Resist : SSR4
Developer: TMAH



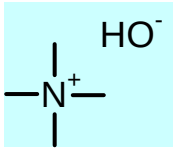
X-slit

Resolution was limited to hp28nm by pattern collapse with 50nm thick.

Pattern Collapse Improvement by New Developer

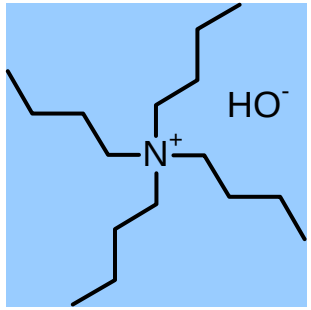
Selete

26nm L/S **25nm L/S** **24nm L/S**

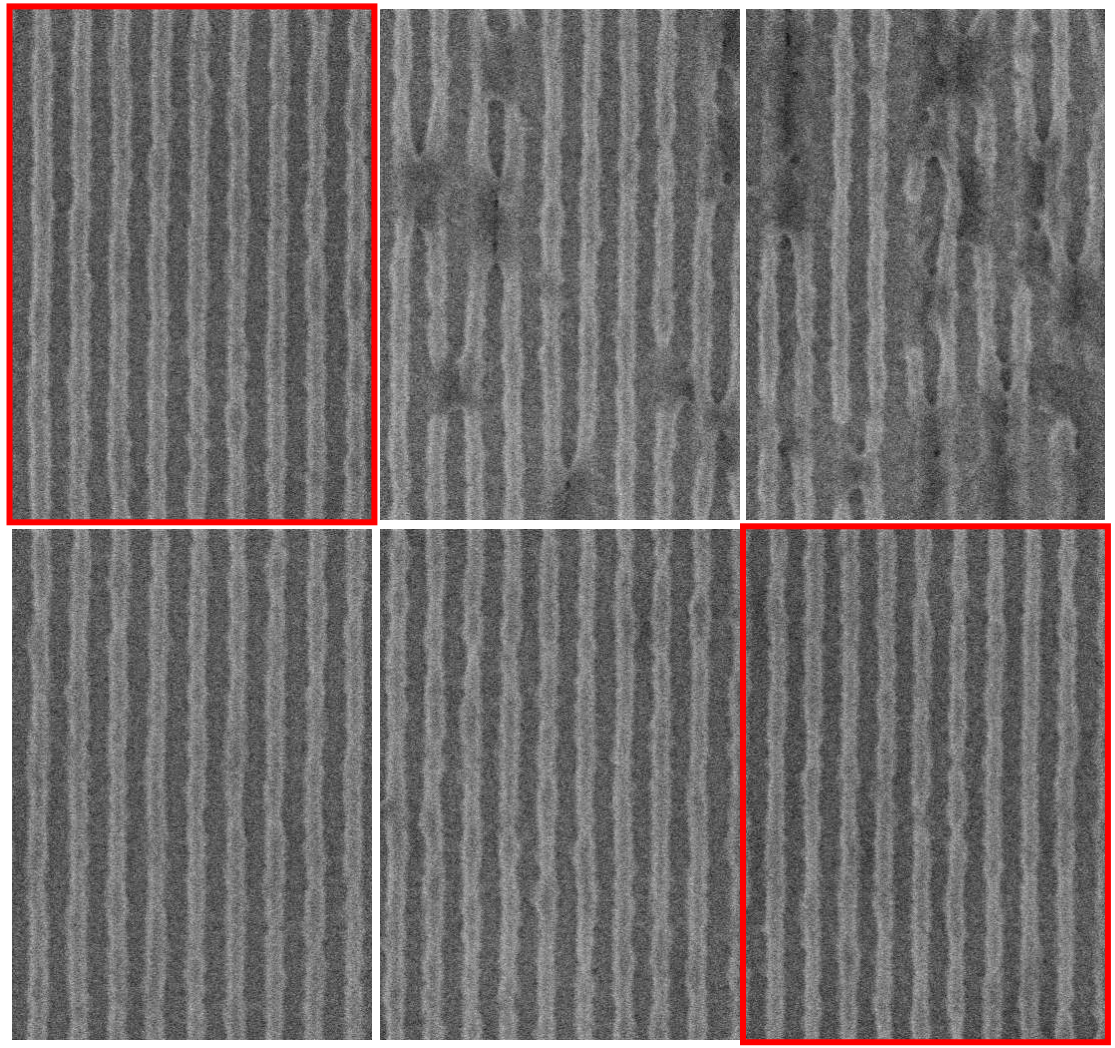


TMAH
0.26N

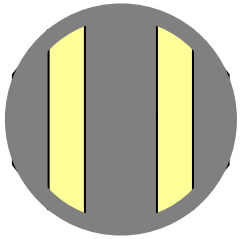
New Developer



TBAH
(Tetrabutyl ammonium hydrooxide)
0.26N



SFET NA0.3
Resist : SSR4
Thick. : 50nm



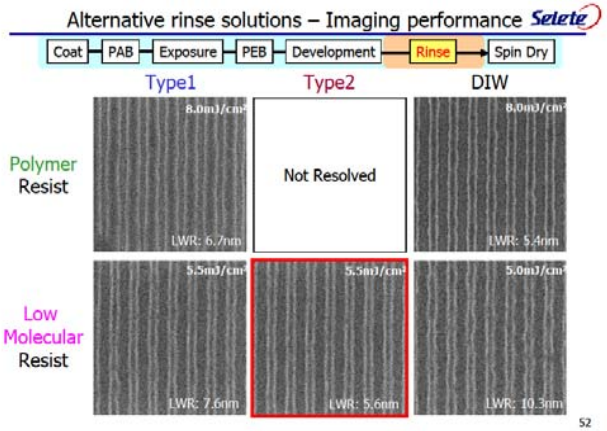
X-slit

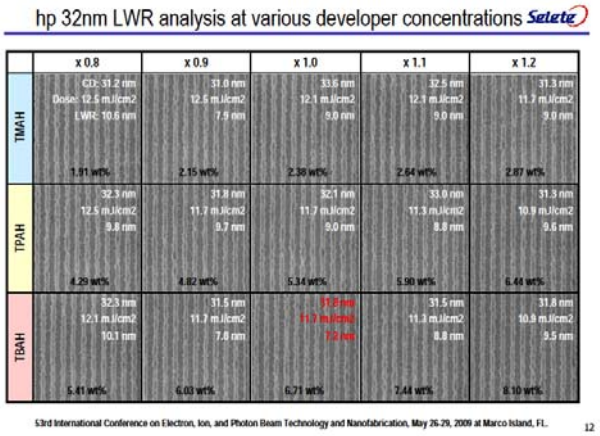
Resolution limit achieved hp24nm

LWR reduction by process

Selete's previous reports

- Post development rinse (T.Itani, ICPST2009)
- Developer solution (J.J. Santillian, EIPBN2009)





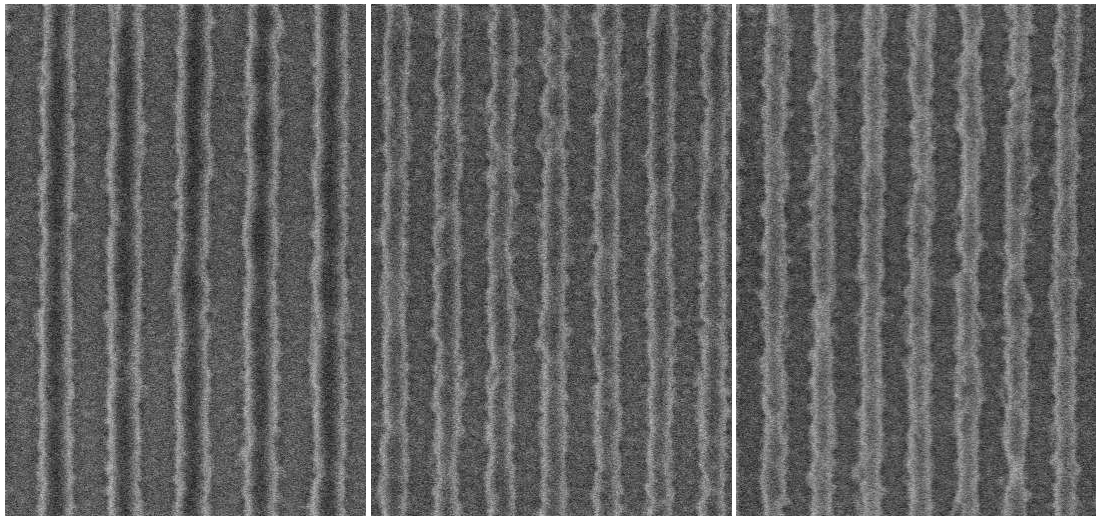
Previous reports

- Under layer (H.Xu,SPIE2009)
- Solvent Vapor treatment (Y.Inatomi, SPIE2006)
- Post development bake (K.Sho, SPIE2005)
- Developer concentration (Ryoo, SPIE2001)
- Development process (K.Matsunaga, MNC1998)

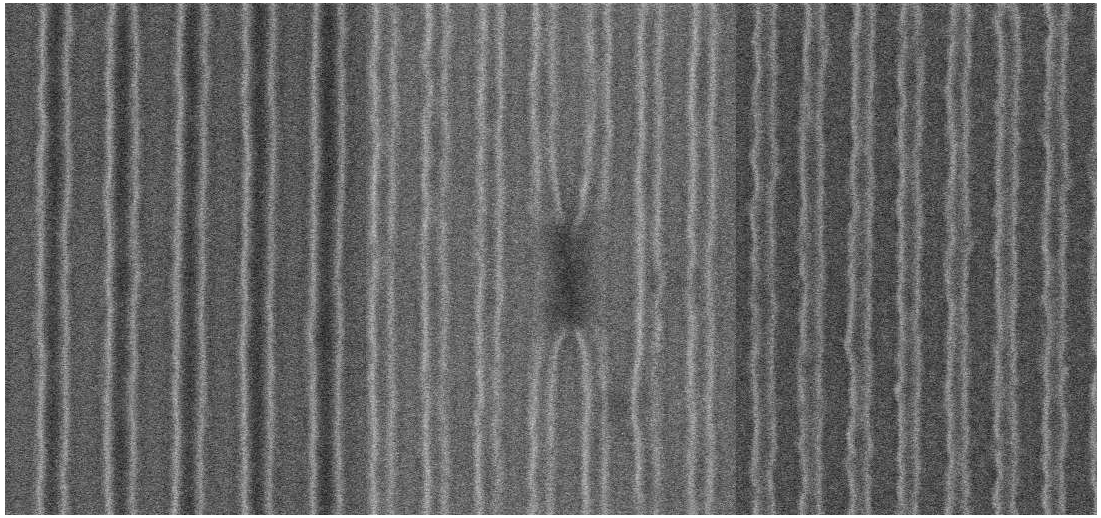
LWR Improvement by New Rinse Solution

45nm L/S **35nm L/S** **32nm L/S**

DIW

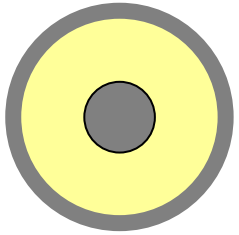


New Rinse Solution



L/S	45nm	35nm	32nm
DIW	5.9nm	7.0nm	8.2nm
New Rinse	4.9nm	5.8nm	6.5nm

SFET NA0.3
Resist : PHS type
Thick. : 60nm
Developer: TMAH



Annular
(0.7/0.3)

LWR was improved by 20% at hp32nm

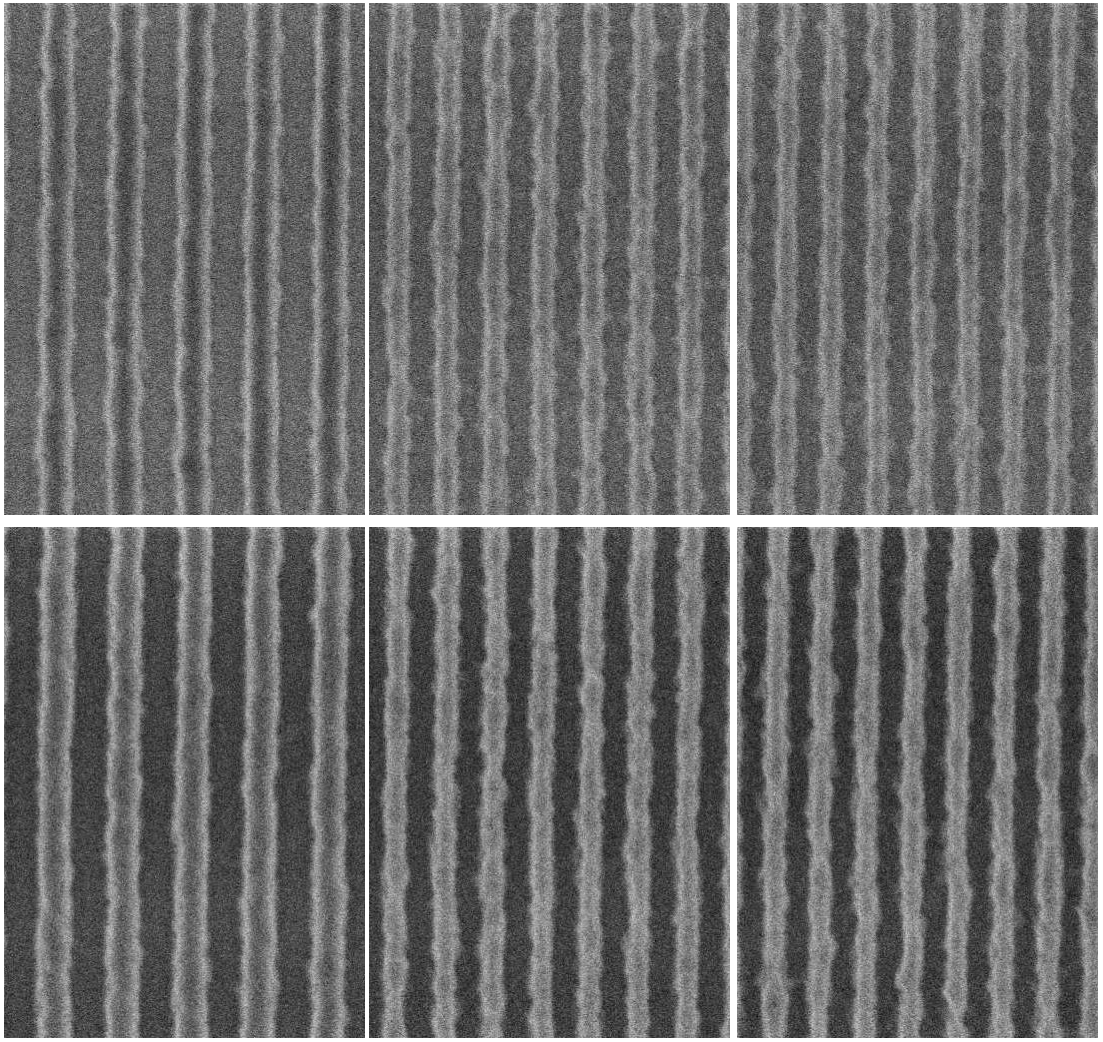
LWR Improvement by Under-layer

Selete

45nm L/S **32nm L/S** **30nm L/S**

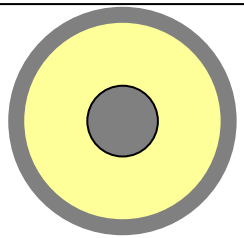
On Si

On Under-layer



L/S	45nm	32nm	30nm
Si	5.7nm	7.4nm	8.2nm
Under-layer	5.4nm	7.1nm	7.5nm

SFET NA0.3
Resist : PHS type
Thick. : 60nm
Developer: TMAH



Annular
(0.7/0.3)

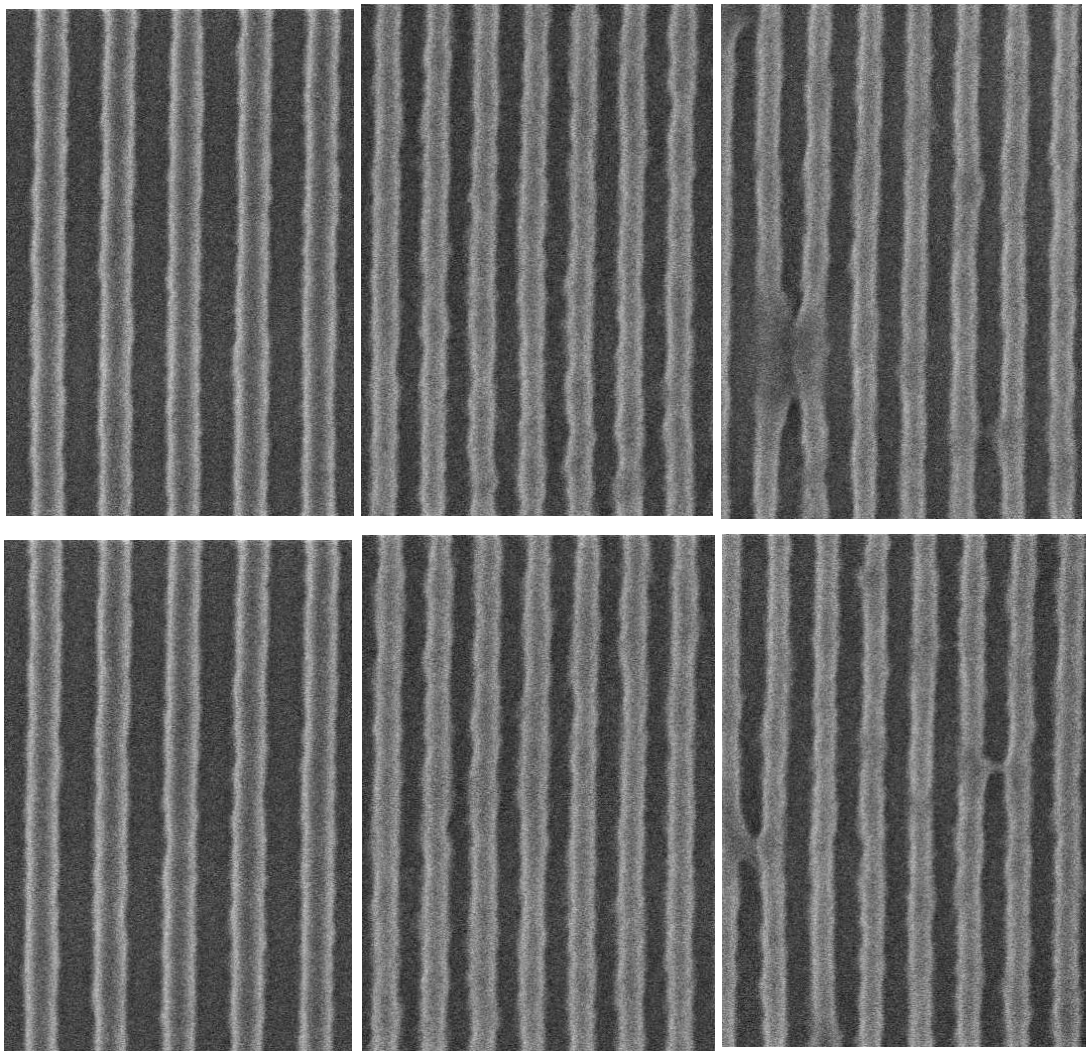
LWR was improved by 8.5% at hp30nm

LWR Improvement by Optimized development recipe

45nm L/S **35nm L/S** **32nm L/S**

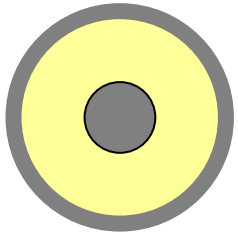
Conv. Dev. recipe

Optimized Dev. recipe



L/S	45nm	35nm	32nm
Conv. Dev.	4.3nm	6.6nm	7.8nm
New Dev.	3.7nm	5.4nm	7.3nm

SFET NA0.3
Resist : Acrylic type
Thick. : 70nm
Developer: TMAH



Annular
(0.7/0.3)

LWR was improved by 14% at hp45nm (3.7nm)

Conclusion

- Resist Materials
  - SSR4 and SSR5 were released for hp2x-nm evaluation.
  - LWR of SSR4 was improved. (5.5nm@hp32nm)
  - Sensitivity of SSR5 almost achieved the target. (10.7mJ/cm2@hp32nm)

- Resist Process
  - Pattern collapse of SSR4 was improved using new developer solution.
  - Resolution limit was achieved hp24nm by prevention of pattern collapse.
  - About 20% reduction of LWR is expected using resist process.

- Action Item
  - Resist process will be optimized to SSR for hp2x-nm evaluation.

Acknowledgements

- A part of this work is supported by New Energy and Industrial Technology Development Organization (NEDO).
- Selete member companies (EUV Lithomask program).
- Resists and materials suppliers.

Appendix

Measurement Conditions of CD-SEM

SEM Condition	
Tool	HITACHI S-9380Ⅱ
HV	800 V
Ip	5.0 pA
Optics Mode	HighReso.
Frame	32

	Line Width	LWR condition
Magnification	200K	
Rotation Corr.	On	
Inverse	Off	
Inspect Area	350	
Meas. Point	350	
Sum Lines/Point	32	17
ACD	Auto / Target 5 /	
Method	Thres. 50%	
Smoothing	7	7
differential	-	5