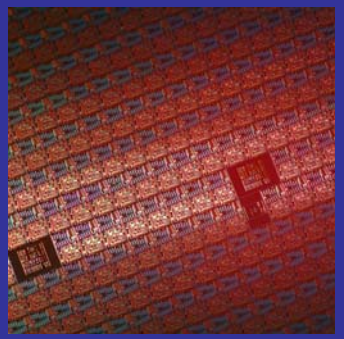
Accelerating the next technology revolution

Implementing E-beam Correction Strategies for Compensation of EUVL Mask Non-flatness

J. Sohn[a], K. Orvek[a], R. Engelstad[b], P. Vukkadala[b], S. Yoshitake[c], S. Raghunathan[d], T. Laursen[e], J. Zimmerman[e], B. Connolly[f], and J.H. Peters[g]

[a] SEMATECH Inc.
[b] CMC, University of Wisconsin - Madison
[c] NuFlare Technology Inc.
[d] CNSE, State University of New York at Albany
[e] ASML, Albany, NY
[f] TOPPAN, Dresden, Germany
[g] AMTC, Dresden, Germany



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Outline

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  - Issues with Polynomial Fits
- Mask Building with Compensation Methodologies
  - Mask Design
  - Compensation Schemes including Finite Element Modeling and Analytical Calculations
  - Predicted IP Errors and Mask iPro Data
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- Acknowledgements

Introduction

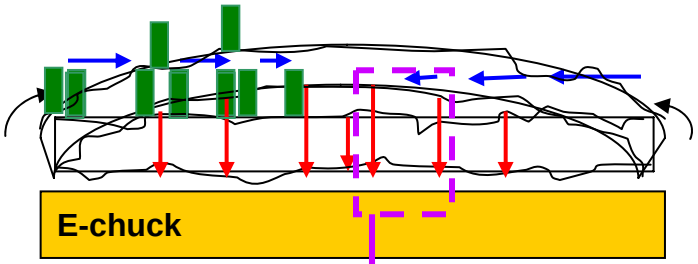
- EUVL mask non-flatness contributes to overlay errors in scanners.
- Required non-flatness targets to meet overlay budgets are tight.
  - SEMI P37 recommends the flatness specification of $\leq$ 30 nm.
  - Aggressive polish can add cost and defects to blanks.
- An image placement (IP) correction methodology was introduced to allow the specifications to be relaxed.
- The industry has been working on several methods for modeling required image placement compensations.
  - Finite element modeling (FEM) and analytical calculation method

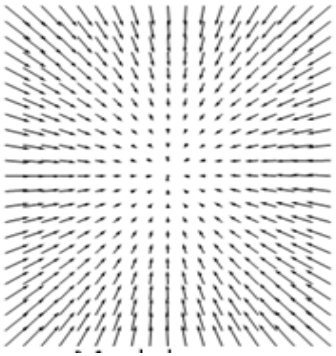
Introduction (continued)

- The key requirement of IP correction methodology is that the chuck flatness must be negligible so it can be neglected in modeling.
  - Chuck flatness in the ADT is reported to be ~50 nm, which is negligible for this work.
- If the compensation works, we are aiming to target EUV mask flatness at $\geq$ 300 nm (typical optical substrate value).
  - Enables reduced cost of ownership and improved substrate yield.
- Valuable learning was obtained from a previous study with test masks built by Samsung. Learning was incorporated into the build of commercial masks for the overlay experiment.
- This presentation presents the first demonstration of a flatness compensation methodology using commercial masks.

IP Error Contributions from Chucking

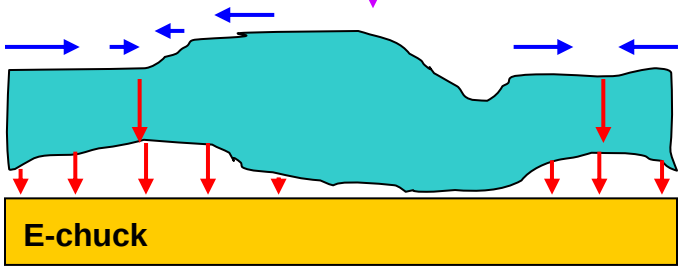
- Bow distortion due to mask flattening by e-chucking (correctable mostly by scanner)

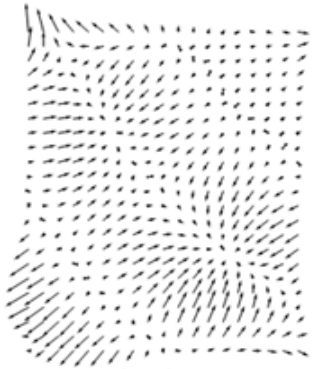




bow IP Error

- Non-linear terms from the backside non-flatness that are transferred to the frontside (not scanner-correctable)

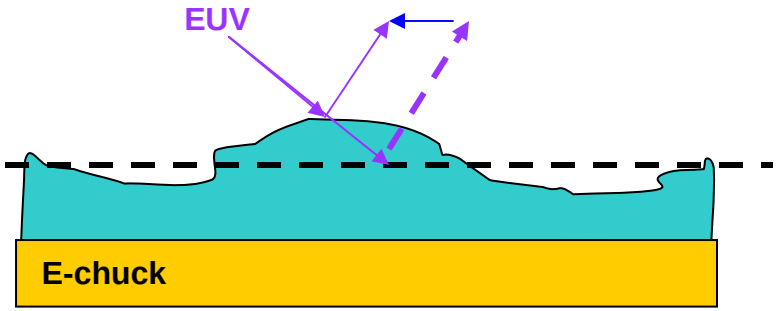




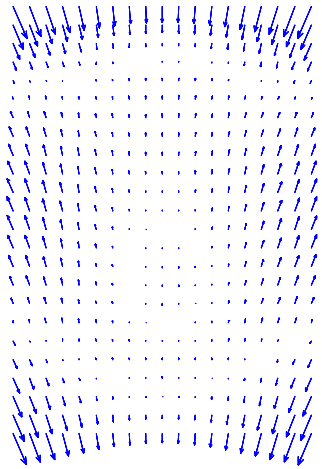
backside IP Error

IP Error Contribution from Non-flatness

- Net non-flatness (z-height) was accumulated from both frontside and backside.
- If we neglect the chuck surface flatness, the final chucked shape will be approximated by the thickness variation.



$$(\text{IP Error})_{\text{Z-Height}} = \frac{\Delta Z \times \tan 6^{\circ}}{4} \cong \frac{\Delta Z}{40}$$



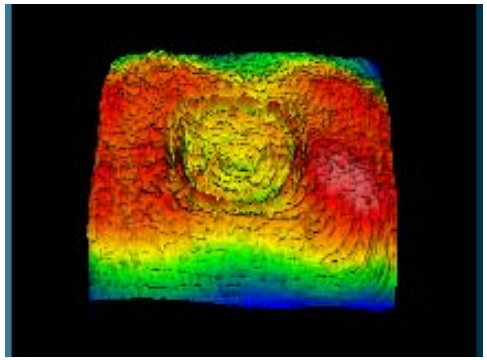
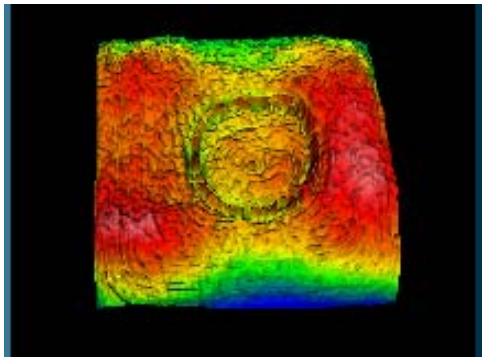
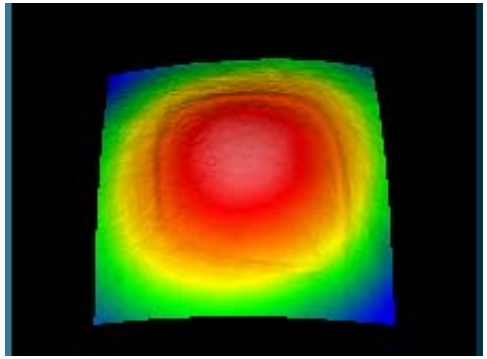
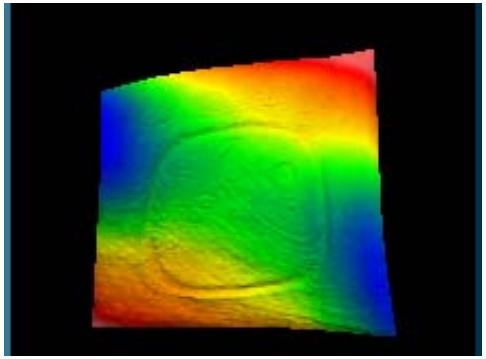
Final Frontside IP Error

Flatness Compensation Methodology

1. Measure blank flatness on both sides
2. Model the effect of chucking the bowed mask flat in the scanner
3. Calculate image placement errors due to residual z-height after chucking
4. Generate a table of combined errors
5. Reverse the sign of the errors → compensation table
6. Add the compensation table into the e-beam job deck
7. Expose wafers in the ADT using both “flat” and “non-flat” masks
8. Measure the overlay of the “non-flat” mask to the“flat” mask

Substrate Flatness Data

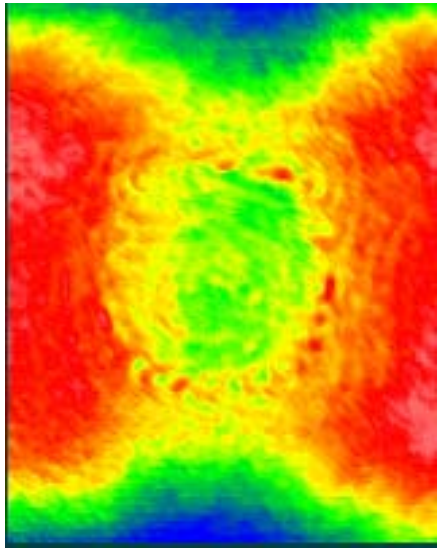
Quality Area 142 × 142 cm^2

	Front	Back
"Flat" Substrate (State-of-the-art flatness)	 66 nm	 62 nm
"Non-flat" Substrate (Typical optical flatness)	 576 nm	 429 nm

Blank Thickness Variation (TV) Data

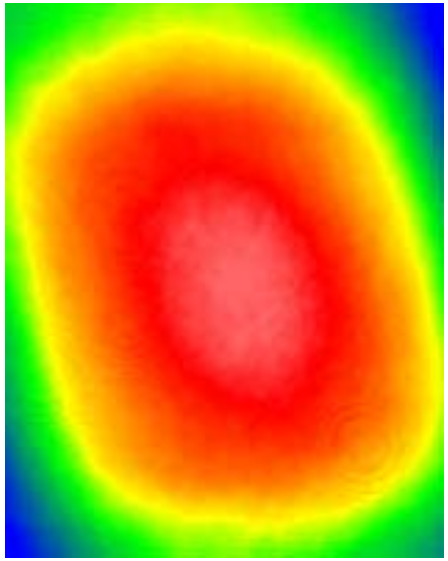
Scanning Field Area

"Flat" Blank TV



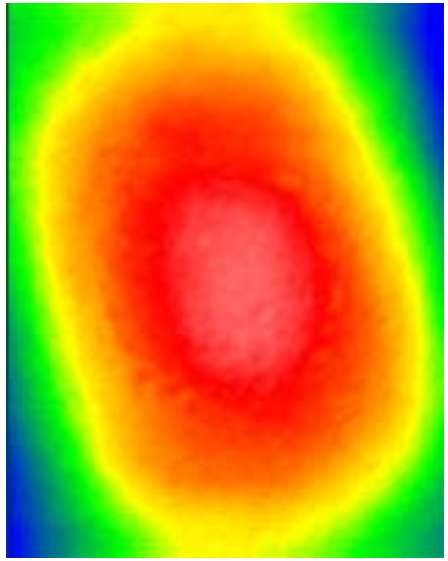
PV = 74 nm

"Non-flat" Blank TV



PV = 412 nm

Subtraction
(Overlay effect on TV)



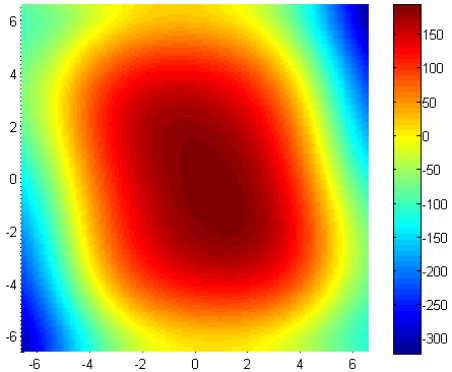
PV = 409 nm

- Overlay will be affected by this overall thickness variation

FEM Modeling Results

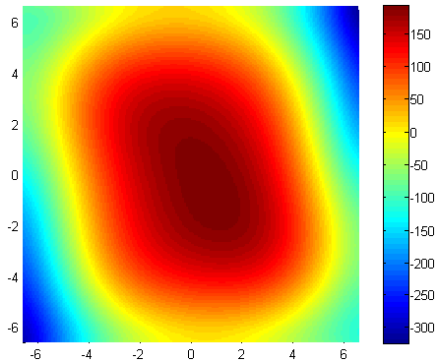
- Chucked reticle OPD of “non-flat” blank
- Plots cover an area of 132 × 132 mm^2

Reticle OPD (FE Simulation) 8x8 Polynomial Fit



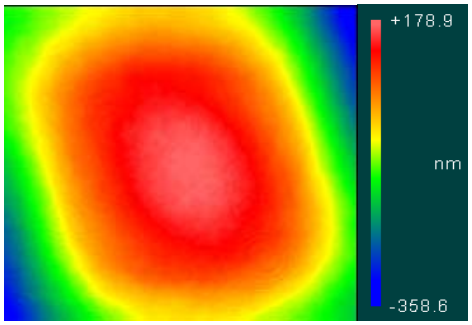
P-V = 516 nm

Thickness Variation Fitted Data 8x8 Polynomial Fit



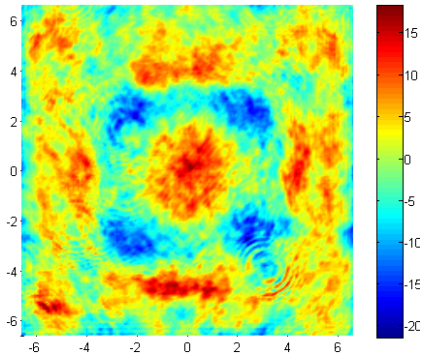
P-V = 517 nm

Thickness Variation Raw Data



P-V = 537 nm

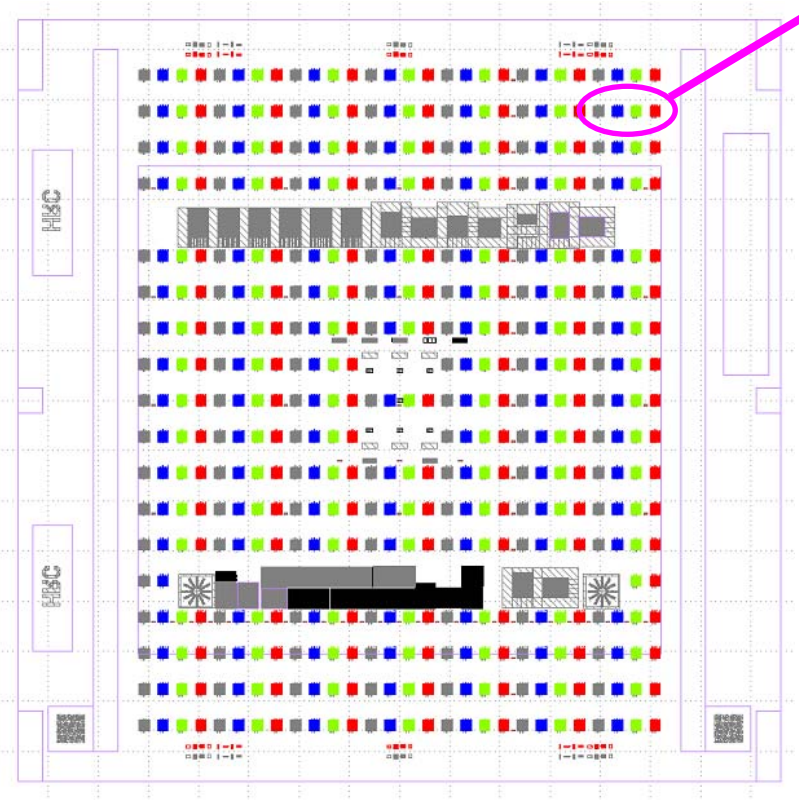
TV Delta Raw Data – Fitted Data



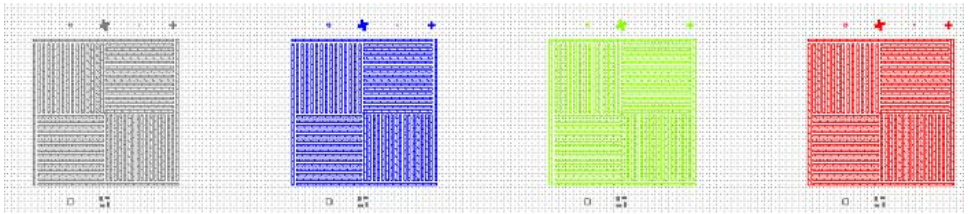
Max. Difference = 40 nm

- Raw thickness variation (frontside – backside) is a good approximation of final chucked front-surface
- **Polynomial fitting misses high frequency data**
  - It could be a real flatness variation and/or from metrology errors
  - Could create a limit to how far compensation can be extended

SEMATECH Mask Design



Repeating set of 4 ASML XPA alignment marks



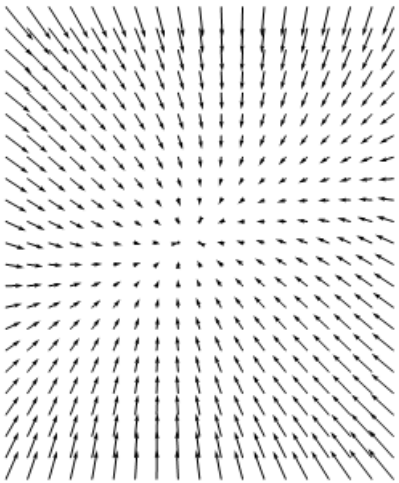
- One left uncompensated
- Up to 3 compensation schemes: For this work
  - Finite Element Method by University of Wisconsin-Madison (UW)
  - Analytical Method by UW
  - Analytical Method by NuFlare Technology Inc.

Example IP Error Vector Plots

University of Wisconsin Analytical Model

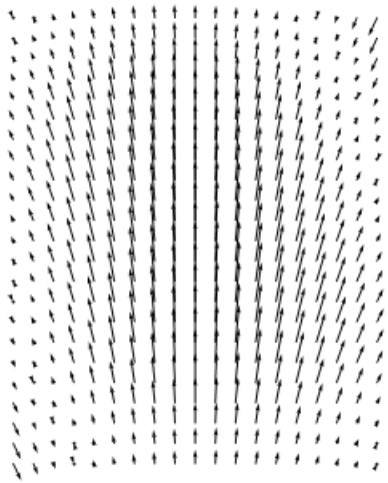
"Non-flat" blank – all values at mask level

IPE_{IPD}



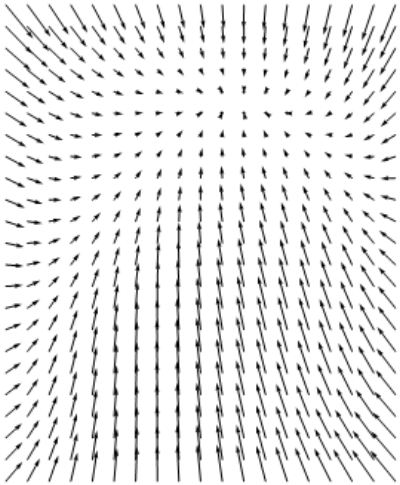
X: Max = 35 nm, Min = -33 nm
Y: Max = 39 nm, Min = -43 nm

IPE_{OPD}



X: Max = 6 nm, Min = -6 nm
Y: Max = 27 nm, Min = -12 nm

IPE_{TOTAL}

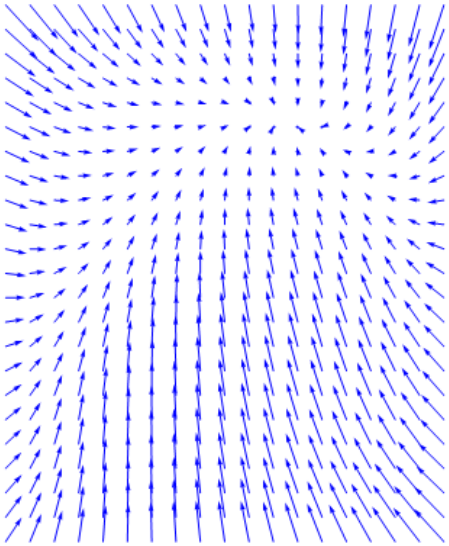
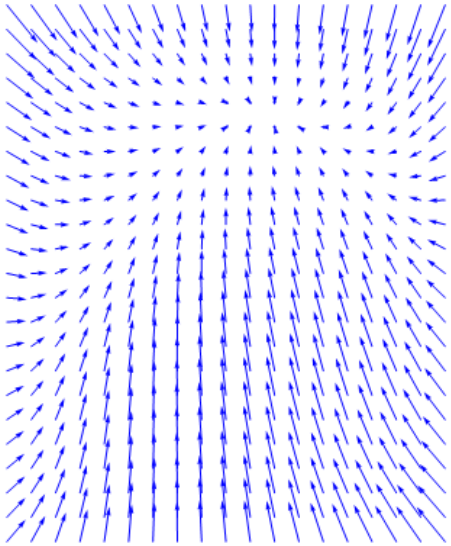
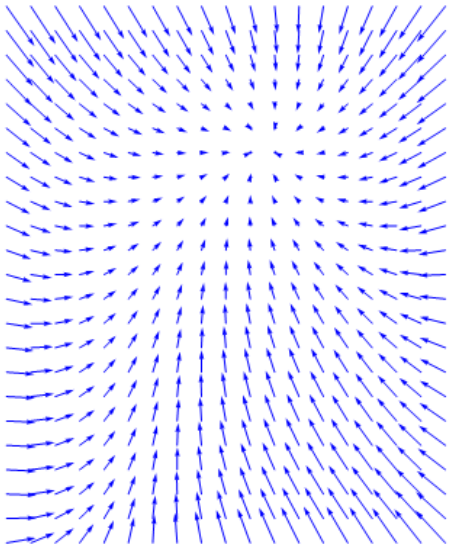


X: Max = 35 nm, Min = -33 nm
Y: Max = 48 nm, Min = -49 nm

- Here the "non-flat" blank (~500 nm non-flatness) has a 27 nm max IP error from z-height, which flatness compensation must correct in order for us to use blanks with such non-flatness.
- Most error comes from IPD correction from mask flattening by the chuck. Most of this can be corrected by the scanner.

Total IP Error Vector Plots

– "Non-flat" mask at mask level

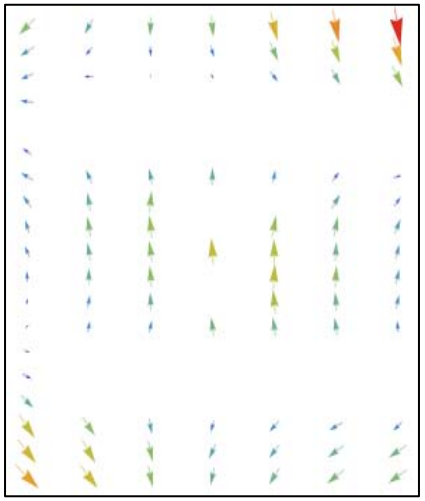
	UW FEM	UW AM	NF AM
			
19×23 matrix	**X:** Max = 39 nm, 3σ = 43 nm **Y:** Max = 53 nm, 3σ = 74 nm	**X:** Max = 35 nm, 3σ = 40 nm **Y:** Max = 49 nm, 3σ = 74 nm	**X:** Max = 35 nm, 3σ = 56 nm **Y:** Max = 47 nm, 3σ = 64 nm
Mask iPRO Data (7×19)	**X:** Max = 40 nm, 3σ = 37 nm **Y:** Max = 62 nm, 3σ = 74 nm	**X:** Max = 40 nm, 3σ = 35 nm **Y:** Max = 59 nm, 3σ = 74 nm	**X:** Max = 48 nm, 3σ = 52 nm **Y:** Max = 50 nm, 3σ = 66 nm

- iPRO data confirmed that masks were successfully fabricated with proposed compensation methods.

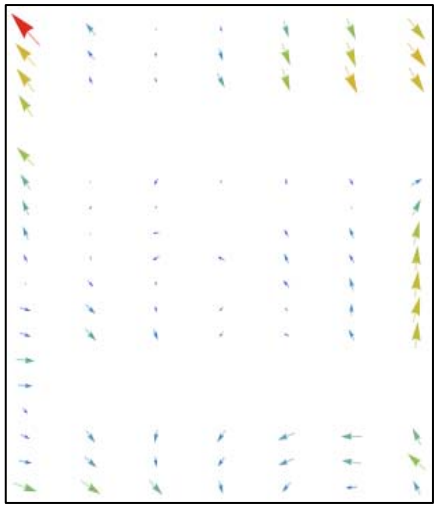
Overlay Data from Exposed Wafers on the ADT

Single Machine Overlay with Multiple Masks

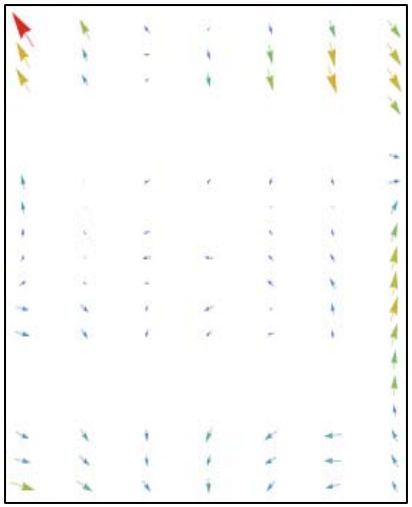
Uncompensated



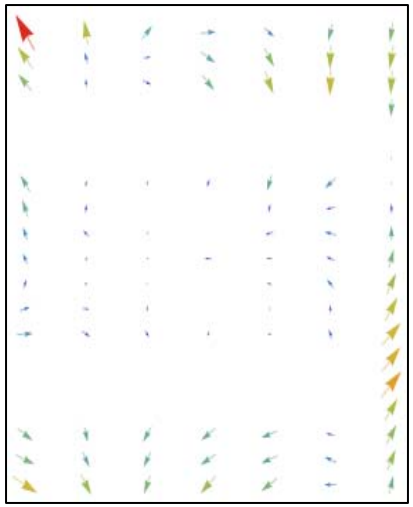
UW FEM



UW AM



NuFlare AM



Layout	X_{max}	$3\sigma x$	Y_{max}	$3\sigma y$
Uncomp	3.5	3.4	6.8	8.9
UW FEM	3.2	3.3	4.3	5.6
UW AM	3.1	3.1	4.9	5.4
NuFlare AM	3.2	3.7	5.0	6.3

- ADT machine overlay with single mask (zero nm mask non-flatness error) is ~3 nm.

- **Compensation improves overlay**
  - All models improved overlay by 24% to 39%.
- Data suggests that analytical method is sufficient for pilot-line production.

Overlay Analysis

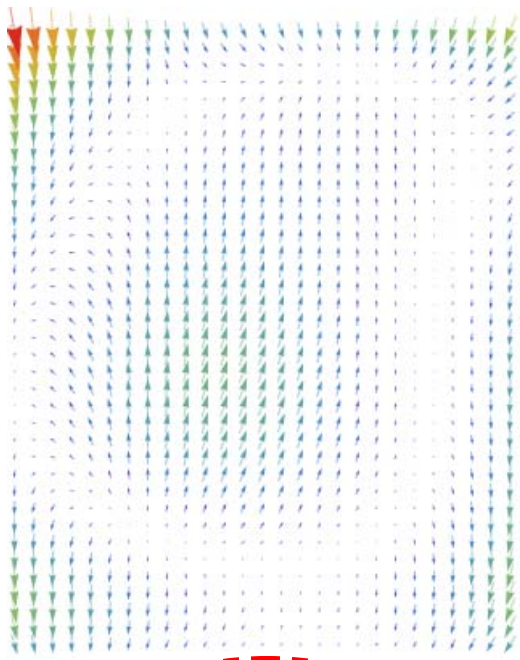
- The compensation did not do as well as predicted
  - ~ 30% improvement vs. over 50% expected
- Possible Reasons
  - The ADT's best SMO data are approximately ~3 nm max error
  - Non-flatness of the "flat" mask
  - Flatness metrology errors including gravity by holder
  - e-Beam writer tool error during mask building
  - Reproducibility error during mask chucking in the scanner
- These errors could create a residual field signature, which could be removed by subtracting the signature from the uncompensated data.

Removing Possible Error Signatures from Wafer Data

Uncompensated wafer overlay

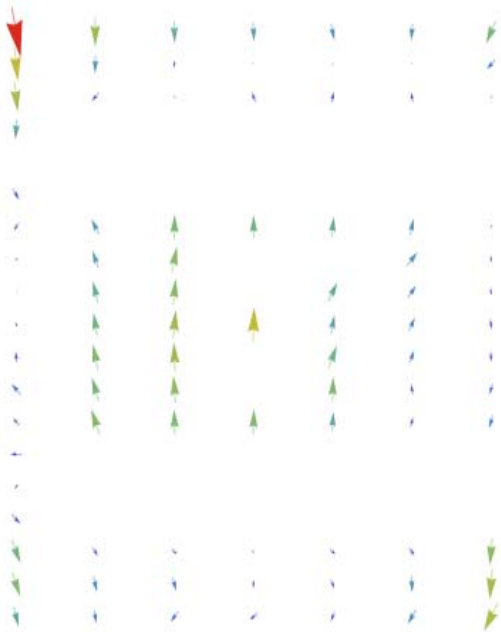
X: Max = 3.3 nm
Y: Max = 6.4 nm

Predicted wafer overlay error from analytical modeling



X: Max = 1.8 nm
Y: Max = 8.2 nm

Uncompensated – compensated

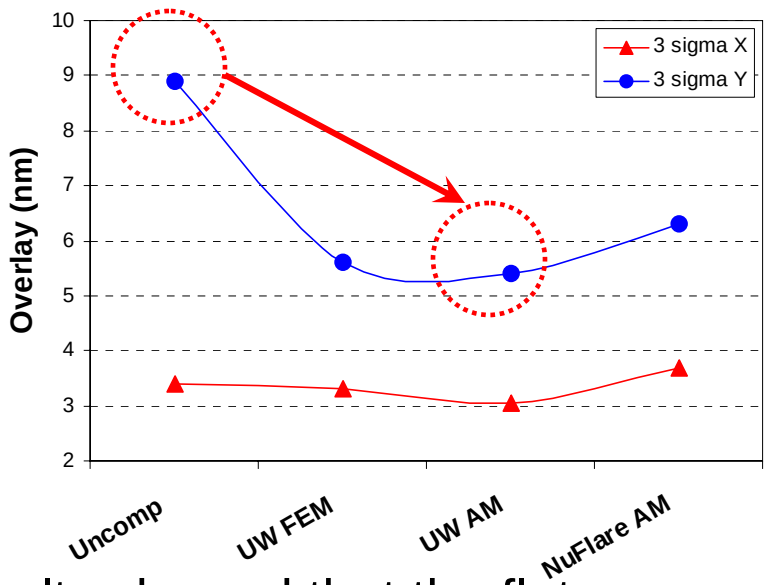


X: Max = 1.8 nm
Y: Max = 7.3 nm

- Good match to predicted errors once field signature is removed

Summary

- First commercial EUV masks were written with blank non-flatness compensation enabled.
- 'Flat' and 'Non-flat' masks were tested on ADT to determine overlay impact of compensation.
- Overlay Results



8.9 nm → 5.4 nm

39% improved

- The overlay results showed that the flatness compensation methodology works to reduce overlay errors with a > 300 nm "Non-flat" substrate.
- Data suggest that the analytical method is sufficient for flatness compensation.

Future Plan

- SEMATECH is planning to build another set of “flat” and “non-flat” commercial masks.
  - Overlay study on ADT will be done using “flat-A”/“flat-B” masks
    - Identify the best possible overlay without compensation
  - Comparion with “Non-flat” to “Flat” will verify if we can achieve equivalent results using non-flat masks with compensation
- The compensation methodology needs to be further refined with testing on pre-production tools with a tighter overlay requirements.

Conclusion

- Non-flatness compensation is a key enabler for EUV lithography.
- SEMATECH and partners demonstrated for the first time that non-flatness correction work.
- Flatness compensation should have a major impact on mask cost
  - enables relaxed flatness standards
  - easier to meet defect requirements (flatness/defectivity trade-off).

Acknowledgements

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- Frank Goodwin, Chawon Koh, Sean Huh; SEMATECH