Accurate Models for EUV Simulation and Their Use for Design Correction

Gian Francesco Lorusso, Jan Hermans, Bart Baudemprez, Eric Hendrickx (IMEC)

U. Klostermann, Stephen Jang, Lena Zavyalova, Jacob Sorensen, Weimin Gao, Kevin Lucas (Synopsys)

Goals

- The ASML EUV ADT became operational at IMEC since June 2008
- Experimental CD data became available to validate model and simulator accuracy

- **Full Resist Model (Calibration and Verification)**
- **OPC Model (Calibration and Verification)**

© imec 2009

Outline

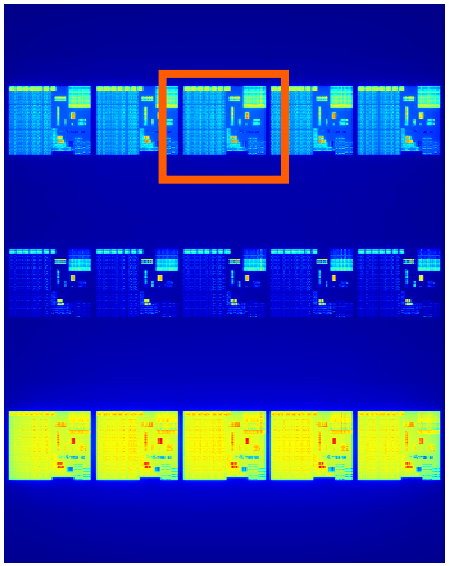
- Full Resist Model Calibration and Verification
  - Introduction
  - Calibration Data and Input Parameters
  - Model Fit and Output Parameters
  - Flare, CD and Pitch Validation
  - CDU Analysis and Simulation
- OPC Model Calibration and Verification
  - Data
    - Description
    - Proximity through Flare
    - MEEF
    - Precision and Stability
  - Flare
  - Shadowing
  - Modeling
    - Flare Map Accuracy
    - Flow and RMS Error
    - 2D Model Verification
- Conclusions

© imec 2009

Full Resist Model Calibration and Verification: Calibration Data and Input Parameters

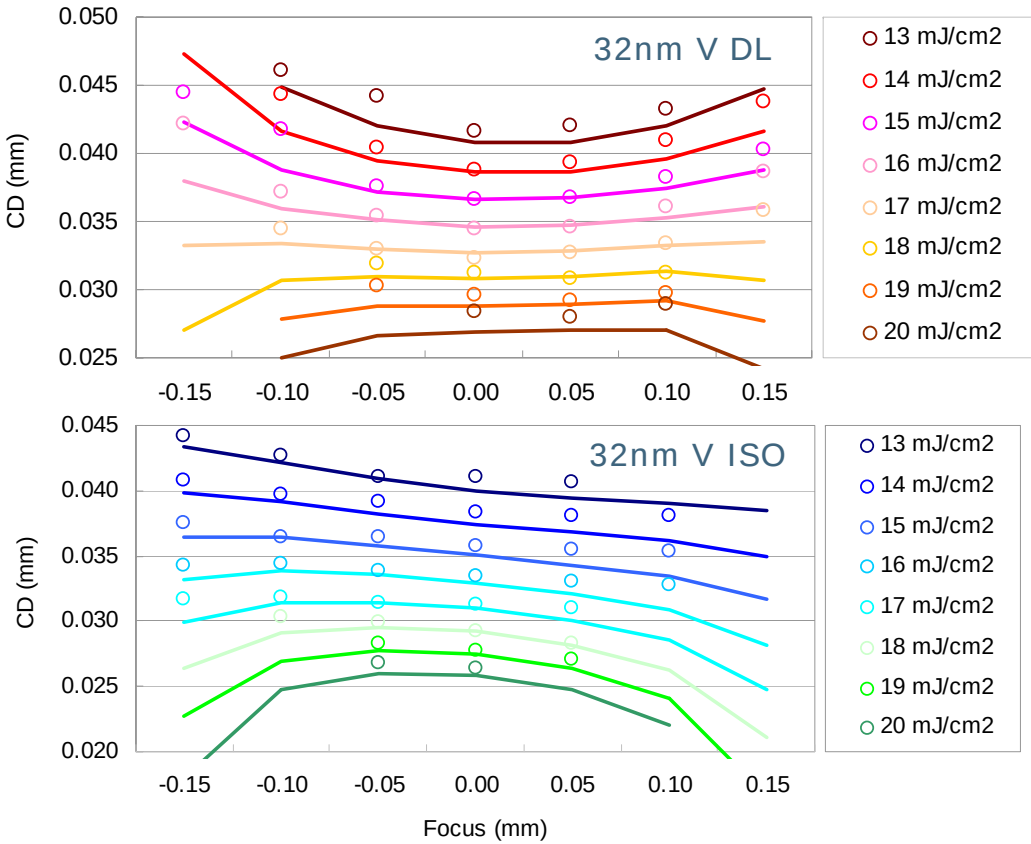
- **Reticle**
  - Die: 1 slit position, 1 scan position
- **Features**
  - CD 32, 36, 40nm
  - Pitch 1:1, 1:5
  - Vertical and Horizontal orientation
- **Layout**
  - FEM 7 x 9
- **Resist**
  - ShinEtsu SEVR-59 (65nm thickness)
- **Exposure**
  - NF = 0nm, DF = 50nm
  - NE = 17 mJ/cm^2, DE = 1 mJ/cm^2
- **Metrology / Analysis**
  - Hitachi CG4000

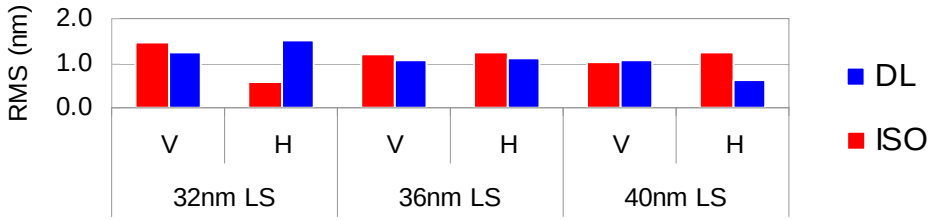
- **Optical**
  - λ = 13.6nm, σ = 0.5, NA = 0.25
- **Mask**
  - Mask CD data
- **Flare**
  - 6.3% (Calculated using Zeiss PSF)
- **Resist**
  - Traditional CAR



FEM's 32, 36, 40nm, DL and ISO, H and V

Full Resist Model Calibration and Verification: Model fit and Output Parameters



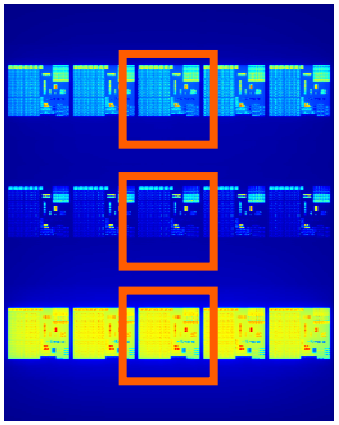


- **Lateral Diffusion length of 18nm**
  - Value in line with expectations
- **Large deprotection rate k1**
  - Deprotection rate was increased for this resist to achieve lower dose
- **Bossung Asymmetry**
  - The model reproduces well Bossung tilt and focus shift as a 3D effect

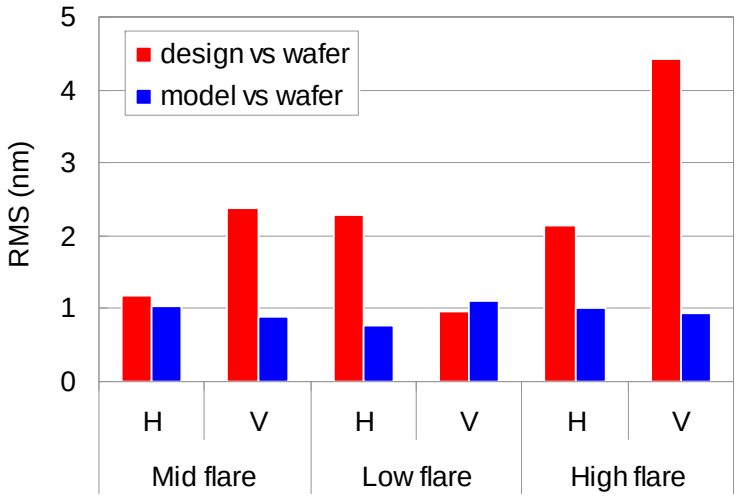
Overall Fit RMS ~ 1nm

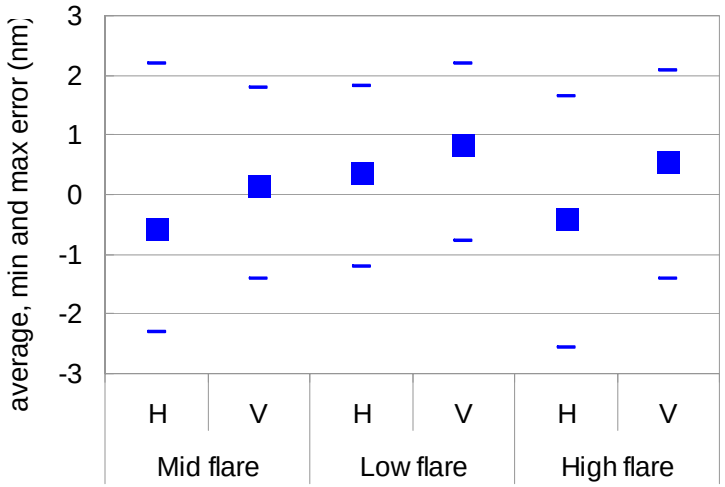
© imec 2009

Full Resist Model Calibration and Verification: Flare, CD and Pitch Validation



(See slide 12 for exposure conditions)

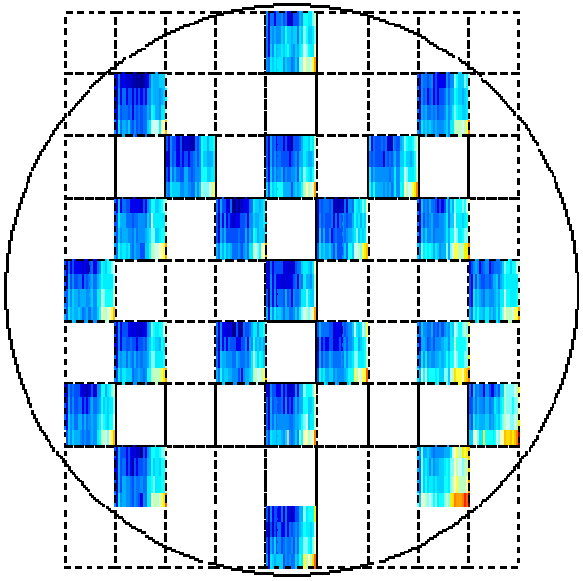


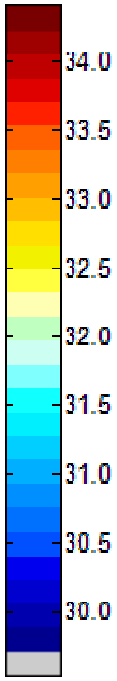


- Average model error ~ 0nm
- Maximum model error ~ 2nm
- Remaining tendencies
  - Model error is not random through pitch

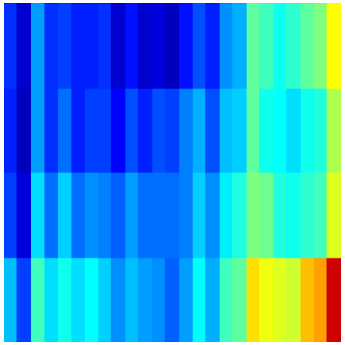
Overall Validation RMS ~1nm

Full Resist Model Calibration and Verification: CDU Analysis



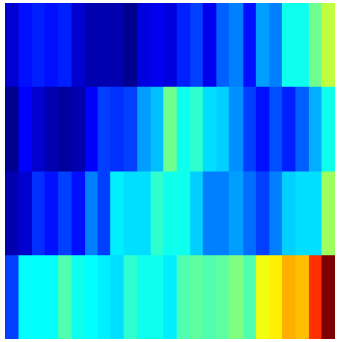


Intradie

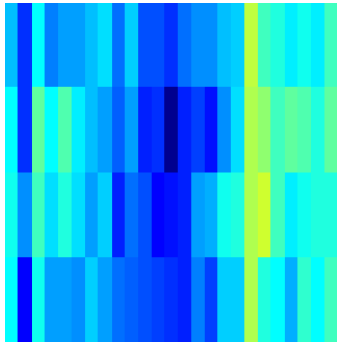


FW CDU HV = 1.88nm

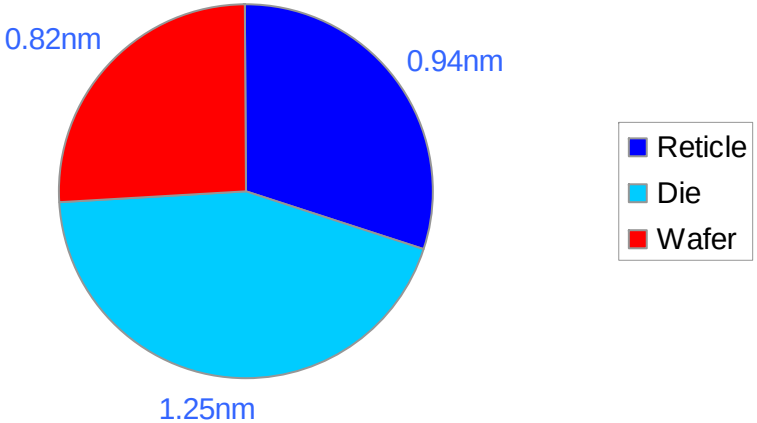
Mask



Intradie after REC



FW CDU HV = 1.62nm

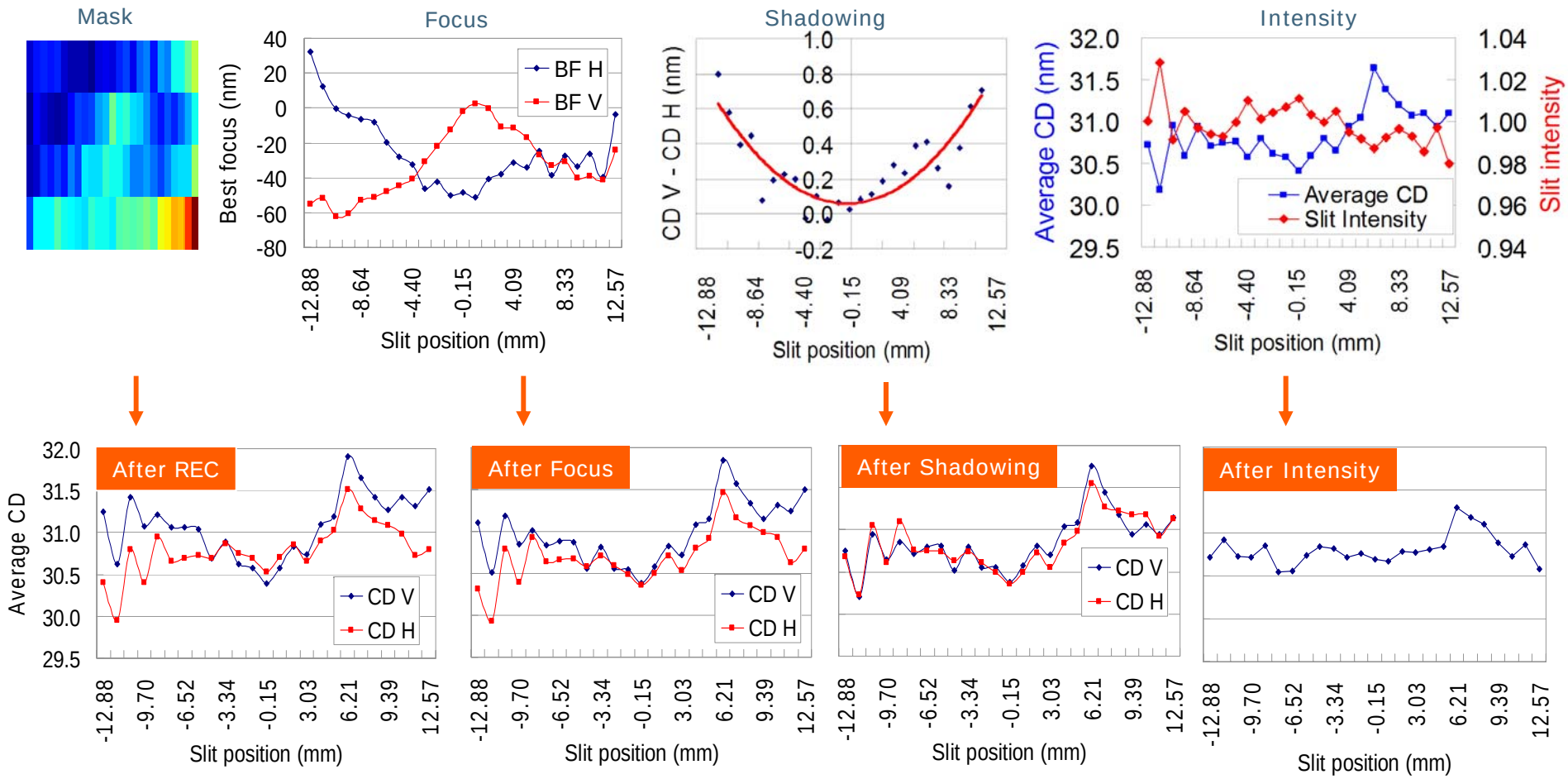


23 fields NF
Mask CDU32
65nm SEVR59
Wafer and Mask metrology
25 slits, 4 scans

32nm FW CDU NF HV = 1.88nm

© imec 2009

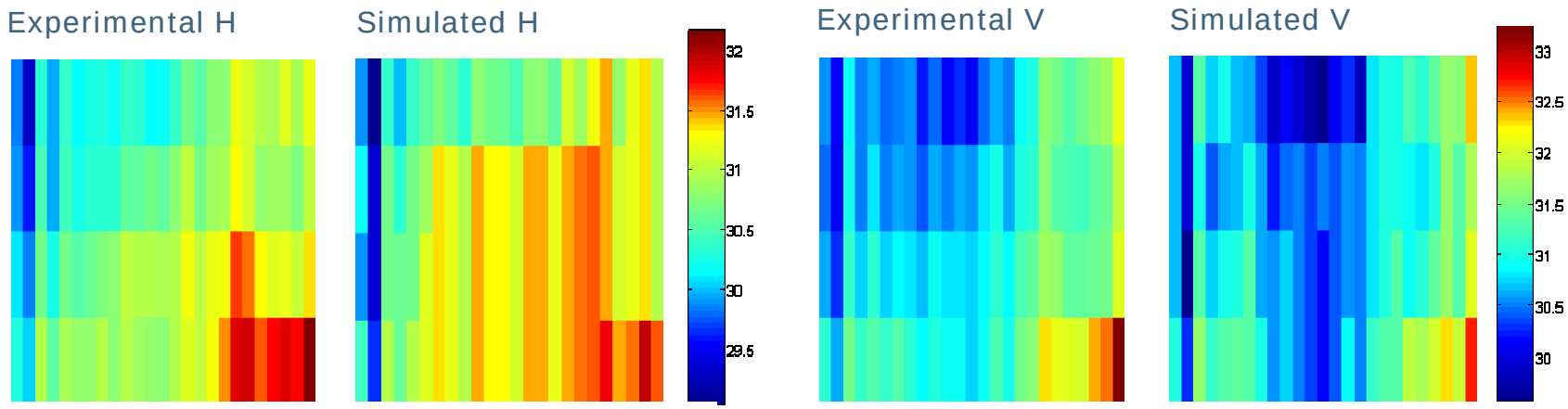
Full Resist Model Calibration and Verification: CDU Analysis

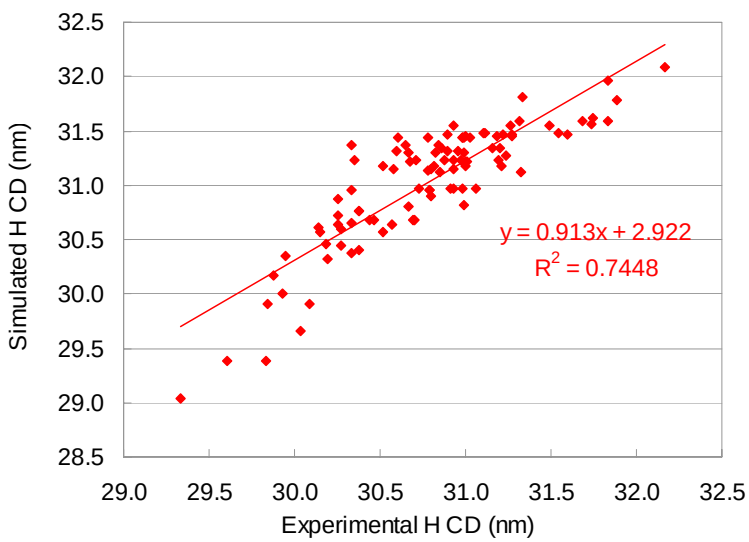


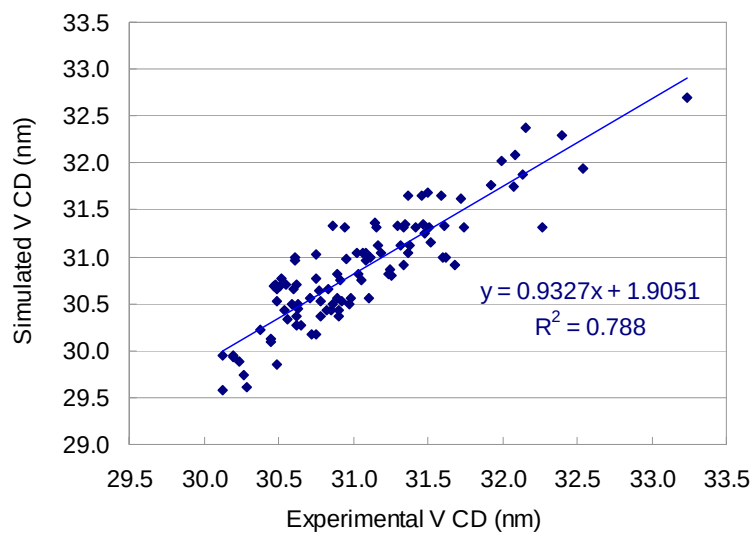
Intra-die CDU can be fully explained by mask, focus, shadowing and intensity fingerprints

Full Resist Model Calibration and Verification: CDU Simulation

Simulator Input: Measured mask CD, slit intensity, best focus and mask azimuth, SEVR59 full resist model







RMS error 0.3nm, maximum delta between experiment and simulation 1nm

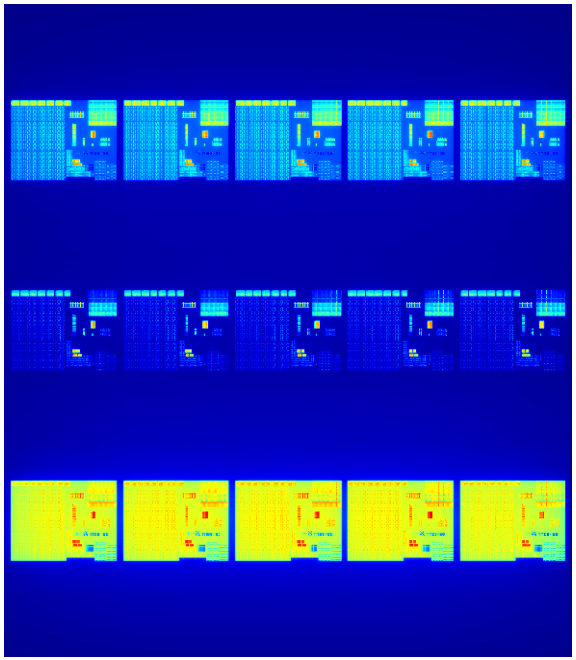
Outline

- Full Resist Model Calibration and Verification
  - Introduction
  - Calibration Data and Input Parameters
  - Model Fit and Output Parameters
  - Flare, CD and Pitch Validation
  - CDU Analysis and Simulation
- OPC Model Calibration and Verification
  - Data
    - Description
    - Proximity through Flare
    - MEEF
    - Precision and Stability
  - Flare
  - Shadowing
  - Modeling
    - Flare Map Accuracy
    - Flow and RMS Error
    - 2D Model Verification
- Conclusions

© imec 2009

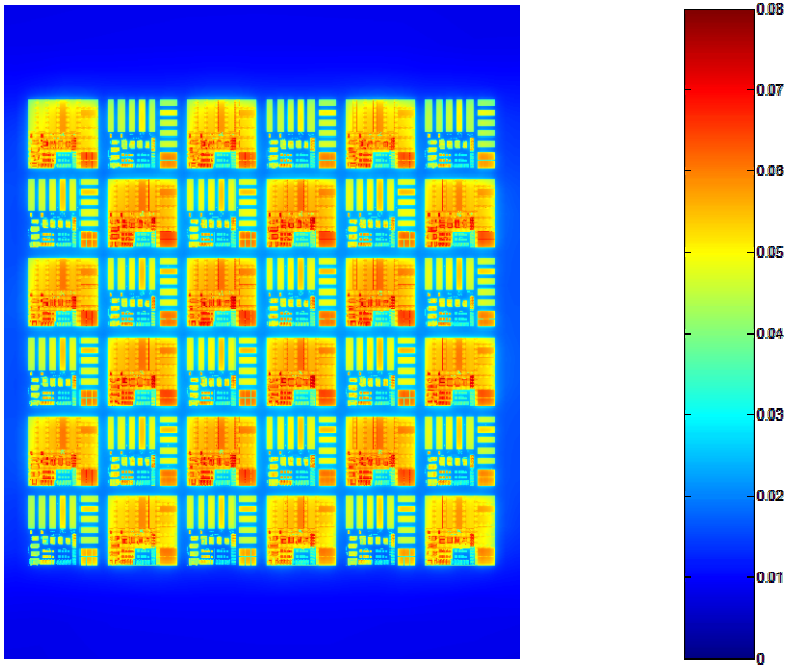
OPC Model Calibration and Verification: Introduction

TM08



Similar flare range

EUV OPC1



- Model Calibration and Verification
- 3 flare flavors, H and V features

- Corrected and uncorrected fields
- 2 flare flavors
- 2 corrected sub-dies

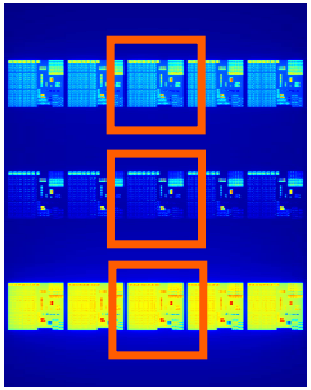
Goals:

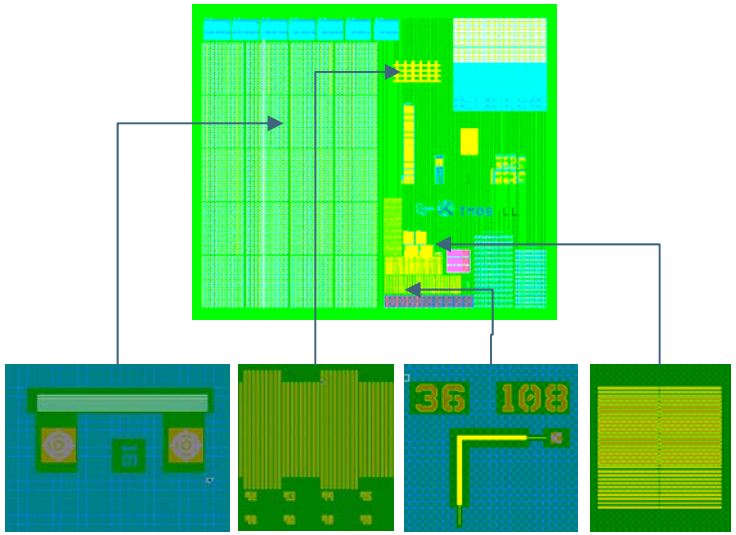
1. ***Calibrate and verify EUV OPC models on TM08***
2. ***Produce and verify corrected designs on EUV OPC1***

OPC Model Calibration and Verification Data: Description

- **Reticle**
  - Die: 1 slit position, 3 scan positions
- **Features**
  - L-bar CD 36 ÷ 46nm, Pitch 1:1 ÷ 1:5
  - MEEF S CD 35 ÷ 40nm, Pitch 1:6
  - MEEF L CD 32 ÷ 50nm, Pitch 1:1 ÷ 1:5
  - EOL, T-EOL, Brick Wall CD 32 ÷ 40nm
    - Vertical and Horizontal orientation
    - Mask measurements
    - > 700 CD measurements/die at wafer
- **Layout**
  - 23 fields exposed in nominal focus and dose
- **Resist**
  - ShinEtsu SEVR-59 (65nm thickness)
- **Metrology / Analysis**
  - Hitachi CG4000

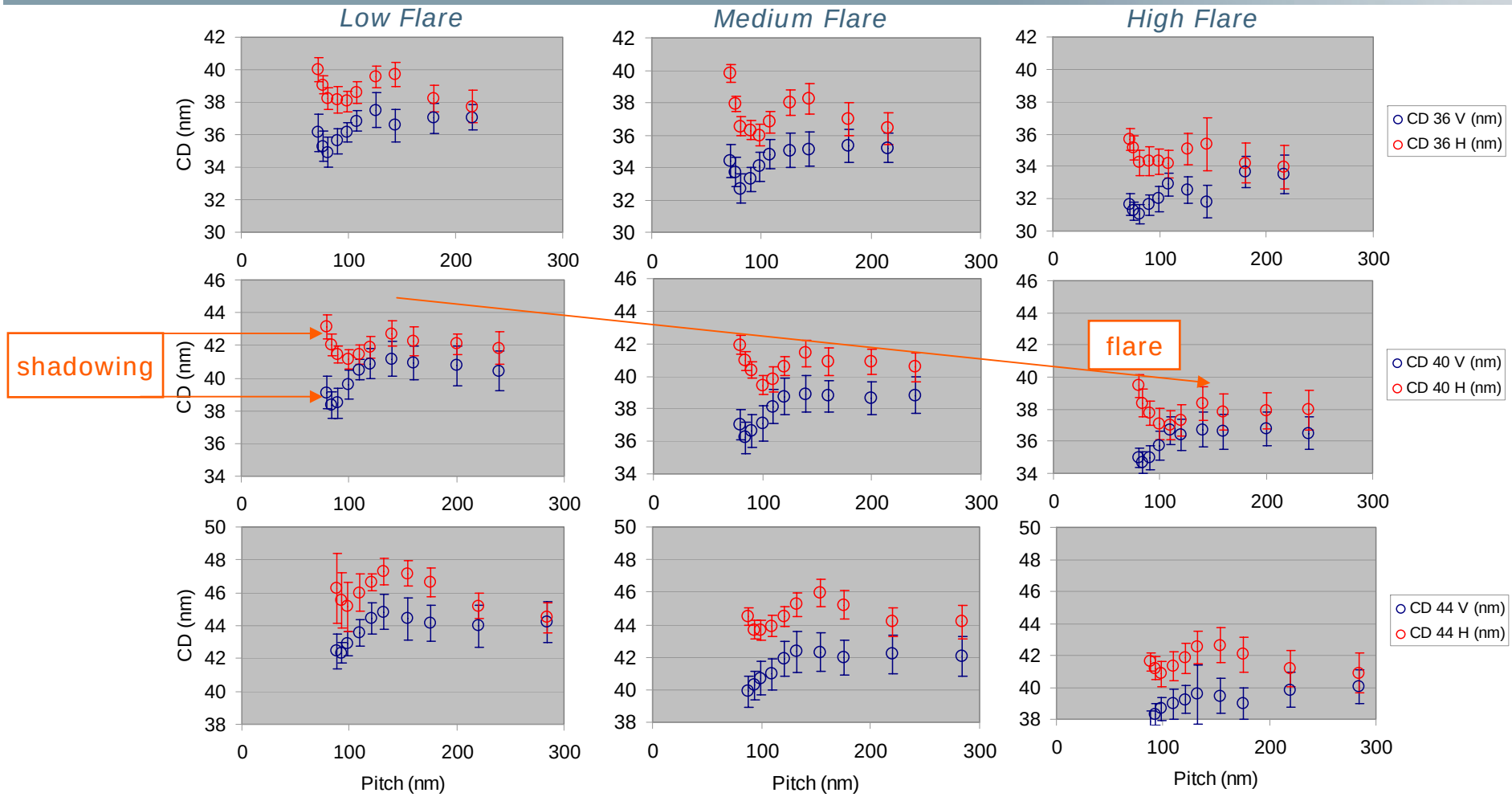
Die Layout





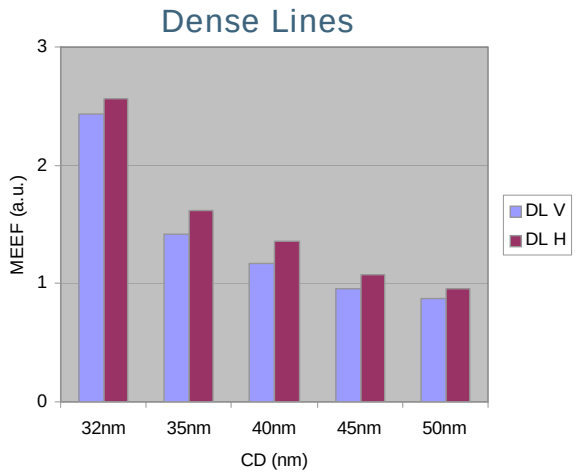
MEEF S *MEEF L* *L-bar* *EOL*

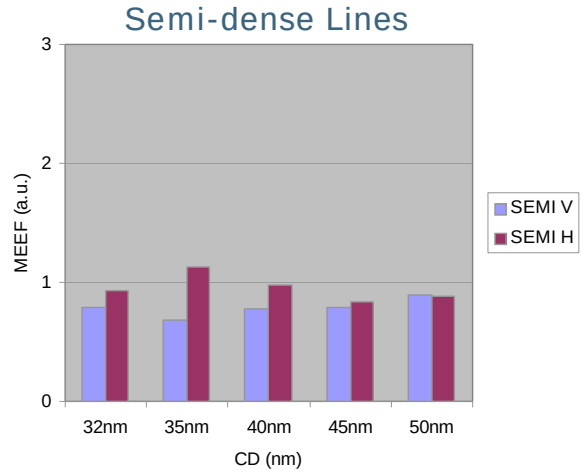
OPC Model Calibration and Verification Data: Proximity Through Flare

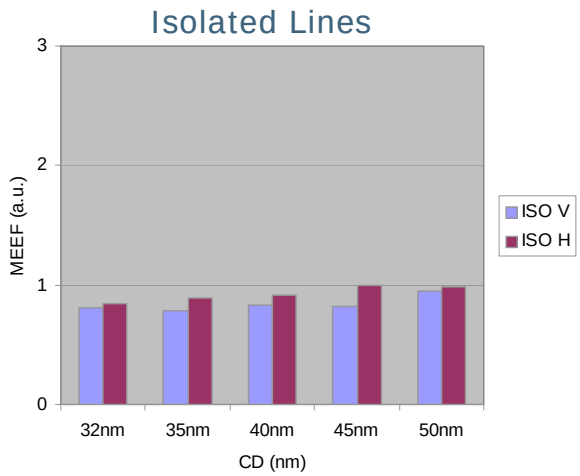


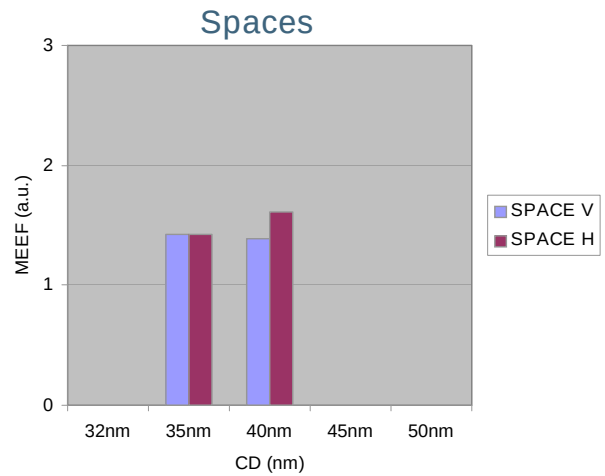
- ***Clear impact of flare on CD***
- ***Clear Impact of shadowing on HV bias***

OPC Model Calibration and Verification Data: MEEF





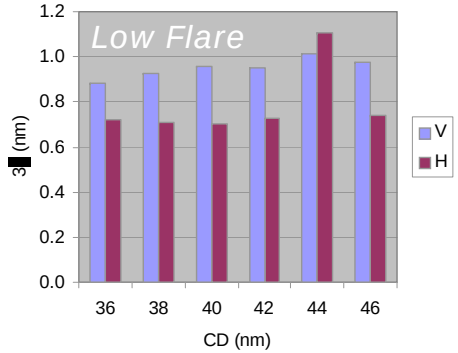


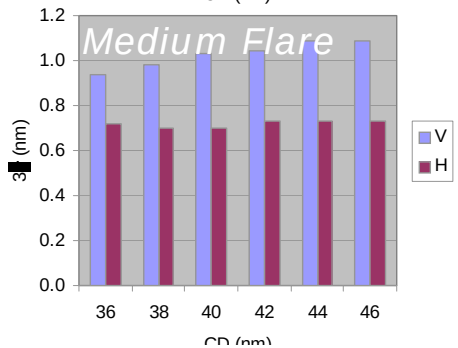


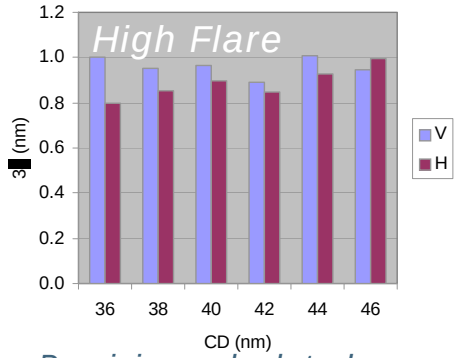
- ***MEEF data were used for calibration/validation and MEEF analysis***
- ***Larger MEEF for Small DL and for Spaces; MEEF ~1 for Semidense and Iso***
- ***Marginal differences between MEEF H and V or through flare***

© imec 2009

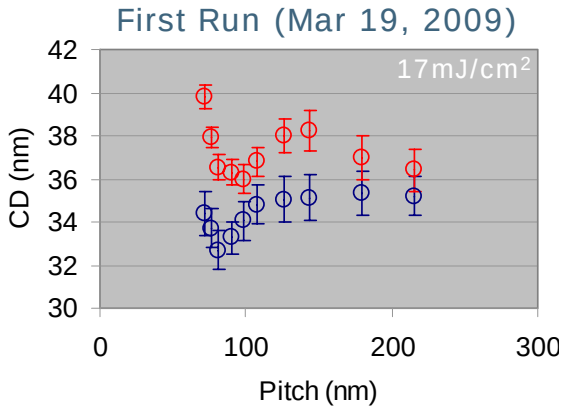
OPC Model Calibration and Verification Data: Precision and Stability

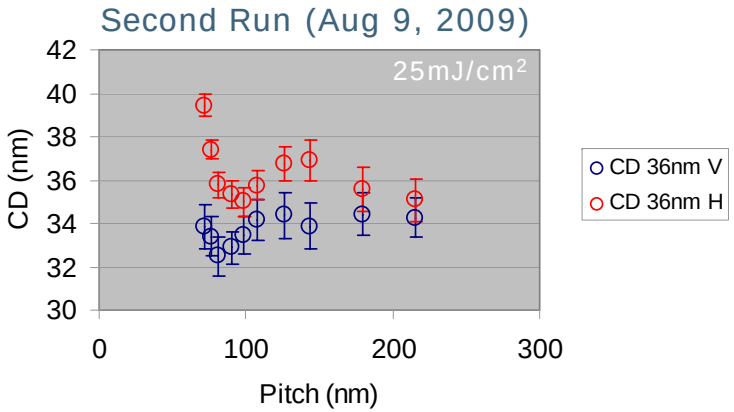






Precision calculated across uniformly exposed wafer on 23 fields



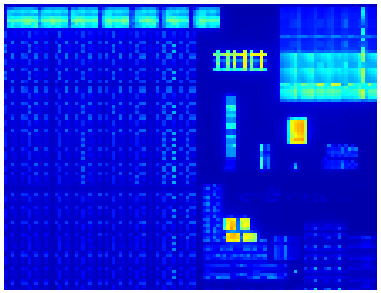


- **Flare** has been monitored at IMEC for over 1 year and resulted stable

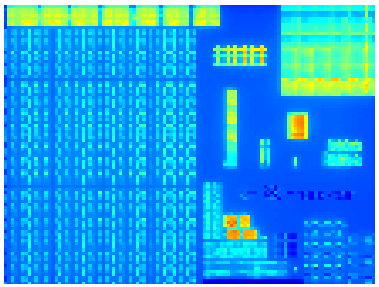
- ***Good precision across wafer (~ 1nm)***
- ***Good CD and Flare stability***

OPC Model Calibration and Verification: Flare

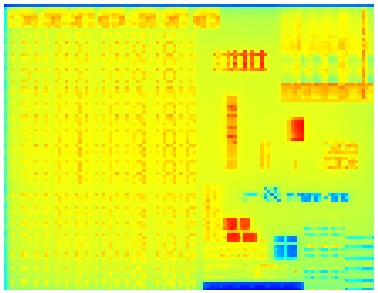
Low Flare

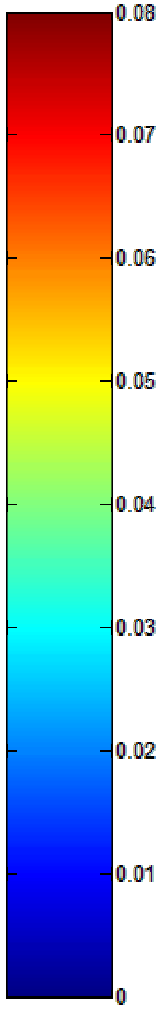


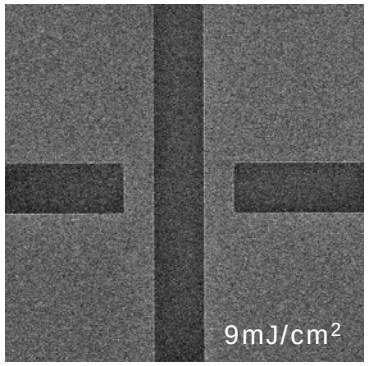
Medium Flare

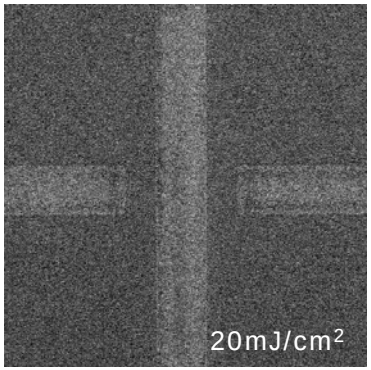


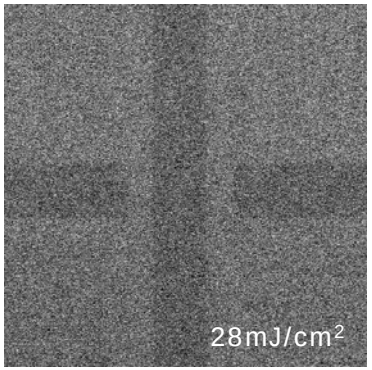
High Flare



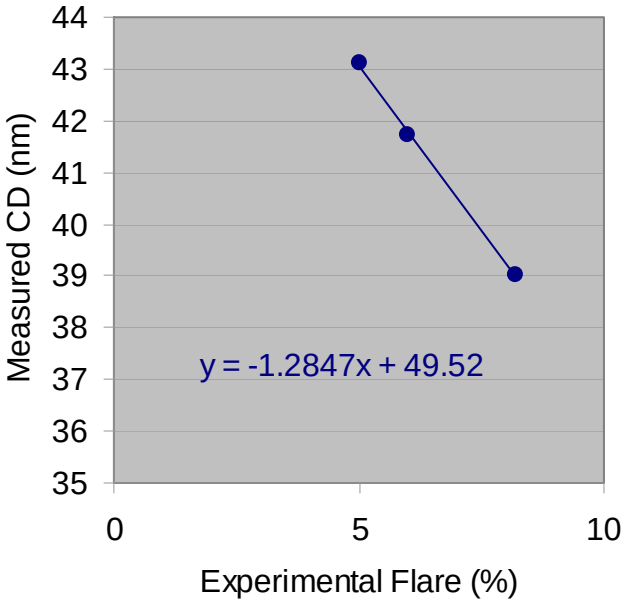








Flare measured using contrast-based flare metrology*



- ***Flare sensitivity ~ 1.3nm / %***

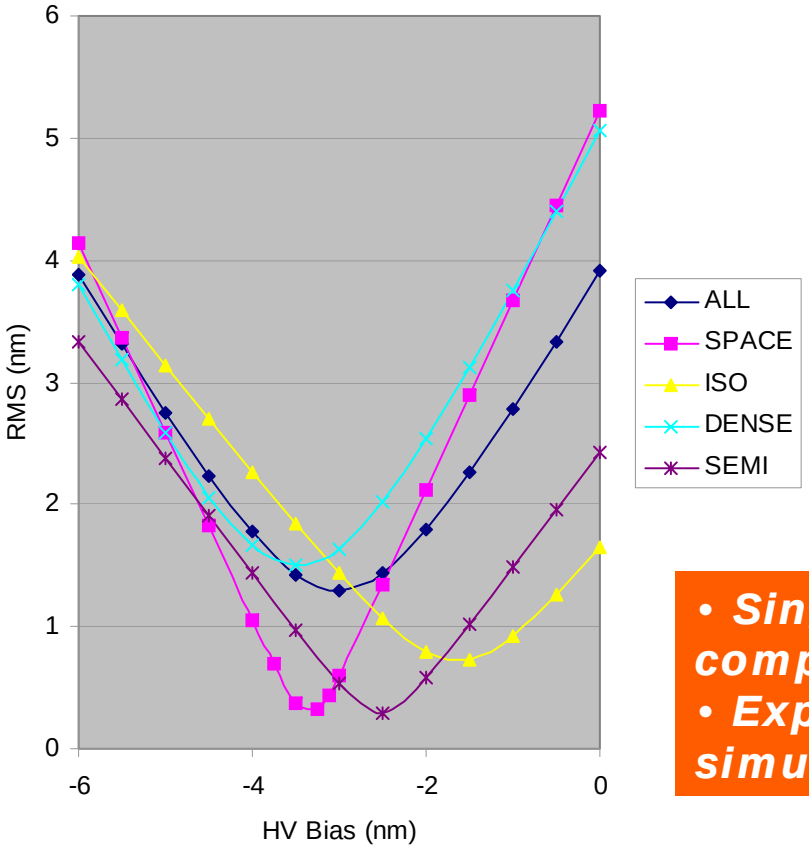
* GF Lorusso et al, "Flare in EUVL: Metrology, OoB, Fractal PSF, and Flare Map Calibration" JM3, in press

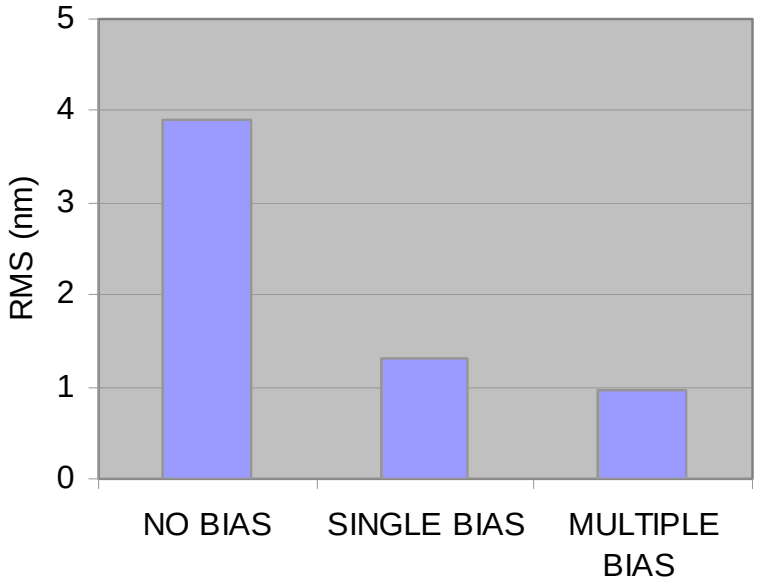
© imec 2009

OPC Model Calibration and Verification: Shadowing

$$RMS = \sqrt{\frac{1}{N}\sum_{1}^{N}(Bias@Wafer - HVBias \times MEEFH)^2}$$

Measured — Variable — Measured



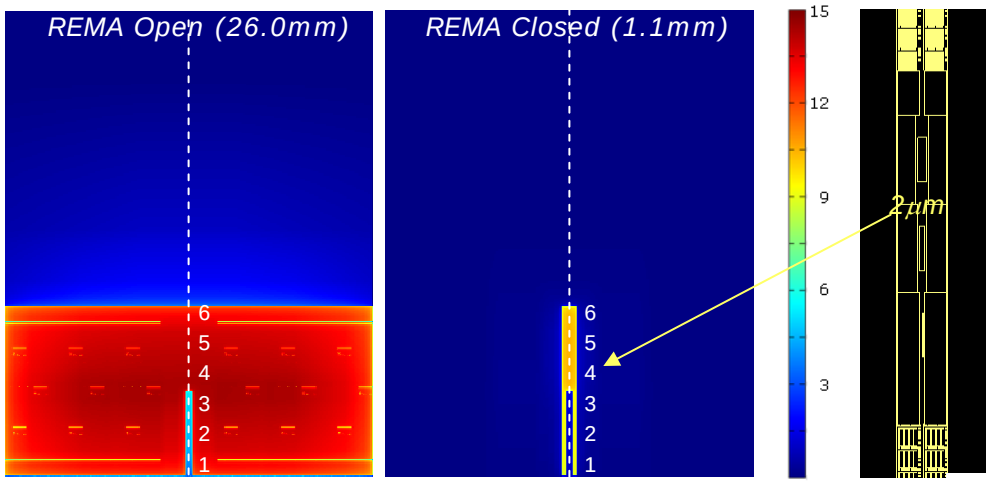


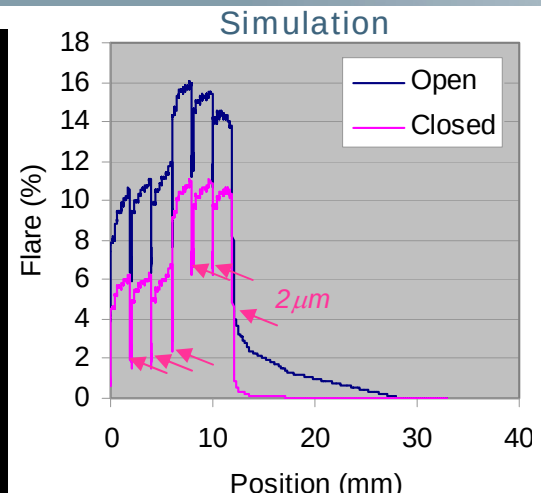
- *Single Bias = one bias for all feature type*
- *Analysis*
  - *Based on experimentally measured MEEF*
  - *Through Flare*

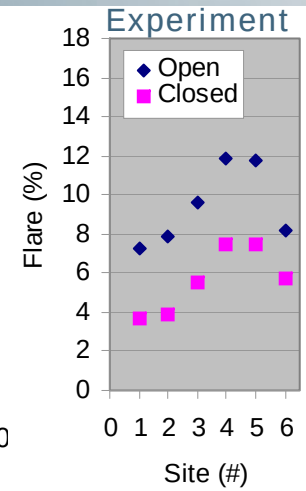
- ***Single bias correction effective to compensate shadowing for 1D features***
- ***Experimental analysis in agreement with simulations***

© imec 2009

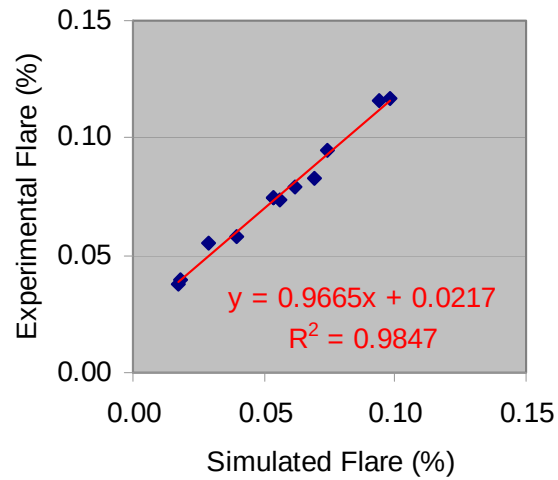
OPC Model Calibration and Verification: Flare Map Accuracy







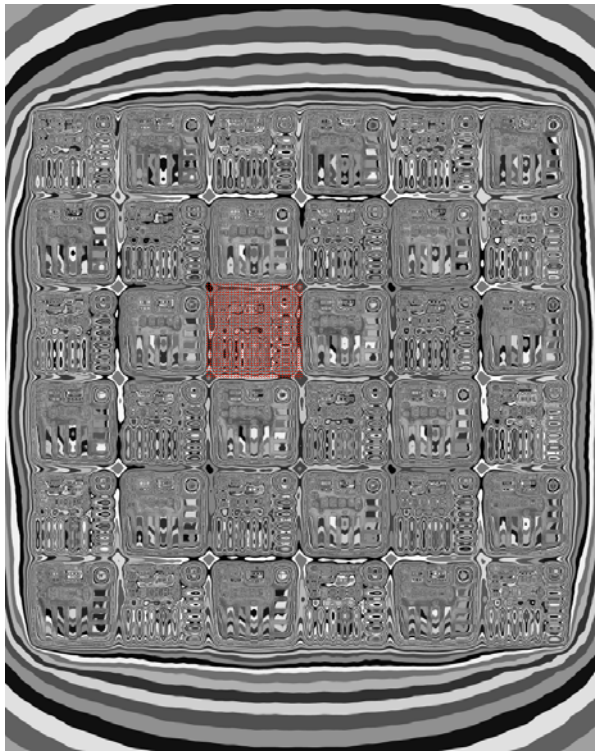
- *6 flare sites were measured with REMA blades closed and open on 2μm targets*
- *The 12 flare measurements (4-12% range) were compared to flare simulations to check accuracy*

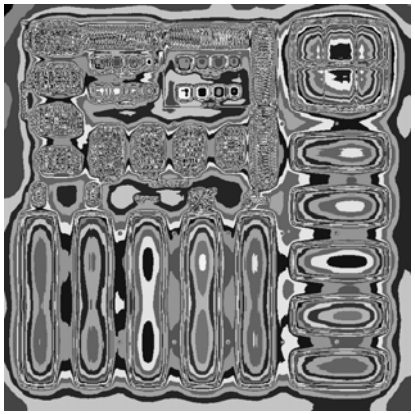


- ***The flare simulation agrees well with experimental flare data***
- ***A ~2% offset is observed, attributed to DUV***

OPC Model Calibration and Verification: Model Flow and RMS

- **Optical Model**
  - *NA = 0.25*
  - *σ = 0.50*
- **Resist Model**
  - *Simple Gaussian model*
- **Shadowing**
  - *Single bias rule-based correction*
  - *HV bias = 1.5nm/edge*
- **Flare**
  - *Flare map-based correction*
  - *Flare sensitivity = 1.3nm/% experimental*

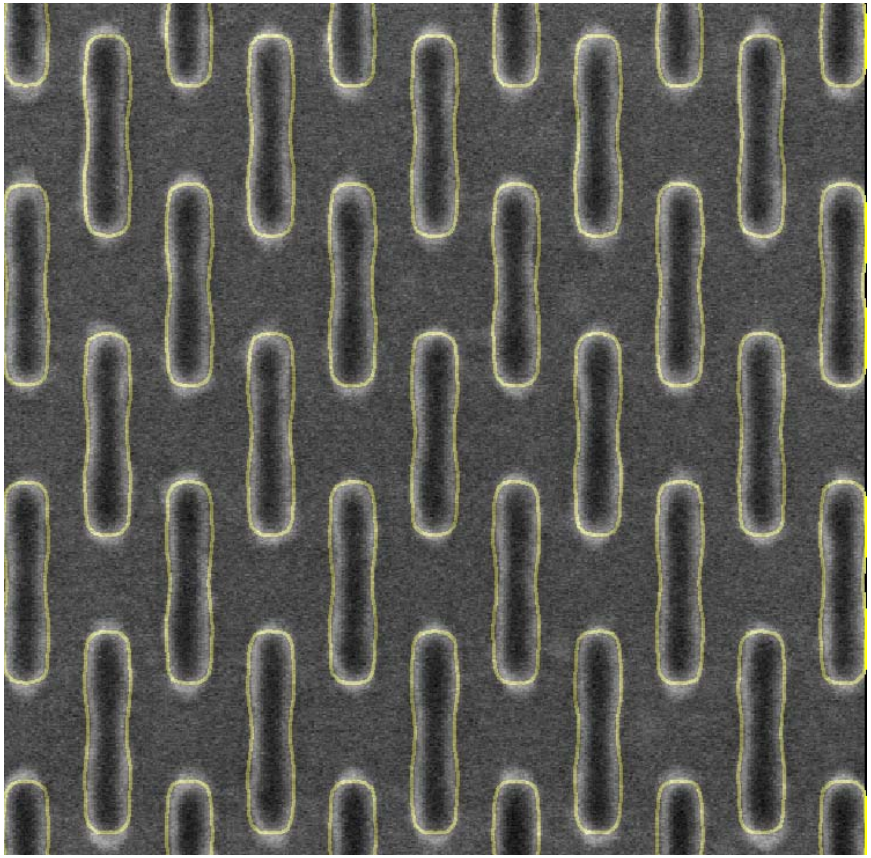


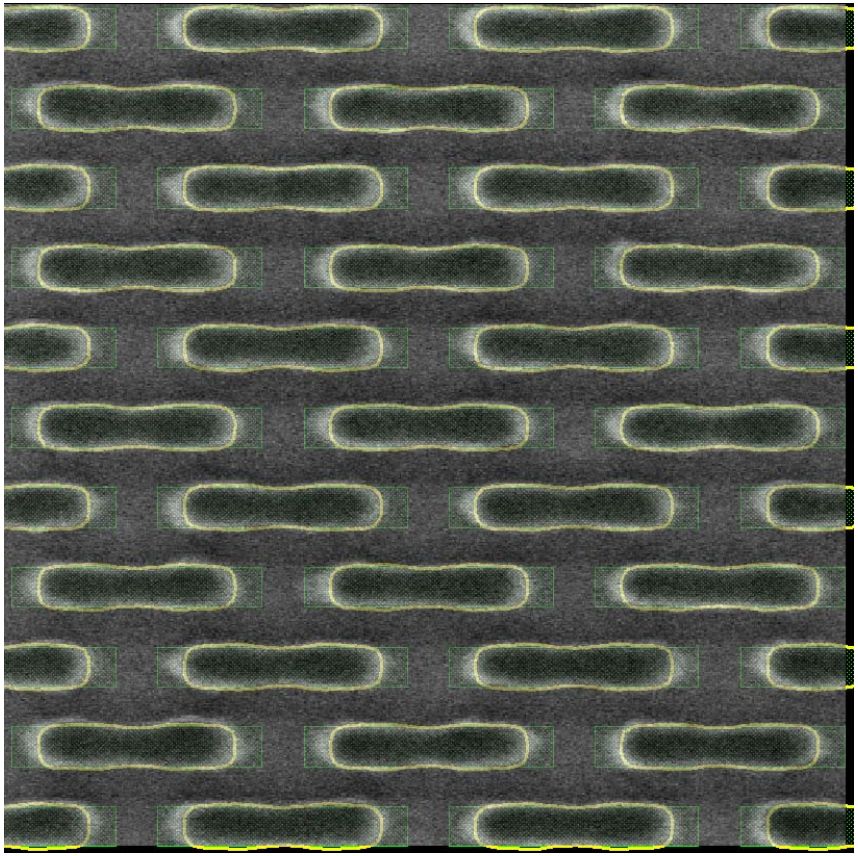


RMS 1D	RMS all	RMS L_Bar	RMS MEEF	RMS Space	RMS EOL
0.64nm	0.74nm	0.71nm	0.63nm	0.41nm	1.34nm

RMS ~ 1nm

OPC Model Calibration and Verification: 2D Model Verification – Brick Wall

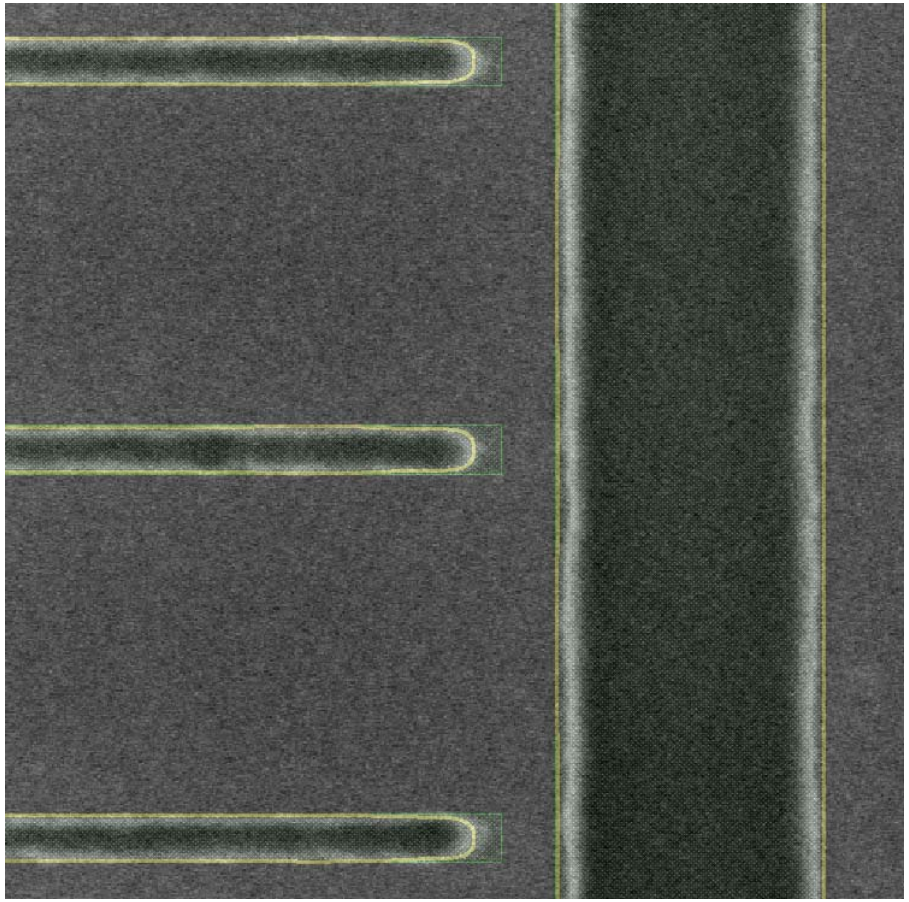


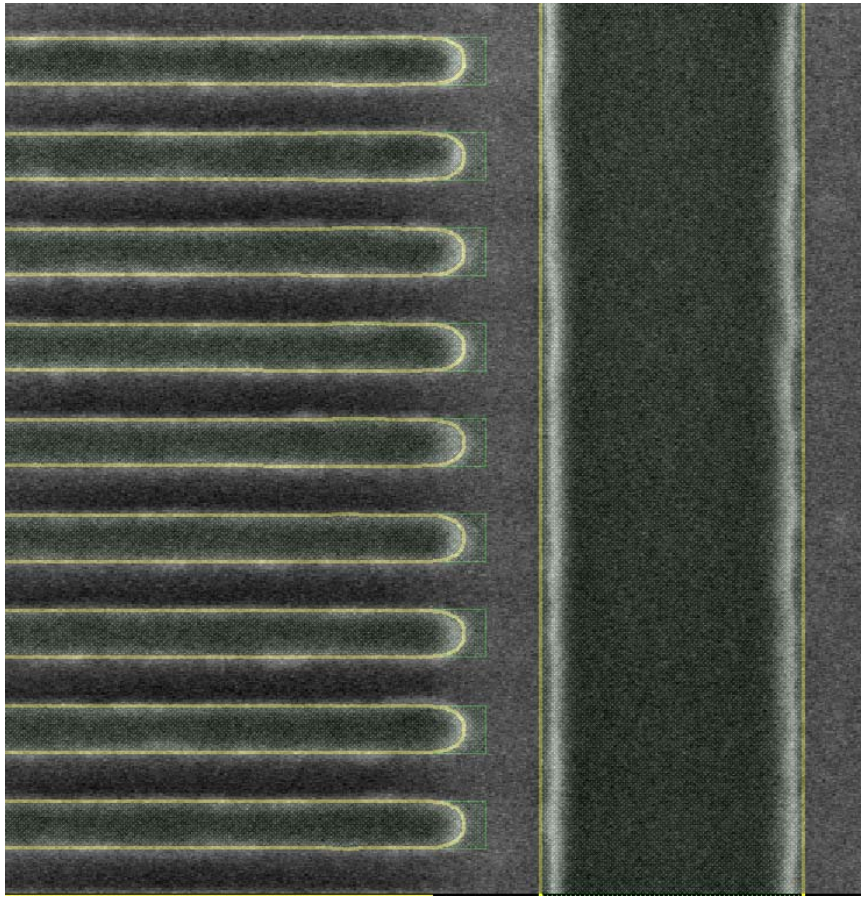


Accurate modeling of Brick Walls

Brick Wall 32nm

OPC Model Calibration and Verification: 2D Model Verification – T End-of-Line





Accurate modeling of T-End-of-Lines

© imec 2009

Conclusions

- **Full resist model**
  - The model was calibrated for ShinEtsu SEVR 59
  - The model accurately predicts **Bossung tilt** and **focus shift**
  - The model validation through flare, CD and pitch demonstrated an **RMS ~ 1nm**.
  - The error drops to **RMS ~ 0.3nm** by using dose, focus, shadowing and mask CD for 32nm DL.
- **OPC**
  - Our goal is to **test/build the OPC infrastructure** that need to be put in place before the introduction of EUVL in production
  - **High quality calibration and verification data sets** for CD and flare were generated
  - We demonstrated the ability to compute an **accurate flare map** require for EUV OPC
  - We demonstrated an **RMS ~ 1nm** in terms of CD for various 1D and 2D structures
  - Verification of **2D features** was successful

© imec 2009

Acknowledgements

- This work would not have been possible without the following contributions:
  - ASML ADT team at IMEC and Veldhoven
  - Philips for providing source support
  - TEL for providing track support
  - Hitachi for providing CD-SEM support
  - Resist vendors for providing resists
  - IMEC colleagues and IIAP partners for their contributions

© imec 2009

25 imec

Years of Making Technology Fly

intel Micron Panasonic ideas for life SAMSUNG tsmc ELPIDA hynix Semiconductor PSC NXP founded by Philips infineon SONY QUALCOMM ST