EUV lithography implementation on contact and metal interconnect level of a 22nm node 0.099 μm^2 6-T SRAM cell

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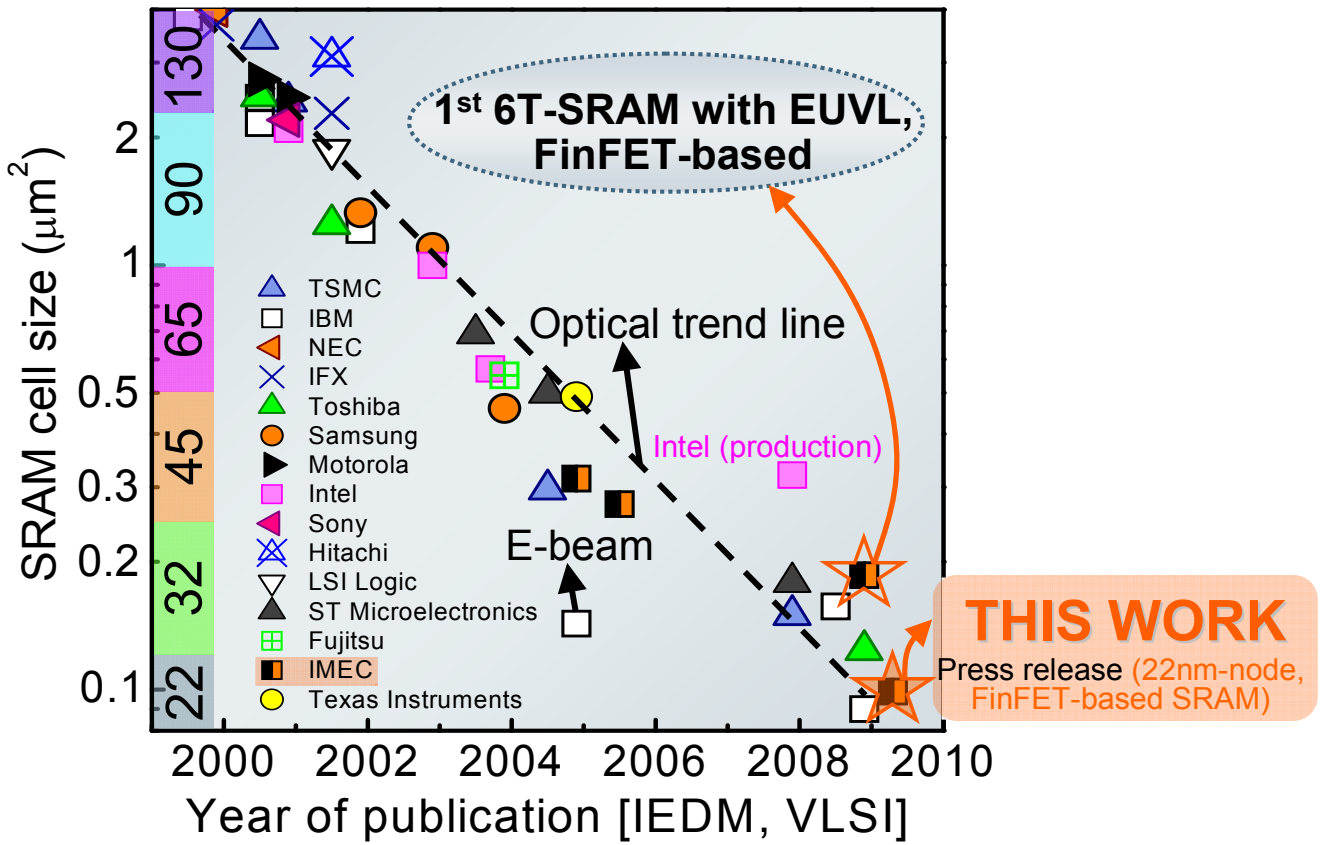
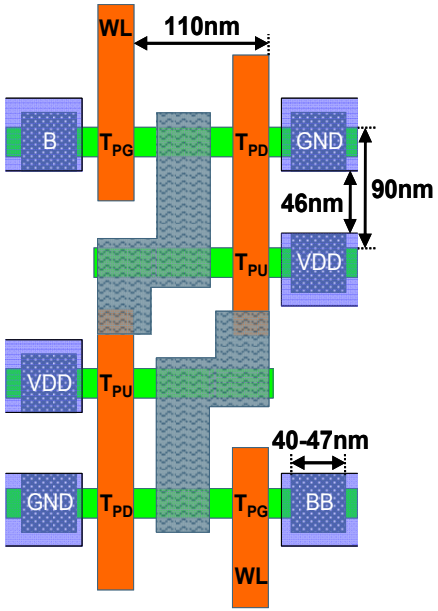
Introduction: Motivation

Feasibility demonstration of using full-field EUV lithography for contact hole and metal trench (M1) single-patterning in 22nm node, FinFET- based, 6T-SRAM



Introduction: 32nm → 22nm node SRAM with EUV

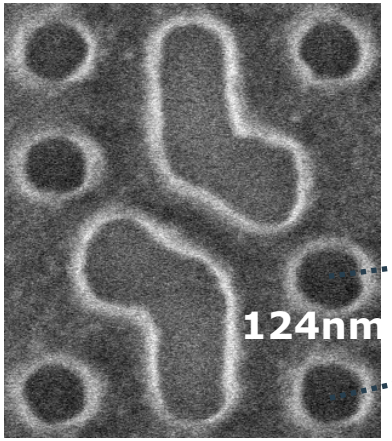
- Previous in 2008 : 32nm node SRAM
  - Implementation of EUV on contact hole level of a 32nm mode **0.186µm²** SRAM cells
- **<u>This work</u>** : Implementation of EUV on the contact hole and the metal level of **0.099µm² FinFET 6T-SRAM**



47% smaller SRAM area

0.186µm² → 0.099µm² SRAM

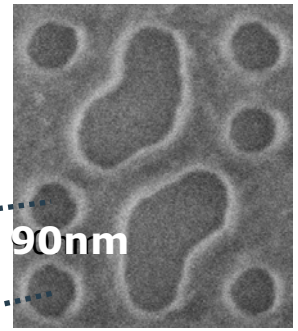
after CH EUV Litho



0.186µm² SRAM

27% Smaller CH pitch

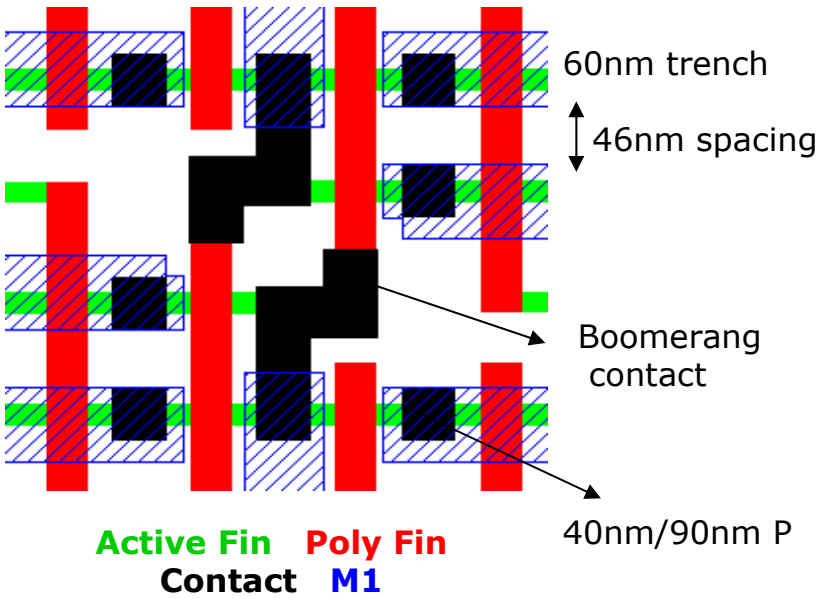
after CH EUV Litho



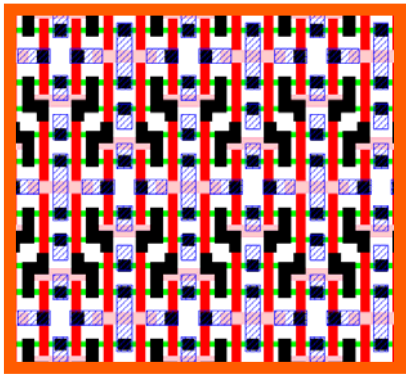
0.099µm² SRAM

Introduction: Target 0.099μm² SRAM cell layout

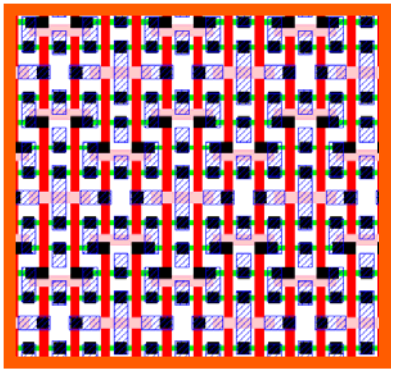
SRAM Cell Design



SRAM array
With boomerang at contact



SRAM array
With rectangular contact



Active, poly layers printed with 193nm immersion (ASML 1900i, NA=1.35)
Contact and metal printed on ASML EUV ADT NA=0.25, σ=0.5

Patterning requirements EUV:

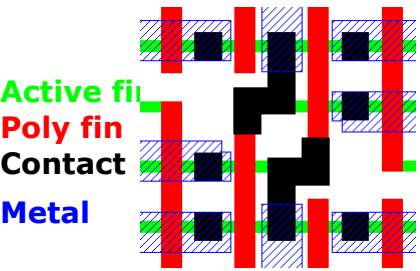
1) **40nm** contact holes & boomerang contact hole imaging on **90nm minimum pitch**
2) 60nm H and V trench with **46nm spacing at M1**

Outline

- Introduction
- ***Contact level patterning***
- Metal level patterning
- Summary
- Acknowledgements

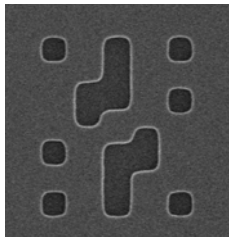
Contact level imaging

Design



Cell Size 0.099 μm^2

Reticle SEM

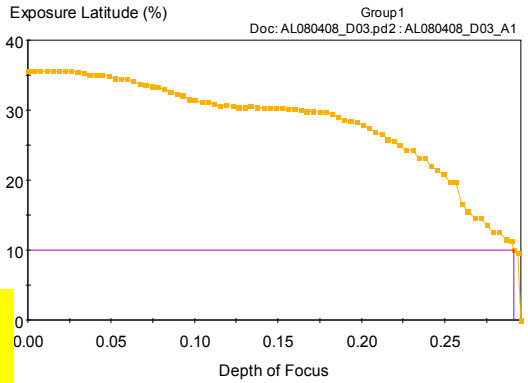


Simulated in resist

Image in resist ADT exposure

*80nm **Fuji FEVS-P1101***
SiOC/APF hard mask

Process window 40nm contacts



EL=35% and 300nm DOF

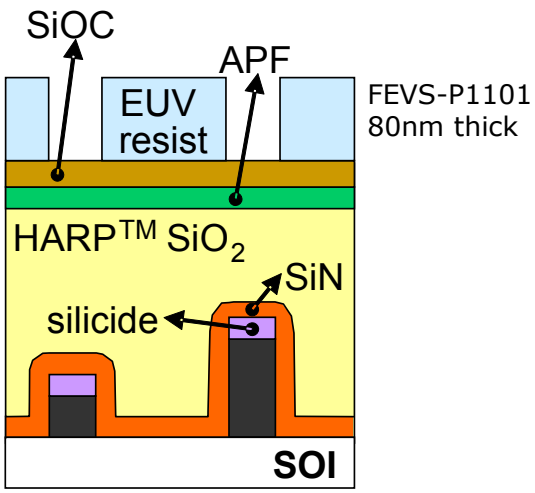
40nm contact through focus

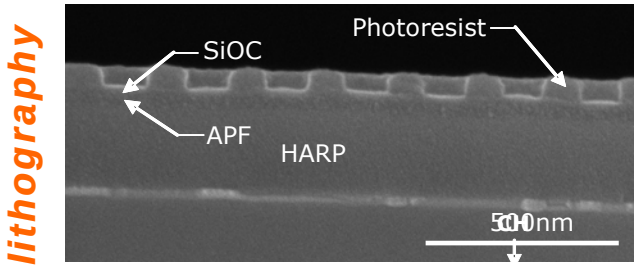
F=-100nm F=-50nm F=0 F=50nm F=100nm F=150nm F=200

ASML ADT EUV,
NA=0.25 PC=0.5
Fuji FEVS-P1101
80nm thick
E= 15 mJ/cm²

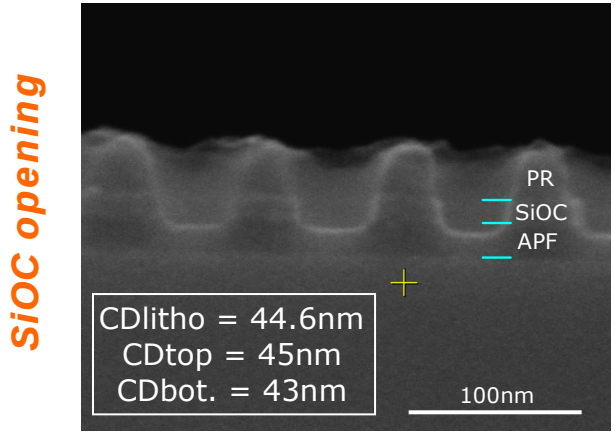
Large process window for 40nm contacts
Imaging challenge : simultaneous printing of round contacts and 'boomerang' shape

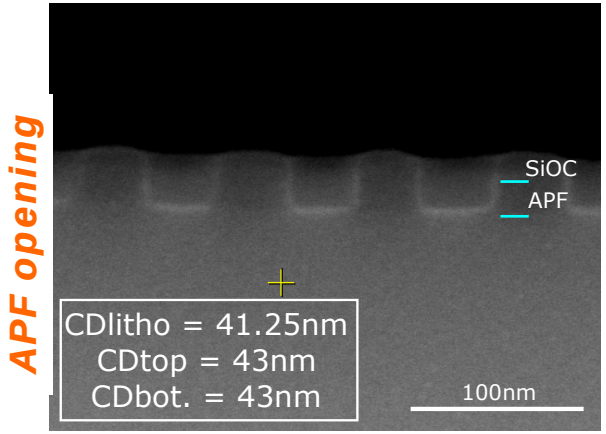
Etch process development for EUV contacts
Hard mask etch





Hard mask etch

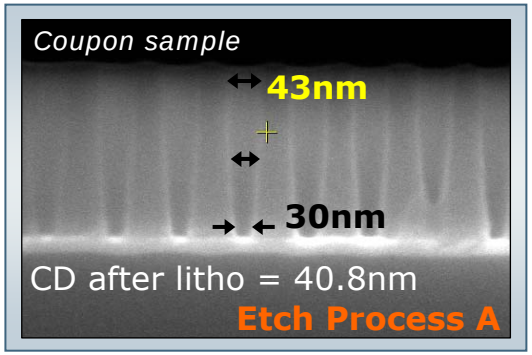


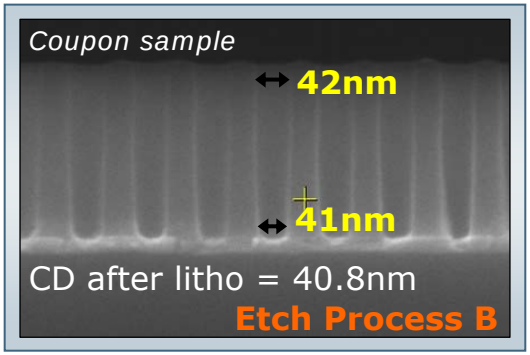


- Etch sequence
  - SiOC opening
  - APF opening
  - HARP Oxide etch
    (see next slide)

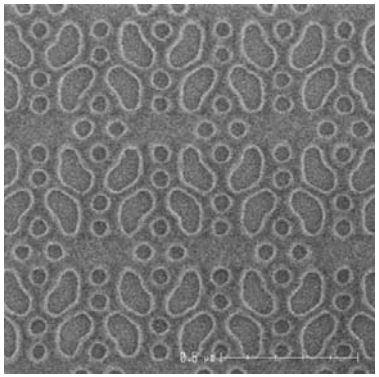
80nm resist thickness sufficient for hard mask opening
Straight APF profiles

Etch Process development for EUV Contacts Transfer in oxide layer (full stack etch)

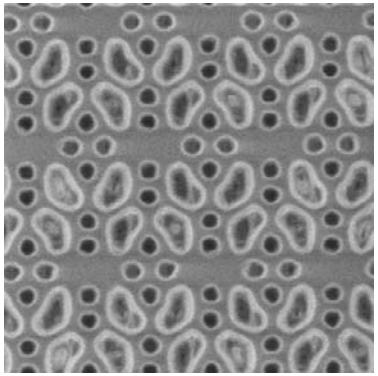


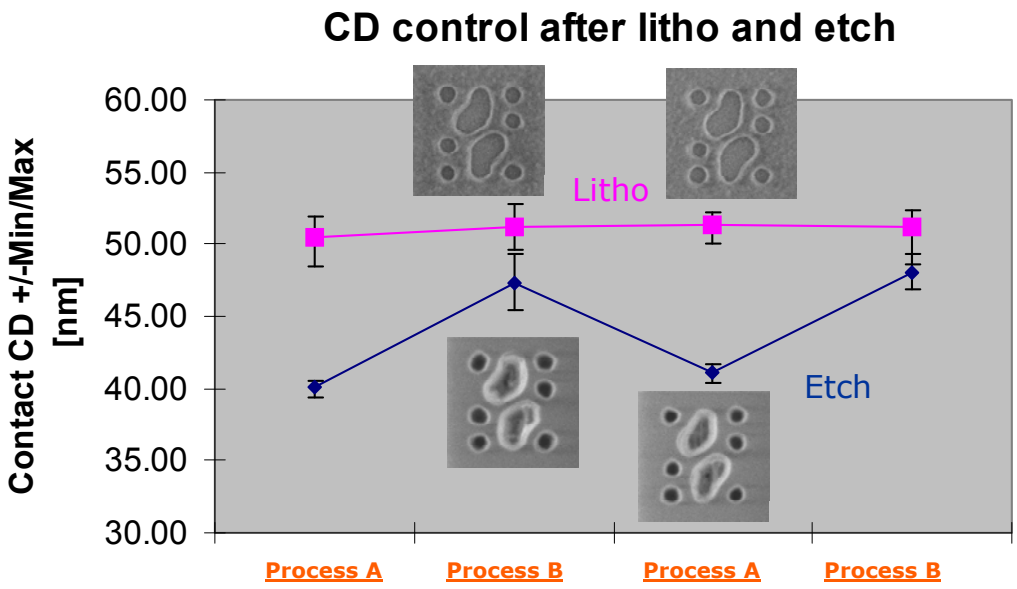


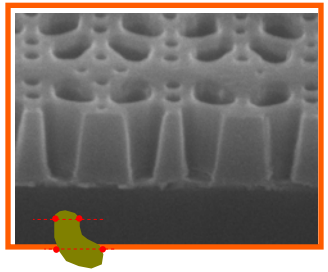
After litho



After etch







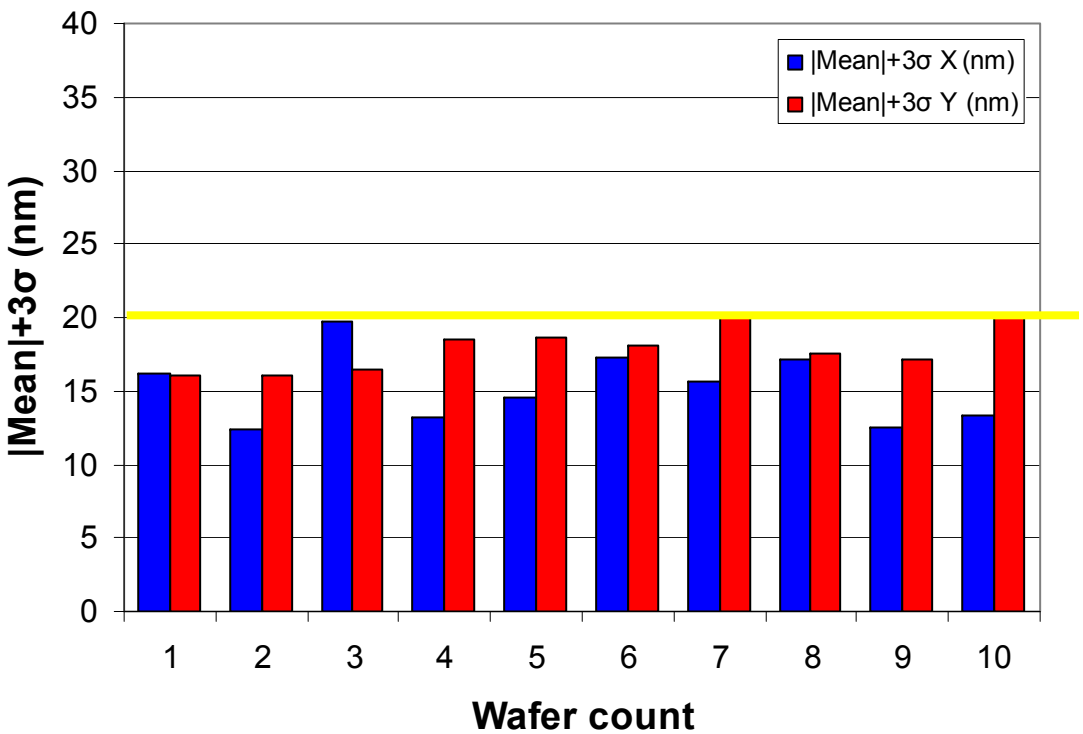
- Less litho etch bias for process B linked with straighter profile
- Significant slope on non-circular contact for both processes

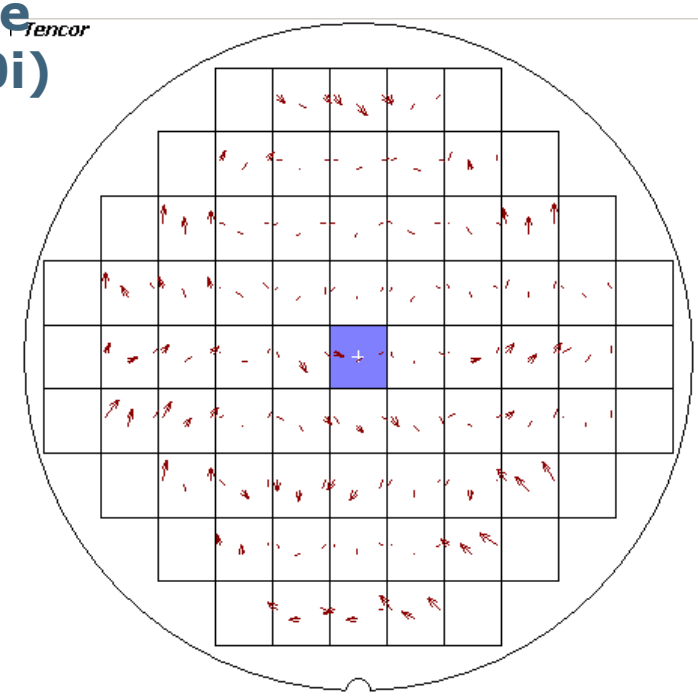
Overlay contact-to-active level ADT to 1900i

X: |Mean|+3σ: 14.8nm
Y: |Mean|+3σ: 17.3nm

Contact-to-active (ADT to XT:1900i)

Measured Overlay



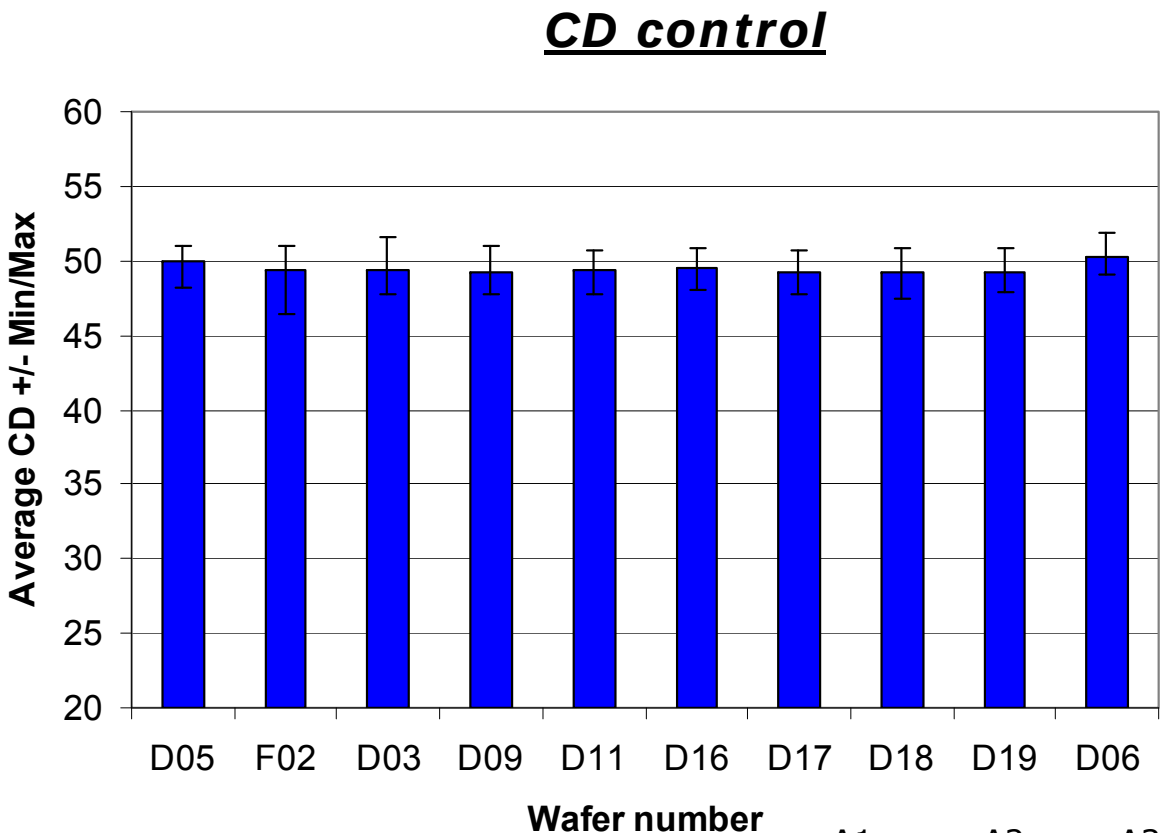


Wafer 9

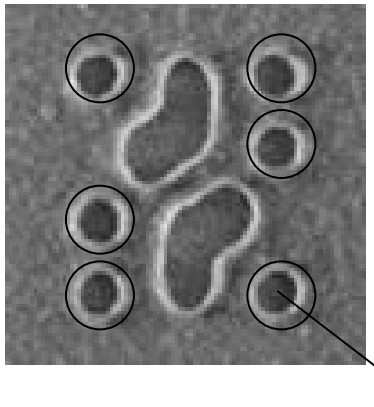
59 fields across wafer
Field size: 26mm x 5mm
3 points intrafield sampling
Avg. batch correctables removed

ADT to 1900i contact-active overlay is <20nm |Mean|+3σ is meeting the specification

22nm SRAM contact level pattering
CD control after litho

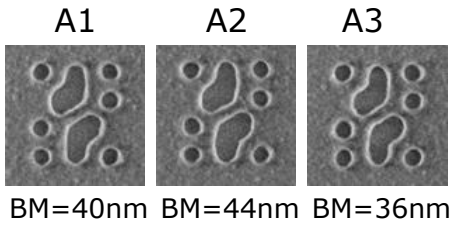


Picture after litho



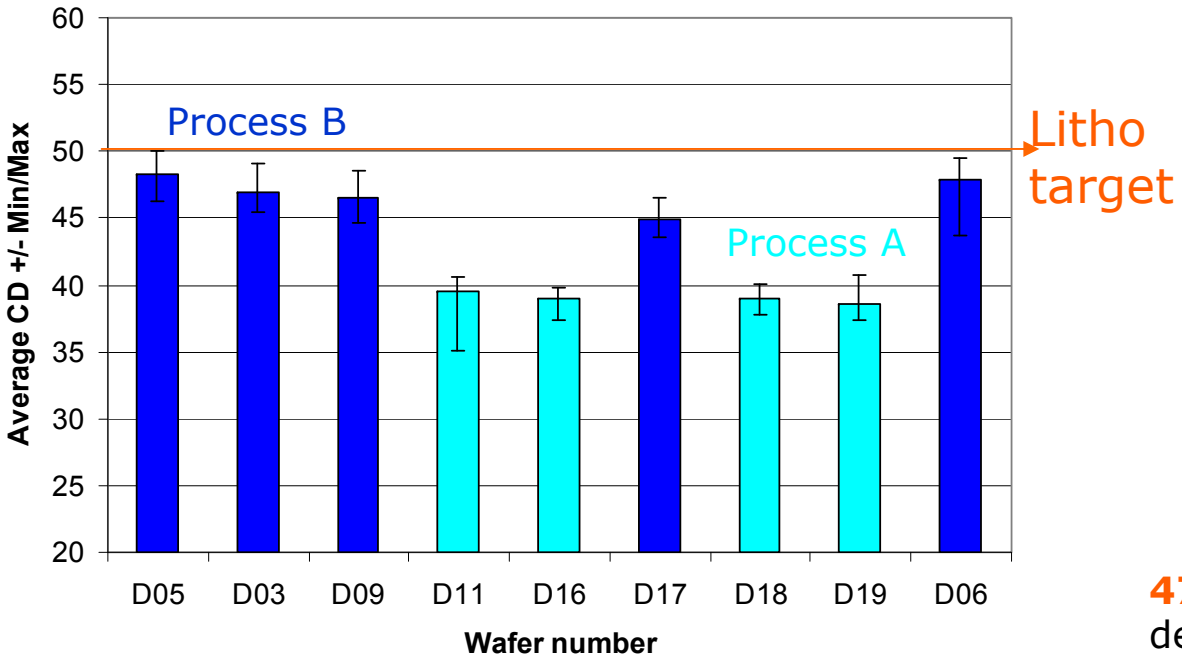
10 wafer lot
|Mean| = 49.4nm
3σ = 2.05nm
Total range = 5.1nm

Resist: Fuji FEVS-P1101
80nm thick, 14.5 mJ/cm2
59 fields across wafer
*3*34 points wafer sampling*

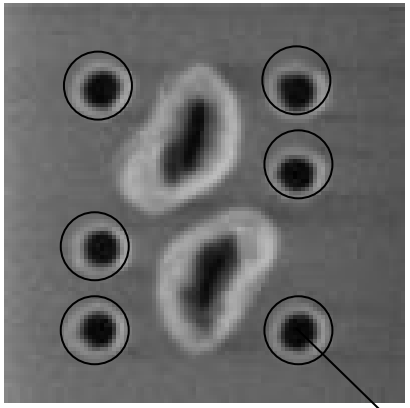


- Good CD control within wafer and within batch

22nm SRAM contact level : CD stability after etch
Split in etch processes



Picture after etch



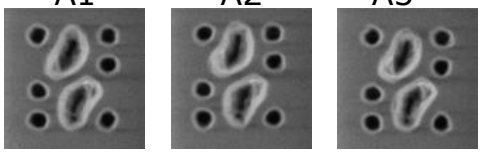
6 CH Avg. CD

47nm or 39nm etched contact
depending on etch process used
(design 44nm, 50nm after litho)

4 wafer lot: etch process A
Avg. CD =39.01 nm
3σ =1.93 nm

5 wafer lot: etch Process B
Avg. CD =46.92 nm
3σ = 4.14nm

A1 A2 A3

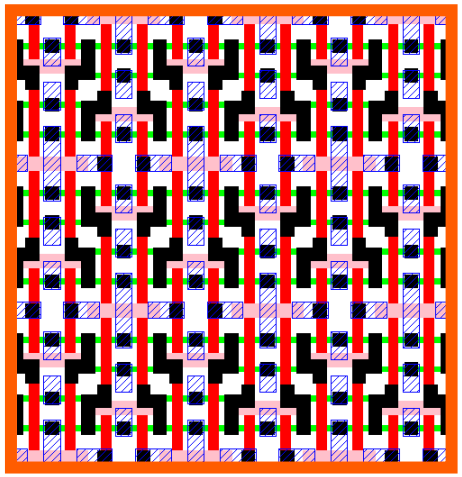


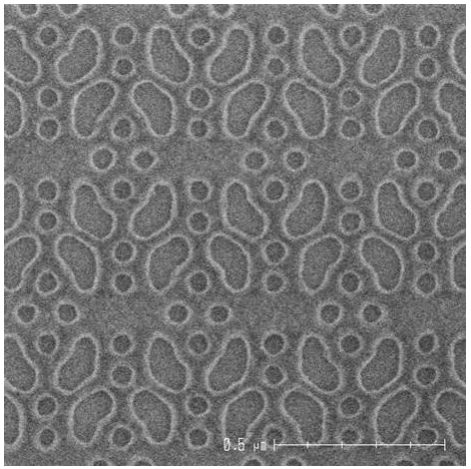
59 fields across wafer
Field size: 26mm x 5mm
*3*34 points wafer sampling*

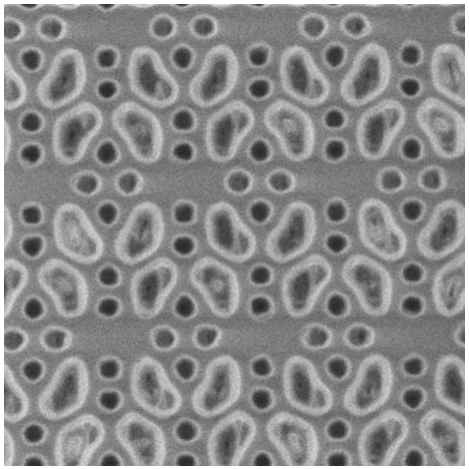
2 different etch processes with different CD bias and profiles applied
Good CD control after etch

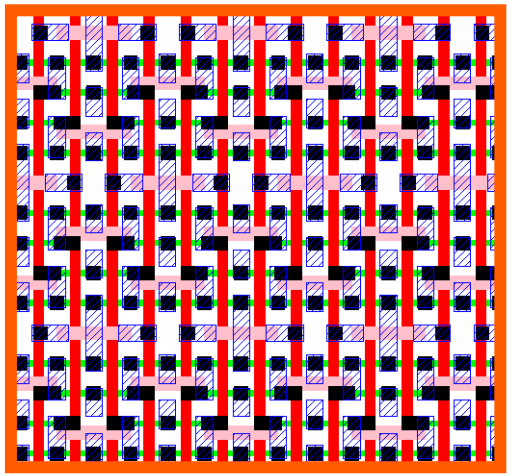
22nm node SRAM array
Contact hole imaging and etch

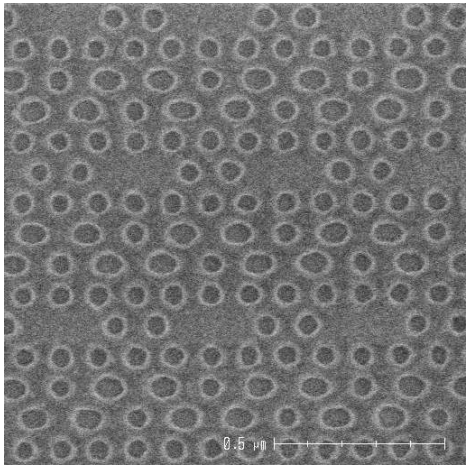
Design | **Image in resist** | **Image After etch**

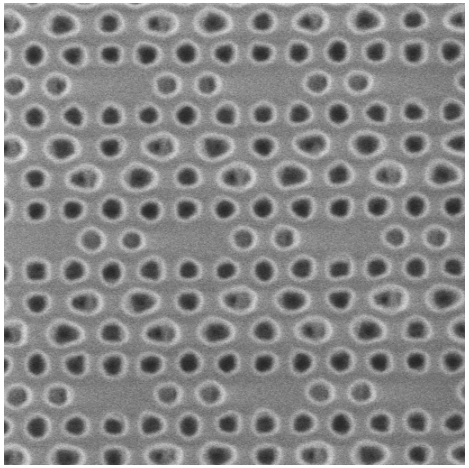






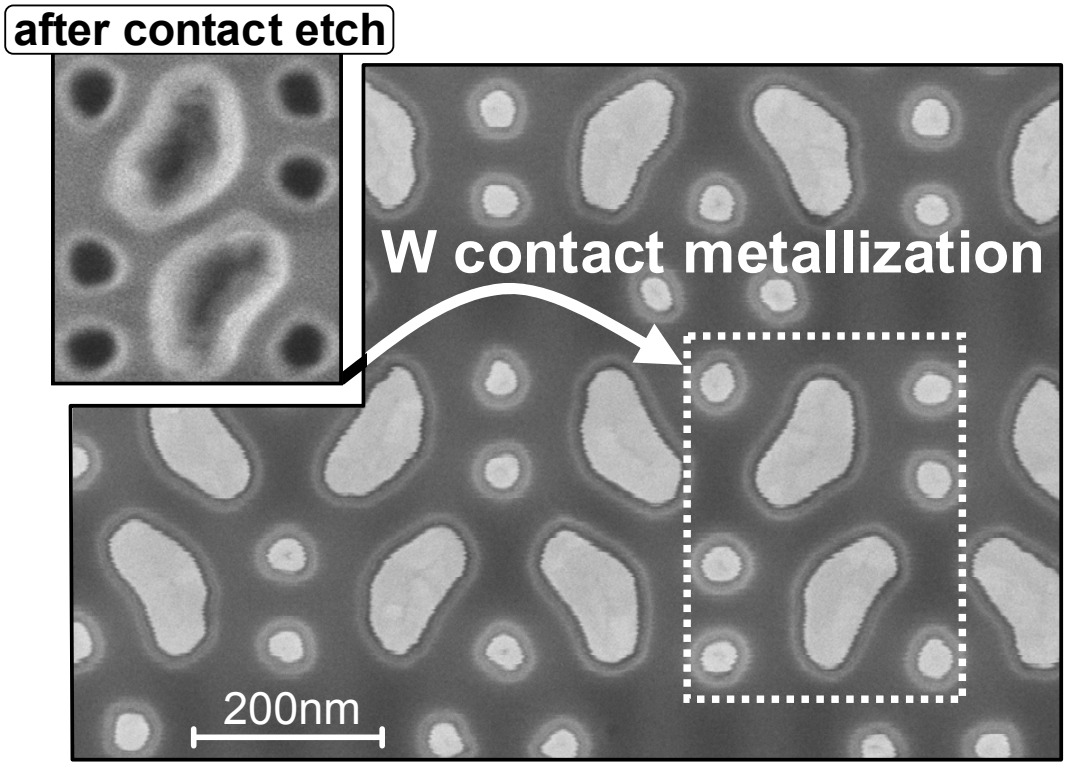


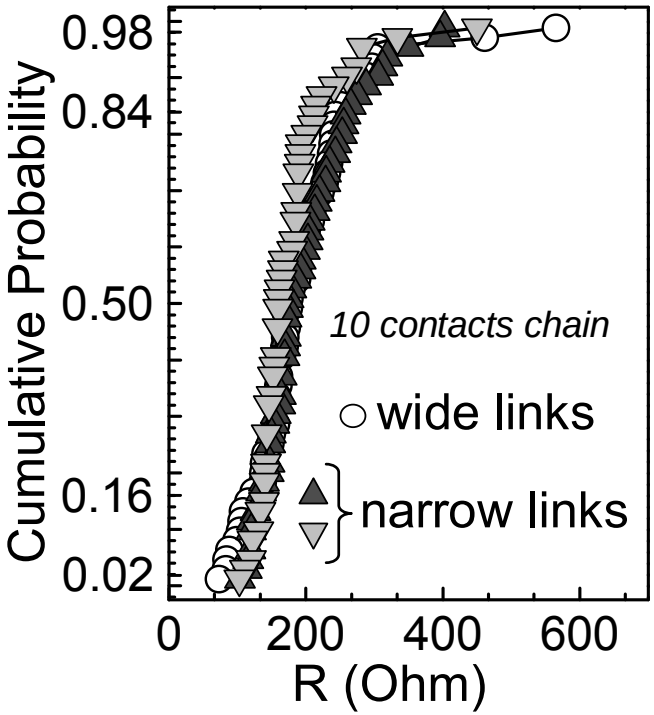




ASML ADT EUV, NA=0.25 PC=0.5
Resist Fuji FEVS-P1101, 80nm thick

22nm SRAM processing: contact metallization





- Optimized W metallization was used to fill the high aspect-ratio contact holes without voids

Outline

- Introduction
- Contact level patterning
- ***Metal level patterning***
- Summary
- Acknowledgements

Metal level Imaging

Design

Active fin
Poly fin
Contact
Metal

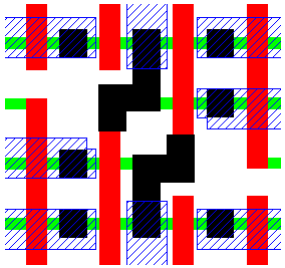
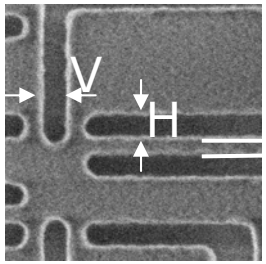


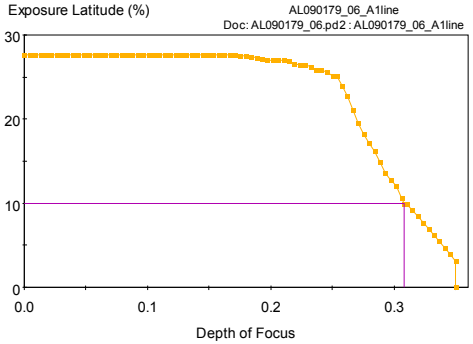
Image in resist ADT exposure



Space=46nm

*100nm **Fuji FEVS-P1101***
On 20nm Brewer BSI.X07333
(for TiN compatibility)
TiN hard mask

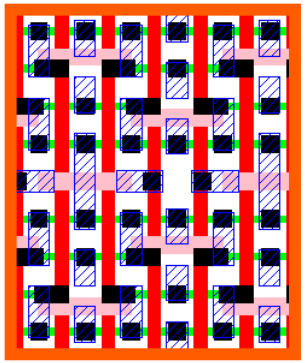
Process window 46nm spacing



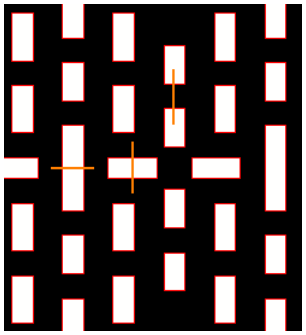
EL=27% and >300 DOF

Patterning challenge : preserve the 46nm spacing after etch

SRAM array



Mask design metal level



Simulation in resist

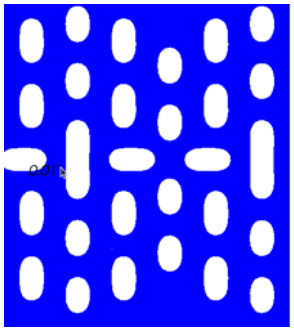
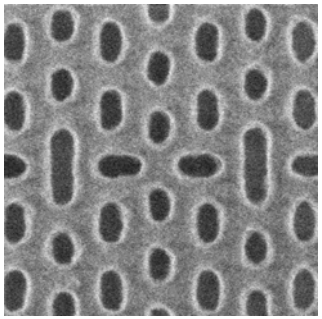


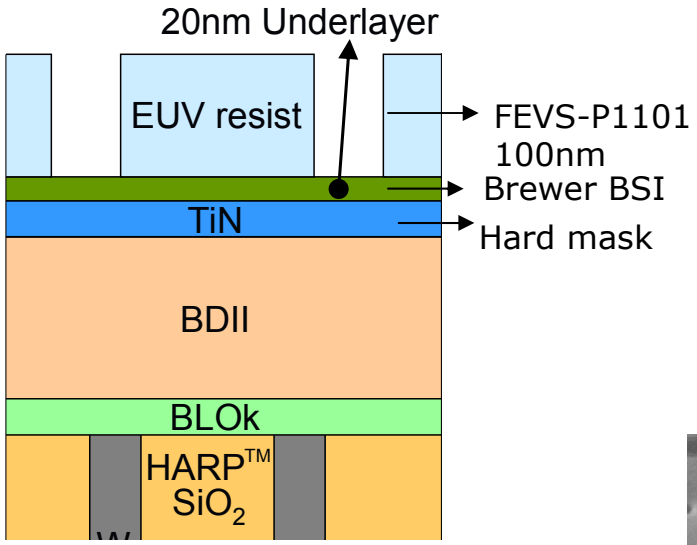
Image in resist ADT exposure

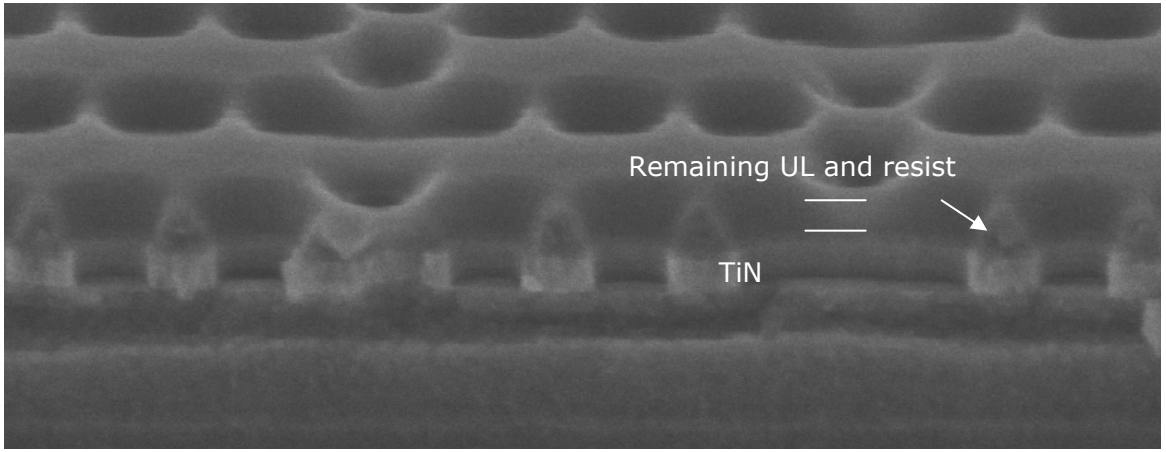


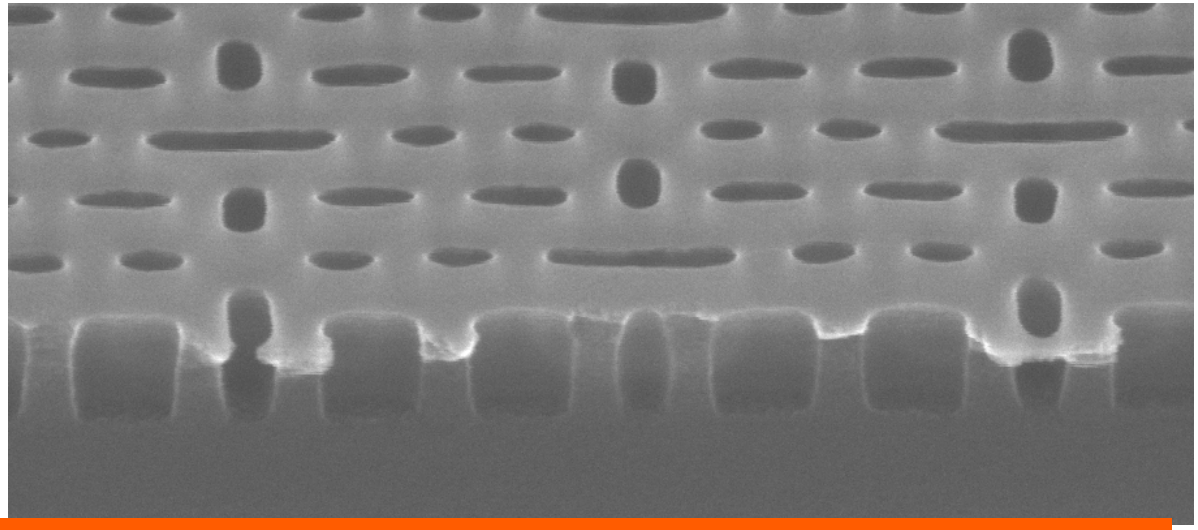
ASML ADT EUV,
NA=0.25 σ=0.5
Fuji FEVS-P1101
100nm thick
E= 13.4 mJ/cm^2

Simulation S-litho EUV

Patterning of metal 1 level of SRAM array
X-section after underlayer etch and TiN Hard Mask etch and after BDII etch





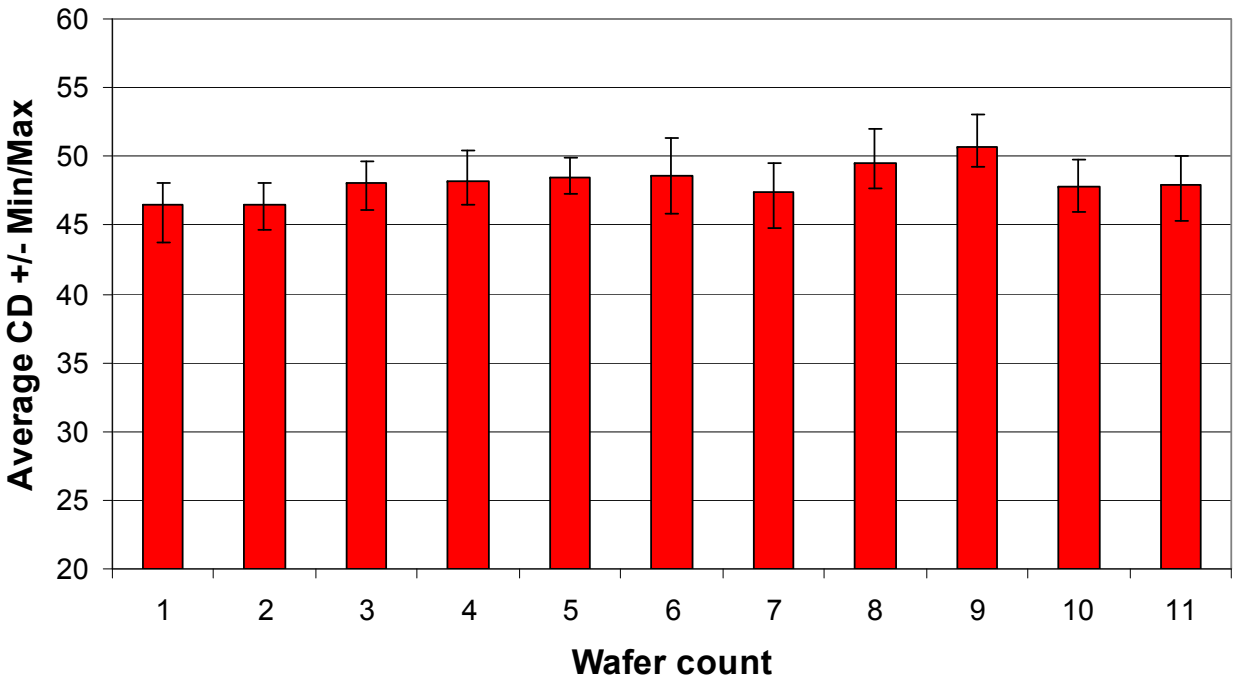


- Etch sequence
  - **Underlayer etch**
  - **TiN etch**
  - **Resist strip**
  - BDII and BLOK etch

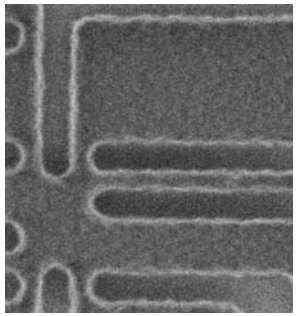
Resist has sufficient etch resistance to pattern the TiN hard mask
Good pattern transfer into BDII

22nm SRAM metal trench patterning CD control after litho

CD control of spacing



Picture after litho



46nm spacing

11 wafer lot
|Mean| = 48.1nm
3σ = 4.7nm
Total range = 9.2nm

Resist: Fuji FEVS-P1101
Dose=10.6 mJ/cm²
59 fields across wafer
Field size: 26mm x 5mm
34 points wafer sampling

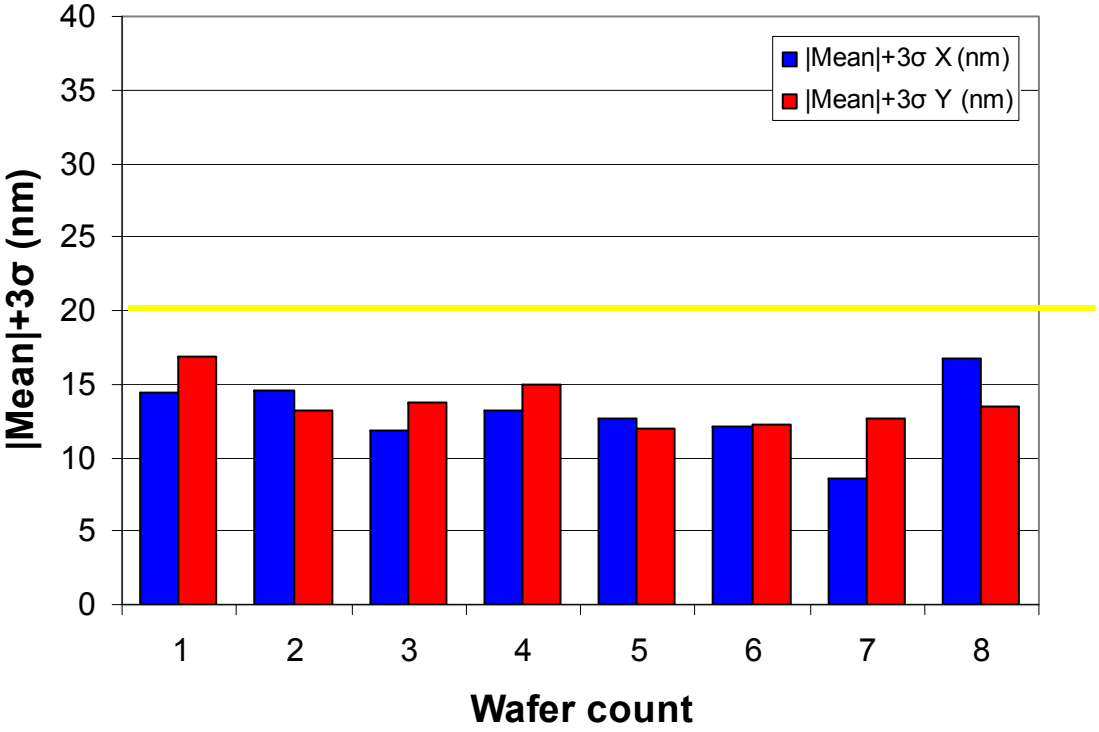
Good CD control within wafer (3σ 2-3nm) and over the batch

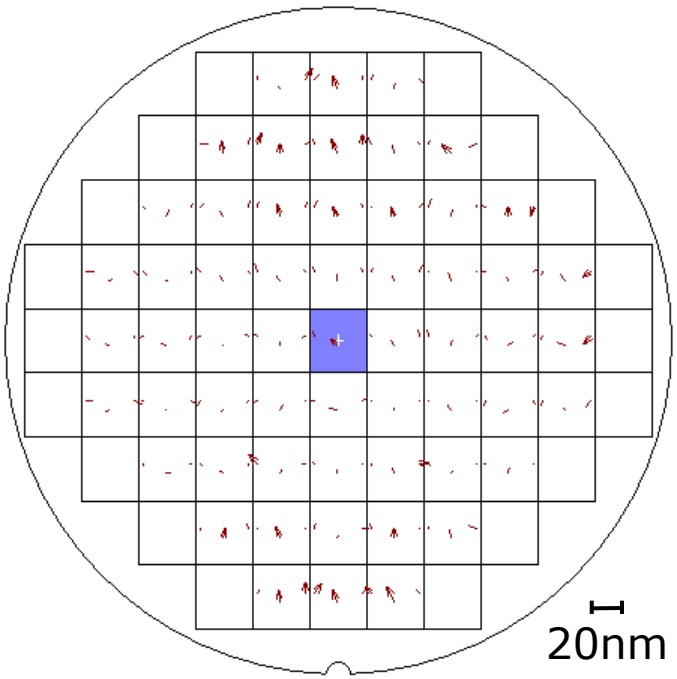
Overlay Metal-to-contact level ADT to ADT

X: |Mean|+3σ: 12.9nm
Y: |Mean|+3σ: 14.9nm

Metal to contact (ADT to ADT)

Measured Overlay



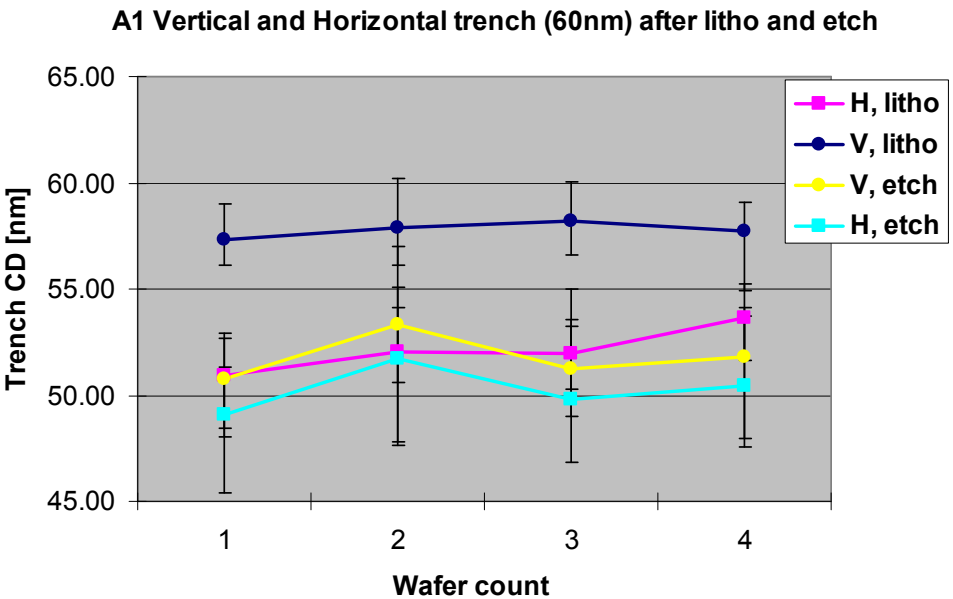


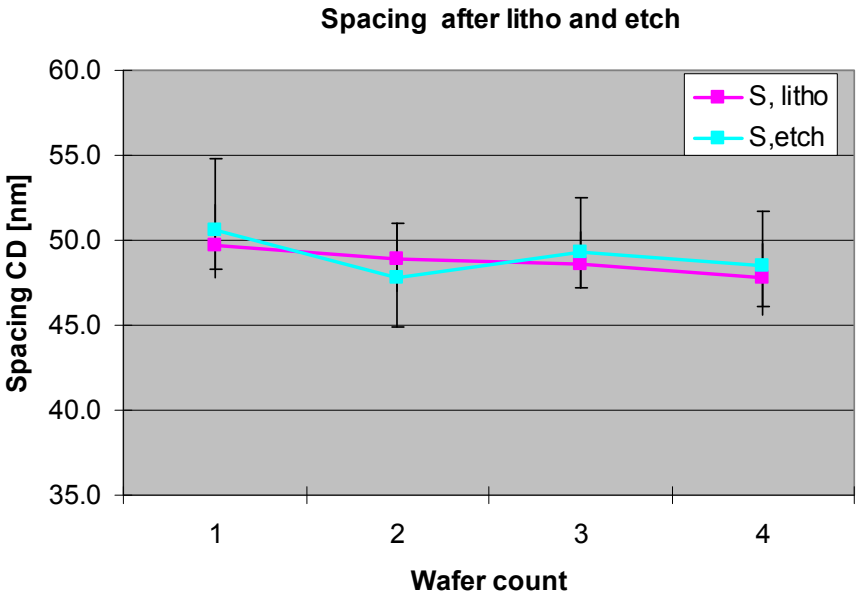
Wafer 7

59 fields across wafer
Field size: 26mm x 5mm
3 points intrafield sampling
Avg. batch correctables removed

ADT to ADT metal-contact overlay is <15nm |Mean|+3σ

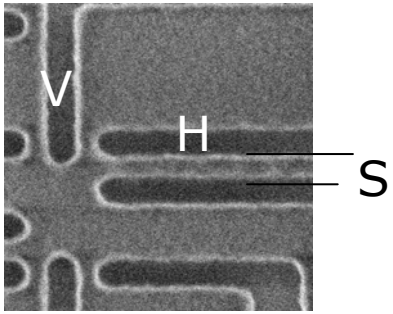
22nm SRAM Metal level pattering
CD control after litho and after etch (0.099µm^2 cell)

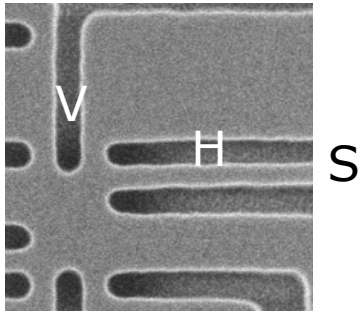




Litho 4-wafer lot

V trench = 57.77nm
2.7nm (3σ)
H trench = 52.14nm
4.1nm (3σ)
spacing = 48.75nm
3.6nm (3σ)





Etch 4-wafer lot

V trench = 51.79nm
5.2nm (3σ)
H trench = 50.26nm
5.3nm (3σ)
Spacing = 49.04nm
5.2nm (3σ)

Good CD control after etch
HV bias of 5nm on trenches due to shadowing effect (litho)
Spacing is well preserved after etch (0 nm litho-etch bias)

22nm node SRAM array metal patterning 0.099μm² array

Design

At metal level
50nm trenches

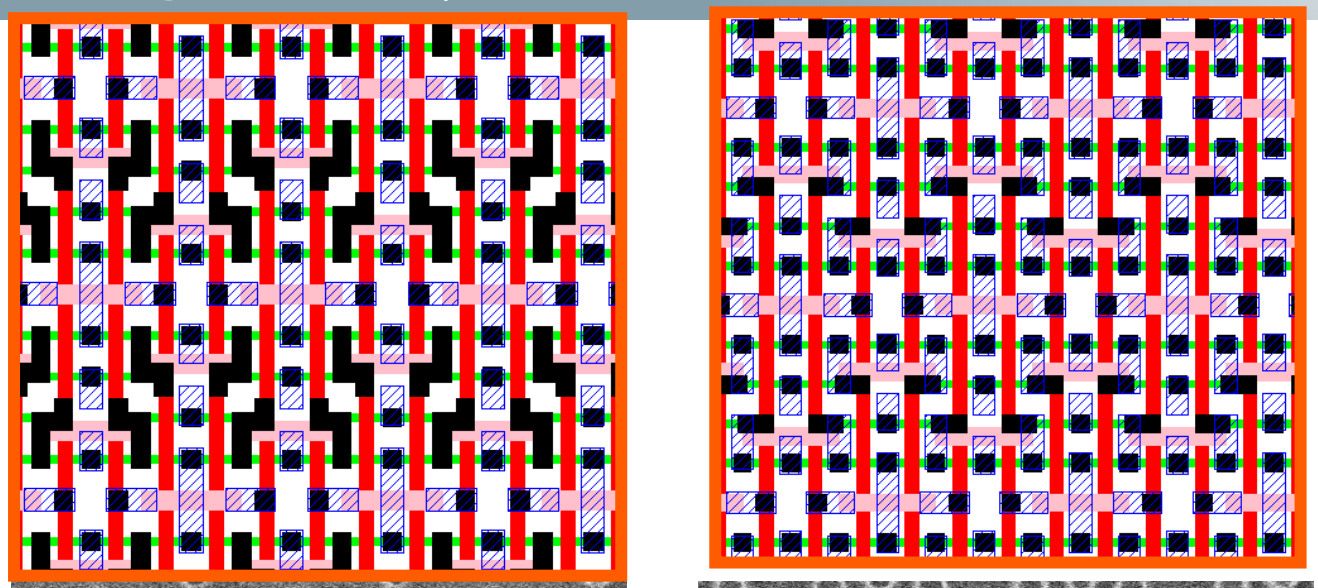
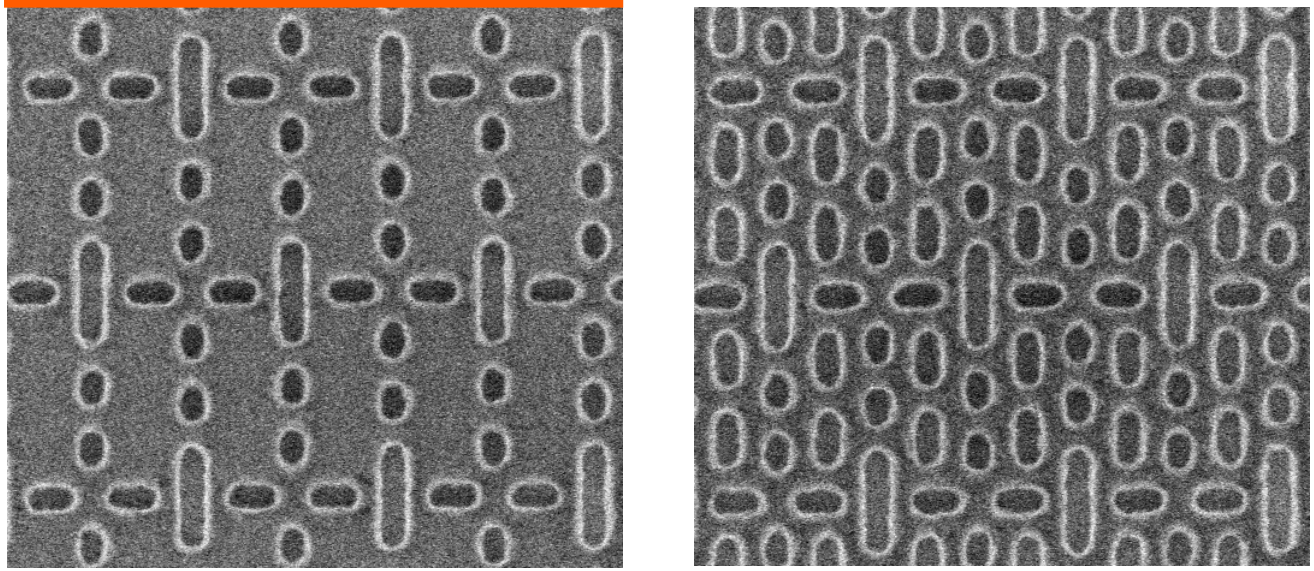


Image in resist



ASML ADT EUV, NA=0.25 PC=0.5
Resist Fuji FEVS-P1101, 100nm thick
On 20nm BSI X07333
E= 10.6 mJ/cm²

Metal level : SRAM array device patterning
0.099μm² array after litho and etch

Image in resist
ADT exposure

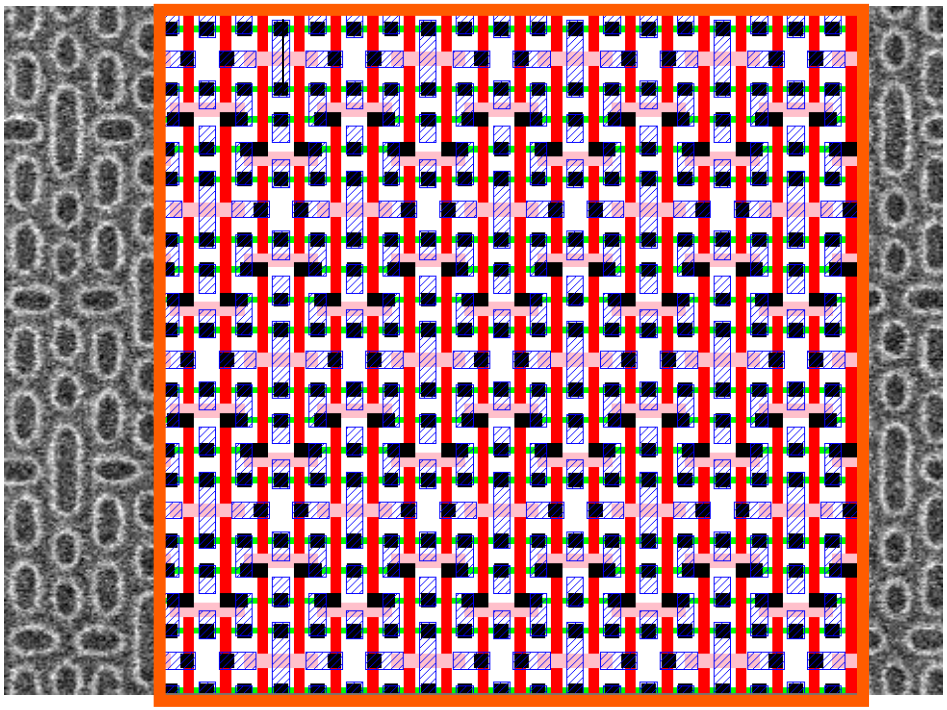
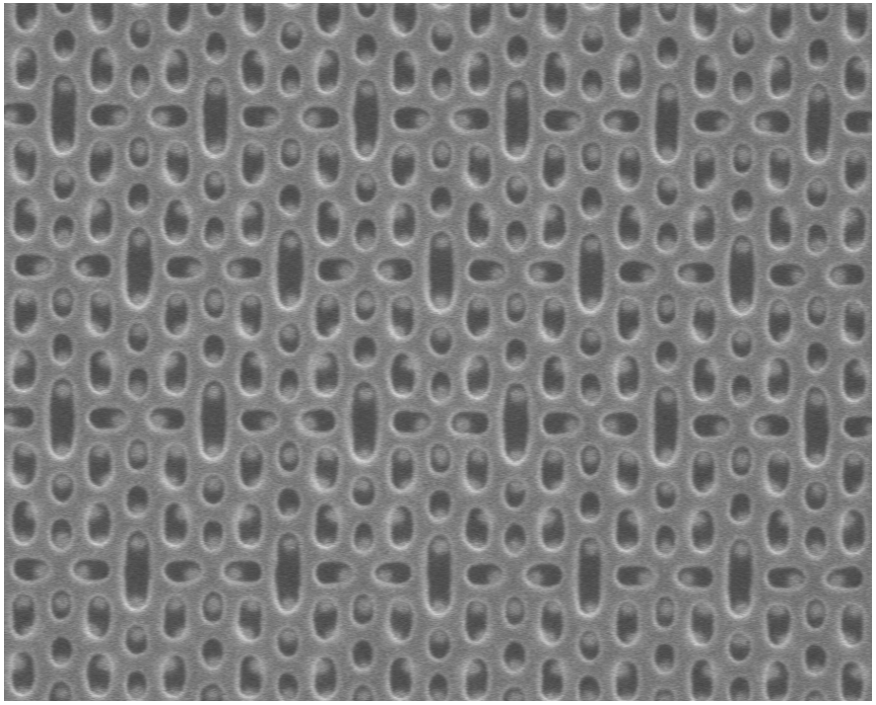


Image After etch

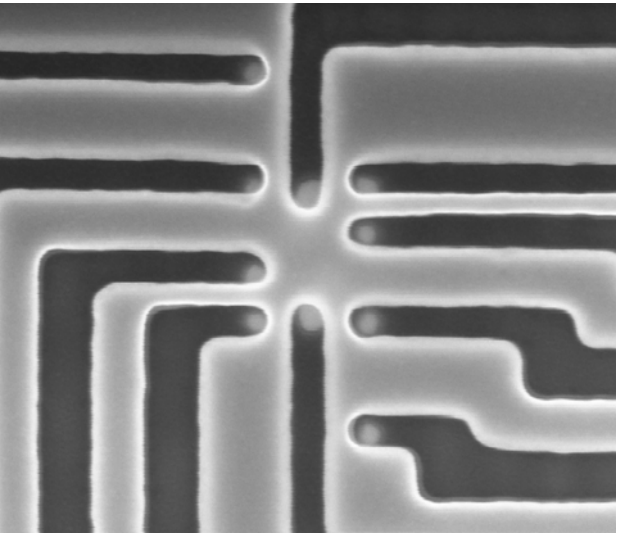


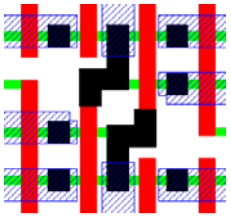
ASML ADT EUV, NA=0.25 PC=0.5
Resist Fuji FEVS-P1101,100nm thick
On 20nm underlayer BSI

Successful metal array patterning on devices batch
Good overlay demonstrated

Metal level SRAM device patterning patterning for 0.079μm² SRAM

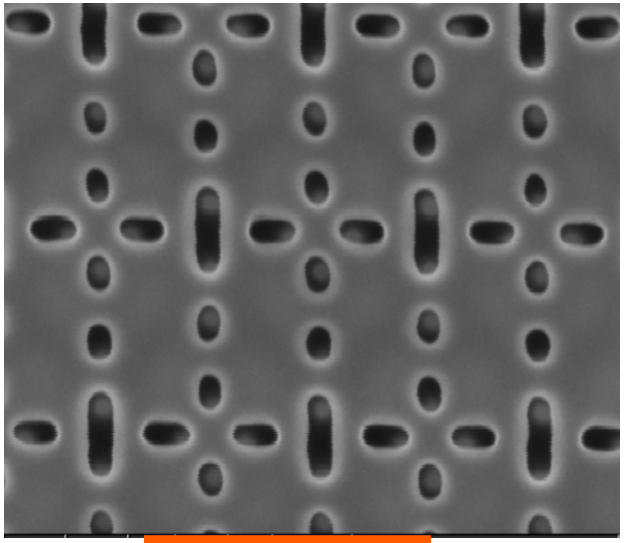
S-RAM cell

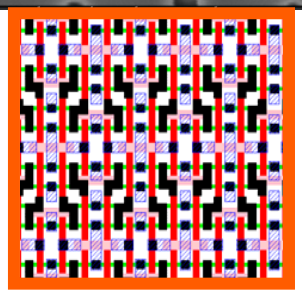




42nm spacing

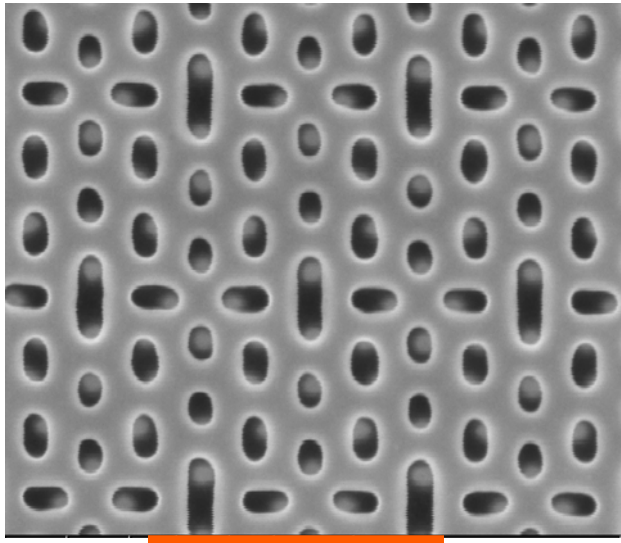
SRAM array
With boomerang at contact

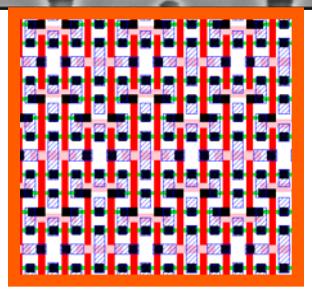




44nm trenches

SRAM array
Rectangular contacts

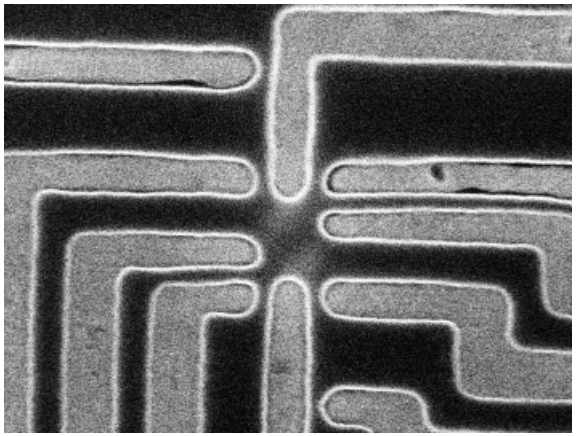




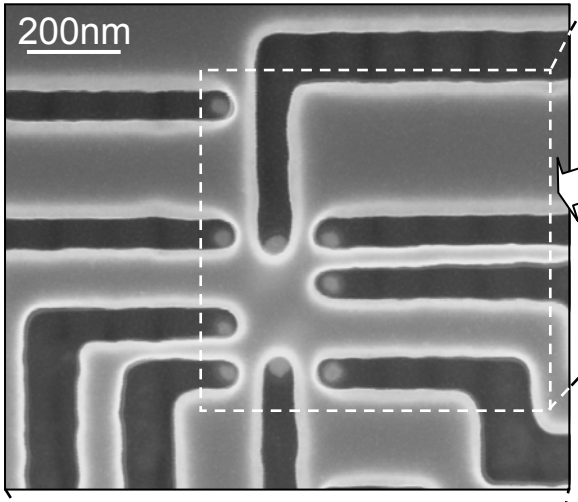
Good patterning results also on 0.079μm² SRAM array processed with Fuji FEVS-P1101

22nm SRAM further processing 0.099μm² cell

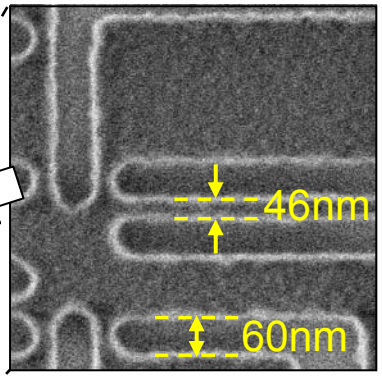
after M1 CMP

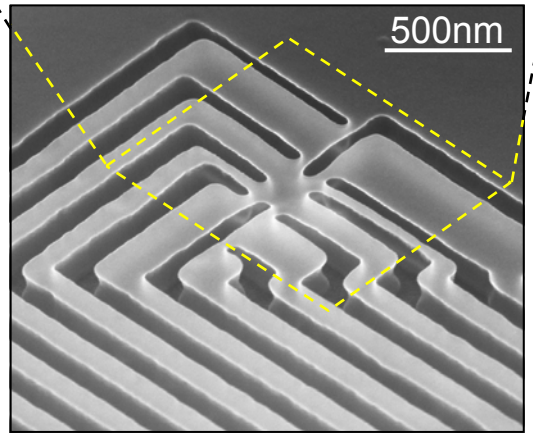


after M1 Etch

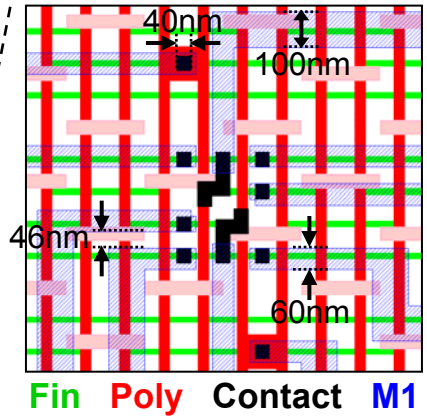


after M1 Litho

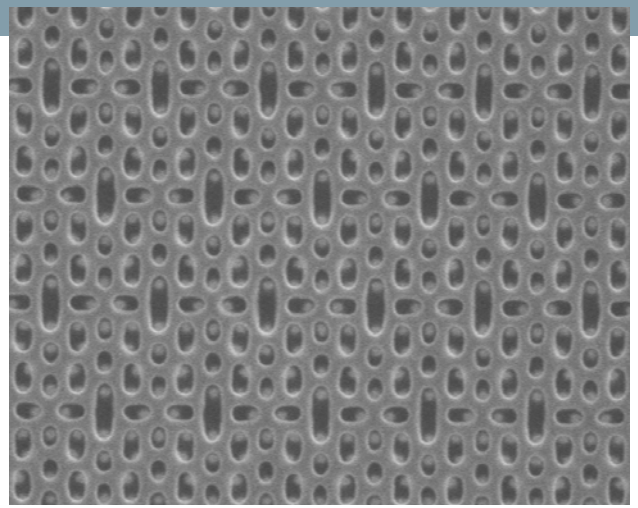


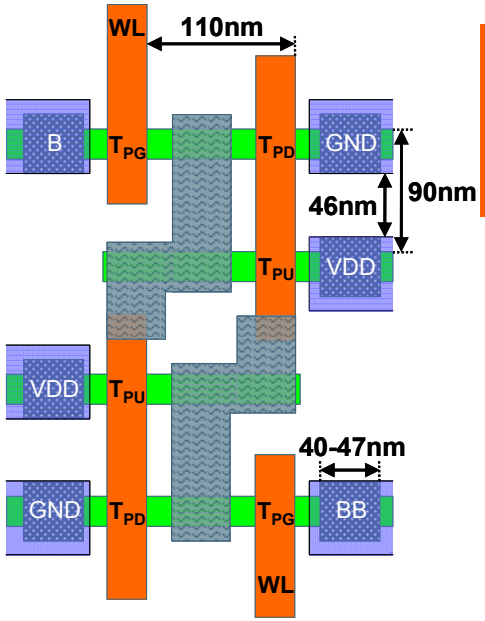


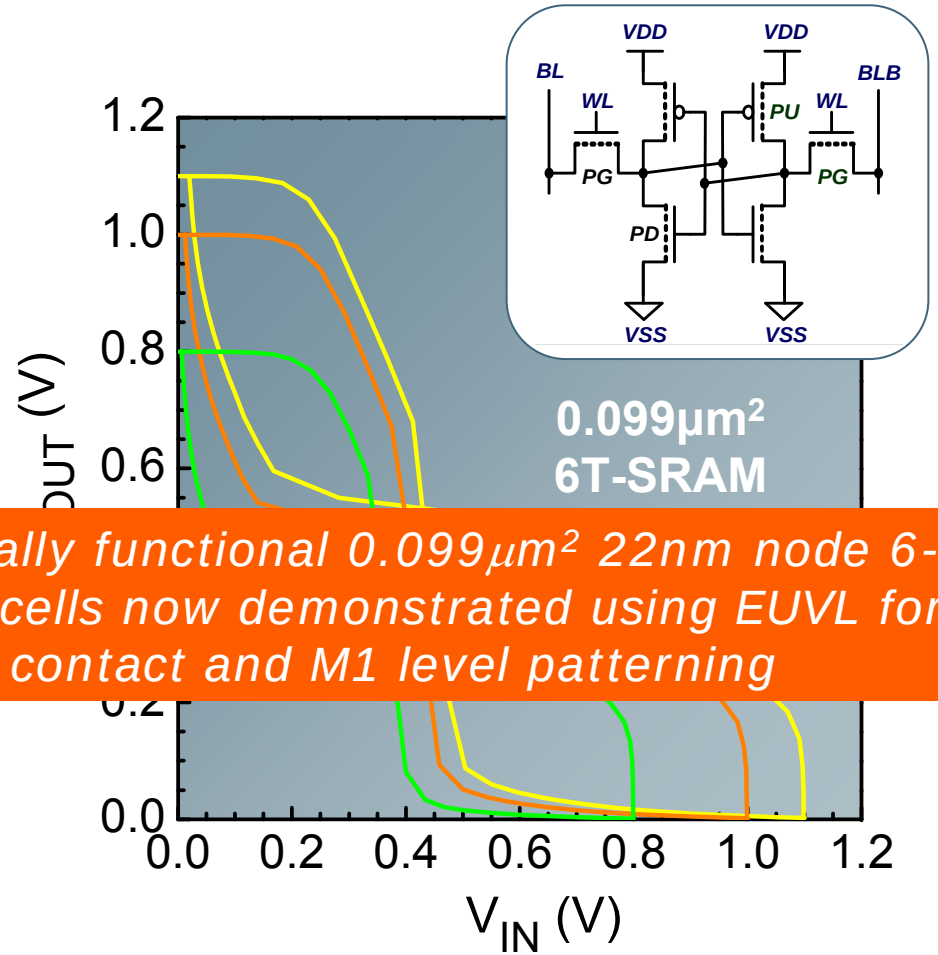
0.099μm² SRAM



Electrical data : butterfly curves







Electrically functional 0.099μm^2 22nm node 6-T SRAM cells now demonstrated using EUVL for contact and M1 level patterning

Outline

- Introduction
- Contact level patterning
- Metal level patterning
- ***Summary***
- Acknowledgements

Summary

- Litho and etch process for contact & metal 1
  - Good CD control after litho and after etch

- Electrically functional 0.099μm^2, High-k/Metal Gate FinFET-based, 6T-SRAM cells demonstrated using a single patterning approach for Contact & M1 levels with Full-Field EUV Lithography (NA=0.25)
  - *Detailed Device results to be presented at IEDM'09 (A. Veloso et al)*

- Patterning of 0.079μm^2 SRAM feasible with current resist

Acknowledgements

Many thanks to:

- ASML
  - ADT teams at IMEC and in Veldhoven
  - Charles Pigneret, Andre van Dijk, Leon Romijn, Sjoerd Lok, Bas Hultermans, Hans Meiling
- TEL
  - Neil Bradon, Kathleen Nafus, Shane 0'Neill, Hideo Shite
- IMEC
  - Gian Lorusso, Vincent Truffert
  - IMEC pilot line
- IMEC IIAP partners
  - Especially Ardavan Niroomand (Micron), Keundo Ban (Hynix), Weimin Gao (Synopsys)

25 imec

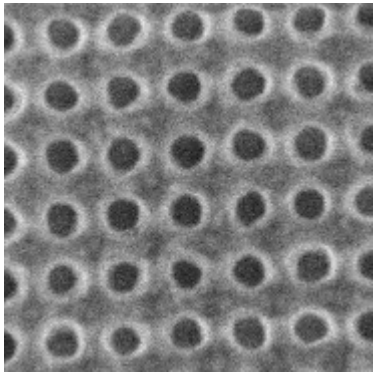
Years of Making Technology Fly

intel Micron Panasonic ideas for life qimonda SAMSUNG tsmc ELPIDA hynix Semiconductor PSC NXP founded by Philips infineon SONY QUALCOMM ST

Back-up slides

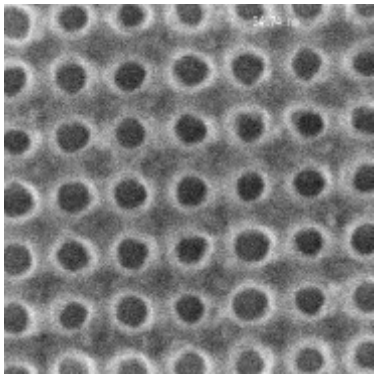
Contact hole resolution on the ADT
Resolution down to 34nm

38nm 1:1



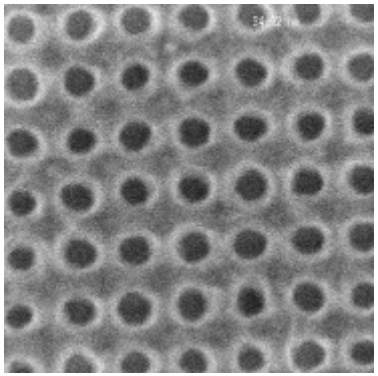
E = 19 mJ/cm^2

36 nm 1:1



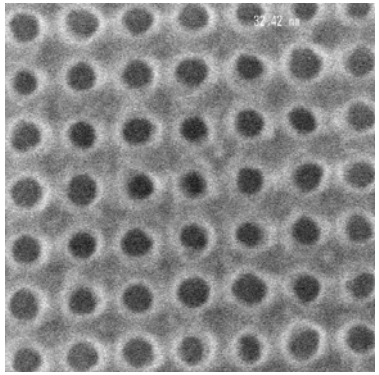
E = 22 mJ/cm^2

35nm 1:1



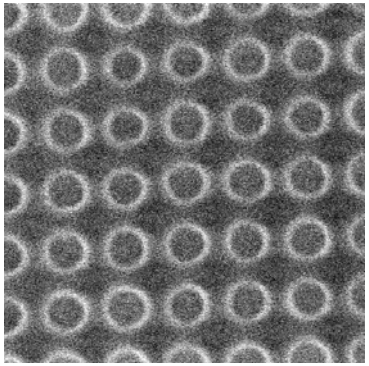
E = 22 mJ/cm^2

34nm 1:1

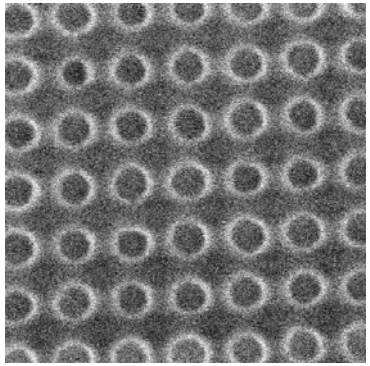


E = 23 mJ/cm^2

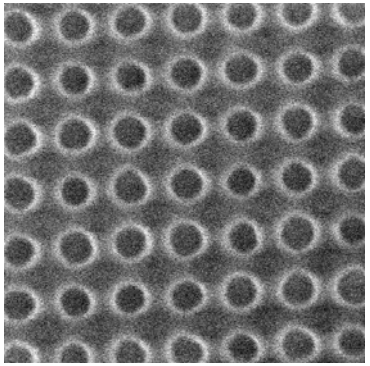
Resist: Fuji FEVS-P1101
Thickness: 80nm



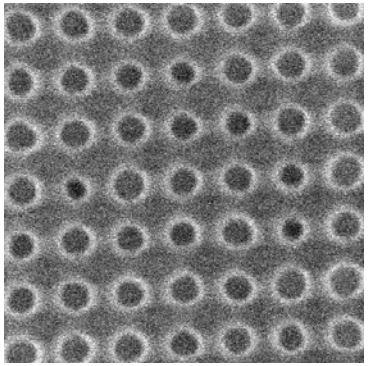
E = 27.4 mJ/cm^2



E = 29.1 mJ/cm^2



E = 32.5 mJ/cm^2



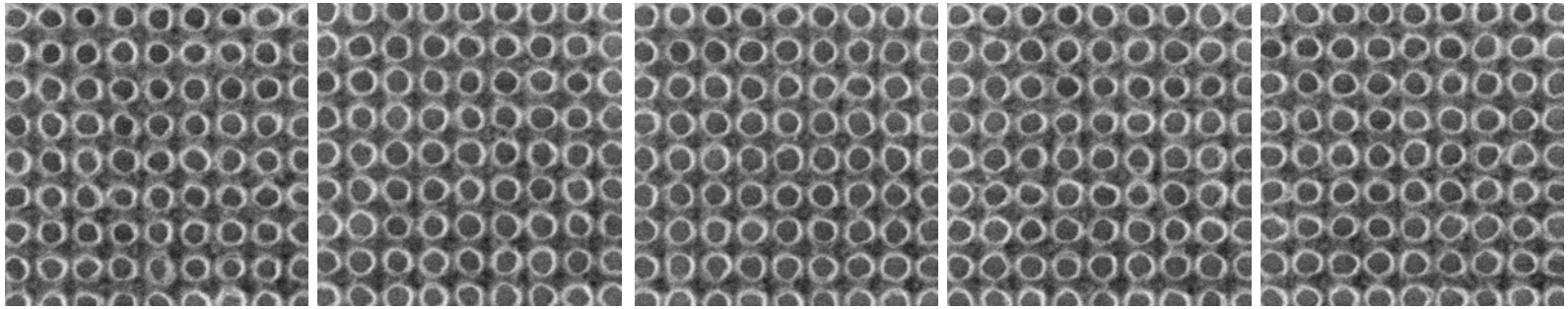
E = 32.5mJ/cm^2

Resist: SEVR-59

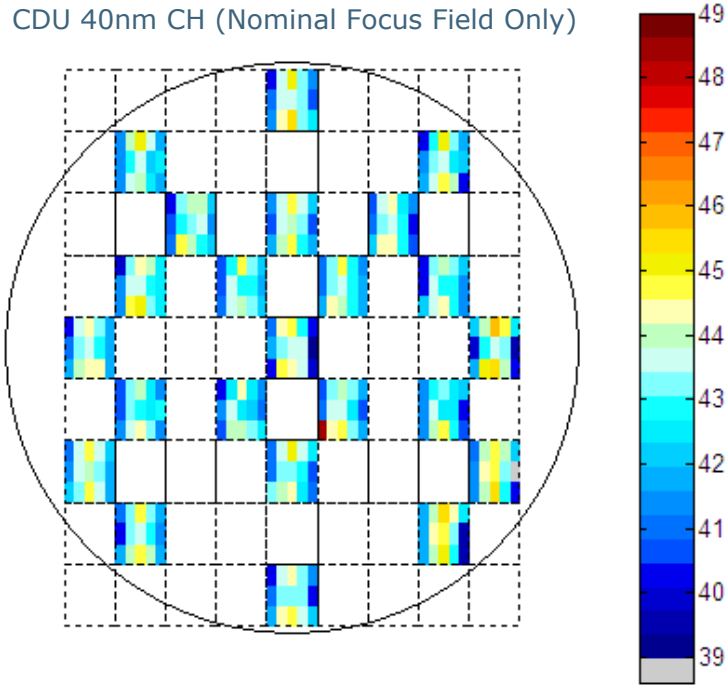
Fuji FEVS-P1101 is the POR resist for contacts
low dose to size and wide processing windows at 40nm

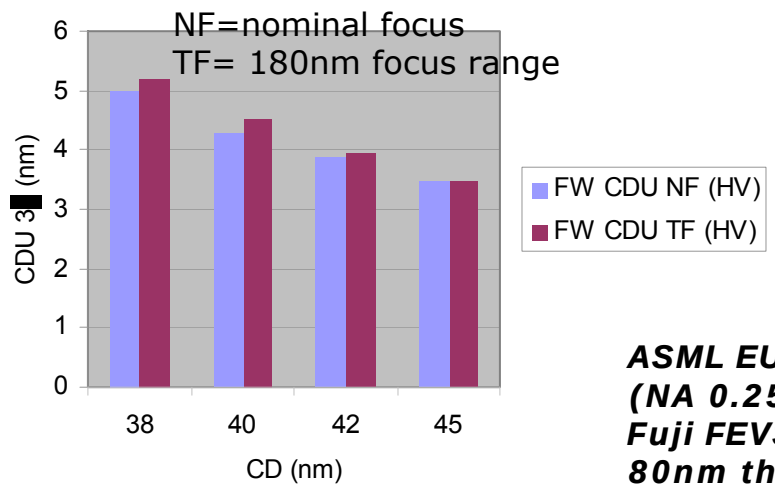
40nm CH performance
CDU performance

40nm CH through slit



CDU 40nm CH (Nominal Focus Field Only)

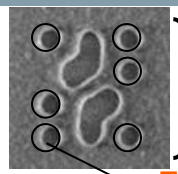




ASML EUV ADT
(NA 0.25, σ=0.5)
Fuji FEVS-P1101
80nm thick

Good CDU results demonstrated

22nm SRAM contact level pattering
CD control for 50nm and 40nm contacts after litho

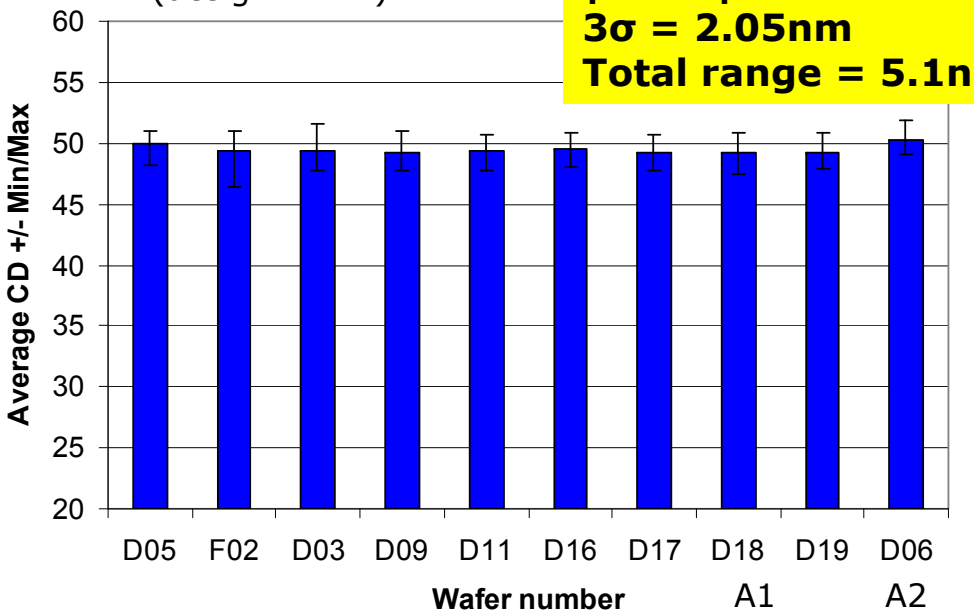


6 CH
Avg. CD

50nm contact
(design 44nm)

CD control
44nm contact design

10 wafer lot
|Mean| = 49.4nm
3σ = 2.05nm
Total range = 5.1nm

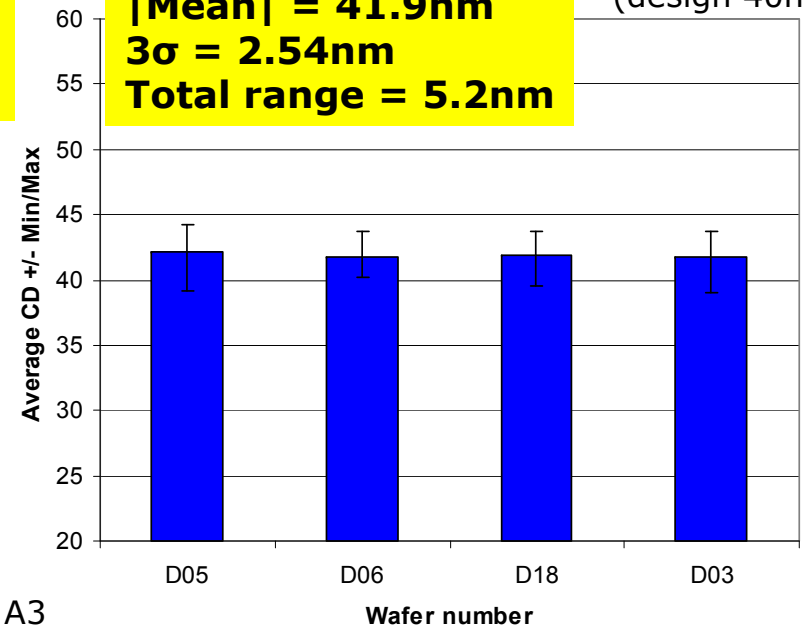


Resist: Fuji FEVS-P1101
80nm thick, 14.5 mJ/cm2
59 fields across wafer
*3*34 points wafer sampling*

CD control
40nm contact design

40nm contact
(design 40nm)

4wafer lot
|Mean| = 41.9nm
3σ = 2.54nm
Total range = 5.2nm



A1 A2 A3

BM=40nm BM=44nm BM=36nm

Resist: Fuji FEVS-P1101
80nm thick, 15 mJ/cm2
59 fields across wafer
*3*34 points wafer sampling*

- Good CD control within wafer and within batch for both 50nm and 40nm CH
- Electrical batch processed with the target contact CD at 50nm after litho