IEUVI Update
EUVL Symposium, Prague
Oct 21, 2009

Paolo Gargini
Chairman ITRS
Chairman Technology Strategy Committee, SIA
Director of Technology Strategy
Intel Fellow
IEEE Fellow
And

David Chan, Jacque Georger, Frank Goodwin,
George Huang, Bryan Rice, Andrea Wüest, Stefan Wurm
Outline

• Background and ITRS Lithography
• IEUVI Overview
• Source TWG
• Resist TWG
• Mask TWG
• EUV Mask Infrastructure Development
• Summary
Outline

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• Resist TWG
• Mask TWG
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• Summary
2009 ITRS
http://www.itrs.net


Europe  Japan  Korea  Taiwan  USA


2009ITRS
2009 Litho ITRS Update
<table>
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<td>DRAM ½ pitch (nm) (contacted)</td>
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<td>45 193 nm immersion with water</td>
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<td>32 193 nm Immersion Double Pattern</td>
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<td>EUV (DRAM / MPU)</td>
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<td>22 EUV</td>
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<td>ML2</td>
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<td>Directed Self Assembly</td>
<td>Interference Lithography</td>
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<td>Narrow Options</td>
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<td>Directed Self Assembly</td>
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This legend indicates the time during which research, development, and qualification/pre-production should be taking place for the solution.

- Research Required
- Development Underway
- Qualification / Pre-Production
- Continuous Improvement

[Source: 2009 ITRS Litho Chapter Tables Work in Progress, Sept, 2009]
Potential Show Stoppers

- **Resist** Limitations (Shot Noise, Photo electron Blur), e.g. set upper limits on LER & Resolution.
- **Cost** of Ownership – all technologies
- **EUV Lithography**
  - **Source** availability at required power levels and life time.
  - **Mask** Defects
  - **EUV Mask Infrastructure** (actinic inspection tools for blank, patterned mask, mask review)
Complexity Level Keeps on Increasing

- Update Lithographic Requirements
  - Separate into DRAM, Flash, MPU
- **Double patterning** (at least 3 types of approaches)
  - Double Exposure (DE), Litho Process Litho Etch (LPLE)
  - DP of Uncorrelated Lines (trenches) / Correlated Lines (lines)
  - Double Patterning Spacer Technology

- Double exposure / patterning requires a complex set of parameters when different exposures are used to define single features
### Litho Requirements

**Table 76a&b  Lithography Technology Requirements—Near-term Years**

<table>
<thead>
<tr>
<th>Year of Production</th>
<th>2007</th>
<th>2008</th>
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<td>59</td>
<td>52</td>
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<td>59</td>
<td>52</td>
<td>45</td>
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<td>CD control (3 sigma) (nm) [B]</td>
<td>7.1</td>
<td>6.2</td>
<td>5.4</td>
<td>4.7</td>
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<td>3.7</td>
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<td>Contact in resist (nm)</td>
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<td>65</td>
<td>57</td>
<td>50</td>
<td>44</td>
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<tr>
<td>Contact after etch (nm)</td>
<td>68</td>
<td>59</td>
<td>52</td>
<td>45</td>
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<td>36</td>
<td>32</td>
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<td>Overlay [A] (3 sigma) (nm)</td>
<td>13.6</td>
<td>11.9</td>
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<td>9.0</td>
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<td>Flash ½ pitch (nm) (un-contacted poly)</td>
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<tr>
<td>Contact after etch (nm)</td>
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<td>36</td>
<td>32</td>
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<td>25</td>
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<tr>
<td>Overlay [A] (3 sigma) (nm)</td>
<td>17.7</td>
<td>14.8</td>
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<td>10.5</td>
<td>9.4</td>
<td>8.3</td>
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<td>MPU/ASIC Metal 1 (M1) ½ pitch (nm)</td>
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<td>52</td>
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<td>64</td>
<td>56</td>
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<td>39</td>
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<td>Contact after etch (nm)</td>
<td>77</td>
<td>67</td>
<td>58</td>
<td>51</td>
<td>45</td>
<td>40</td>
<td>36</td>
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<tr>
<td>Overlay [A] (3 sigma) (nm)</td>
<td>17</td>
<td>15</td>
<td>13</td>
<td>11</td>
<td>10.0</td>
<td>8.9</td>
<td>8.0</td>
</tr>
</tbody>
</table>
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• Background and ITRS Lithography
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• Source TWG
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International EUV Initiative (IEUVI)…

IEUVI Mission: To further the coordination of collaborative efforts among leading EUVL R&D consortia. [http://www.ieuvi.org](http://www.ieuvi.org)
IEUVI – What, How, and Who

• **What:** To address infrastructural issues that need to be resolved for EUVL commercialization.

• **How:** The IEUVI collects technical inputs through its Technical Working Groups (TWGs), and identifies possible show stoppers for commercialization.

• **Who:** IEUVI TWG members include integrated device manufacturers, suppliers, national laboratories and universities.
IEUVI: Since February 2001, 27 meetings

2009 EUVL Symposium
IEUVI Organization

IEUVI Board

Chair: Paolo Gargini  
Organizer: Yumiko Takamori

Member Organizations: IMEC (EU), SEMATECH (US), Selete (JP)  
CEA / LETI (EU), EUVA (JP), MEDEA+, CATRENE, ENIAC, AENEAS (EU),

IEUVI Technical Working Groups (TWG)

Source TWG
Chair: Andrea Wüest (US) SEMATECH
Co-Chairs: Masashi Ogawa (JP) EUVA

Resist TWG
Chairs: Jacques Georger (US) SEMATECH /Intel
Co-Chairs Serge Tedesco (Eu) CEA / LETI  
Masashi Itani (JP) Selete

Mask Infrastructure TWG
Chair: David Chan (US) SEMATECH
Co-Chairs: Iwao Nishiyama (JP) Selete / NECEL  
Jinho Ahn (KR) Hanyang Univ.  
Jan Hendrik Peters (EU) AMTC

Mask Manufacturing TWG
Chair: George Huang (US) SEMATECH/UMC
Co-Chair: Iwao Nishiyama (JP) Selete / NECEL  
Jinho Ahn (KR) Hanyang Univ.  
Jan Hendrik Peters (EU) AMTC
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Source TWG: Goal & Objective

• **Purpose:** Provide a platform for all stakeholders
  - Identify EUV critical issues, and develop consensus on critical technical challenges
  - Provide forum for technical discussions between suppliers and end-users
  - Foster collaborations in development and standardization of source metrology

• **Objective:** Accelerate consensus building in the industry
  - Coordinate key messages to the broader source community
  - Ranking of top technical challenges for HVM implementation of DPP and LPP EUV sources, and update on plans to address the development gaps.
Source TWG: Participating Organizations

- ASML
- Canon Inc.
- Carl Zeiss Laser SMT
- Cymer
- EPPRA
- EUVA
- Gigaphoton
- GLOBALFOUNDRIES
- Hynix
- IBM
- IMEC
- Intel
- LP Photonics
- Media Lario Technologies
- NanoUV Sas
- Nikon Corporation
- Panasonic
- Philips Extreme UV
- Samsung
- Seleve
- SEMATECH
- Toshiba
- TSMC
- Ushio Inc.
- XTREME Technologies GmbH
Source TWG: Accomplishments

• Drive standards development
  – Development of specifications for collector lifetime requirements for alpha, beta and gamma level EUV sources
  – Development of standards for Intermediate Focus (IF) metrology
  – Identified interface opportunities for the industry to reduce cumulative development costs

• Drive industry consensus on critical technical challenges for EUV source commercialization
  – Identify and rank critical issues for EUV source technology
  – Map which of the stake holders will be addressing which EUV source critical issue and which issues are not being addressed
  – Consolidated supplier source performance data into a summary table
2009 On Line Survey Results (89 replies)
Leading EUV Source Technology?

**Pilot line**
- LPP: 55%
- DPP: 44%
- Other: 1%

**HVM**
- LPP: 65%
- DPP: 32%
- Other: 3%
### Survey Results

#### HVM DPP SoCoMo: Showstopper?

<table>
<thead>
<tr>
<th>Question</th>
<th>Percentage</th>
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<tr>
<td>Extendibility to 2nd generation HVM and beyond</td>
<td>63%</td>
</tr>
<tr>
<td>EUV in-band power at IF</td>
<td>55%</td>
</tr>
<tr>
<td>Cost of ownership</td>
<td>45%</td>
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<tr>
<td>Debris mitigation</td>
<td>45%</td>
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<tr>
<td>Collector lifetime</td>
<td>42%</td>
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<tr>
<td>Reliability and stability</td>
<td>42%</td>
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<tr>
<td>Thermal management</td>
<td>37%</td>
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<tr>
<td>Conversion efficiency</td>
<td>34%</td>
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<tr>
<td>Optics contamination</td>
<td>32%</td>
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<tr>
<td>Higher efficiency collector designs</td>
<td>25%</td>
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<tr>
<td>Other: Spectral purity filters</td>
<td>15%</td>
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<tr>
<td>System integration</td>
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*Yes*
Survey Results
HVM LPP SoCoMo: Showstopper?

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<tr>
<th>Issue</th>
<th>Percentage</th>
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<tr>
<td>Cost of ownership</td>
<td>71%</td>
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<tr>
<td>Collector lifetime</td>
<td>60%</td>
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<td>Reliability and stability</td>
<td>59%</td>
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<tr>
<td>Extendibility to 2nd generation HVM and beyond</td>
<td>57%</td>
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<td>Debris mitigation</td>
<td>53%</td>
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<td>EUV in-band power at IF</td>
<td>47%</td>
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<td>Optics contamination</td>
<td>47%</td>
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<td>Driver laser power</td>
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<tr>
<td>Conversion efficiency</td>
<td>37%</td>
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<tr>
<td>Thermal management</td>
<td>35%</td>
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<tr>
<td>Spectral purity filters</td>
<td>34%</td>
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<tr>
<td>Higher efficiency collector designs</td>
<td>29%</td>
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<tr>
<td>System integration</td>
<td>26%</td>
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</tbody>
</table>

Yes
EUV Sources for Actinic Metrology

• Several potential source technologies are being considered for actinic EUV mask metrology inspection tools.

• These source technologies are currently at the development stage and require funding to develop the first generation of fully integrated sources that meet the power and brightness requirements for actinic mask metrology.

• Lack of funding could jeopardize the insertion of EUV lithography at the 22 nm half-pitch node by 2013.
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Resist TWG: Participating Organizations

- AIXUV
- ASML
- ASET
- BOC Edwards
- Brewer Science
- Canon
- Ceil Indus.
- CEA/LETI
- Dongjin
- Energetiq
- Fujifilm
- Global Foundry
- Honeywell
- IBM
- IMEC
- Intel
- JSR
- Nikon
- Nissan Chem.
- Osaka University
- Philips
- Panasonic
- Rohm & Haas (Dow)
- Samsung
- SELETE
- SEMATECH
- Shin-Etsu
- Sumitomo
- SUNY Albany
- Texas Instruments
- TOK
- University of Birmingham
- University of Hyogo
- University of Illinois
Resist TWG: Mission & Objective

- **Mission**: Increased cooperation among EUV resist development community worldwide
  - Coordinate efforts to identify & address top issues

- **Objective**: Provide forum to share information to foster global collaboration to accelerate development of EUV resists

**2009 EUVL Symposium**

Resolutions:
- **Sept. 2008**
  - LBNL e-MET: 15mJ, 24nm hp, 22nm hp, 20nm hp

- **Sept. 2009**
  - Albany e-MET: 14mJ, 24nm hp, 22-24nm hp, LWR: 4.8nm, Sensitivity: 14mJ/cm, DOF: 250nm @ 24nm hp
Resolution using Quadrupole Illumination with three different suppliers CAR resists

UL-1/SMT-3
16.8 mJ/cm²

UL/Resist: UL-1(20nm) / STM-3 (40nm)
PAB: 110C/90sec
PEB: 100C/60sec
Dev: 2.38% TMAH / 30sec
Exp: Albany E-MET 0.3NA Quad

HMDS Si/STM-2
20.0 mJ/cm²

UL/Resist: Si HMDS / STM-2 (50nm)
PAB: 110C/90sec
PEB: 100C/90sec
Dev: 2.38% TMAH / 30sec
Exp: Albany E-MET 0.3NA Quad

UL-1/SMT-5
14.0 mJ/cm²

UL/Resist: UL-1(20nm) / STM-5 (50nm)
PAB: 110C/60sec
PEB: 100C/60sec
Dev: 2.38% TMAH / 30sec
Exp: Albany E-MET 0.3NA Quad
ADT Resolution to 26nm hp Demonstrated

Resist Performance of SMT7 Resist at ADT

<table>
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<th>BF +120nm</th>
<th>30nm HP</th>
<th>29nm HP</th>
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<th>25nm HP</th>
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<td>LWR 3.4nm</td>
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<td>LWR 4.0nm</td>
<td>LWR 5.5nm</td>
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<td>BF +40nm</td>
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<tr>
<td>LWR 3.9nm</td>
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<td>Best Focus</td>
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<td>BF -40nm</td>
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<td>BF -80nm</td>
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- SMT7 is a champion resist exposed at ADT in terms of Z-factor analysis.
- Resist collapse need to be improved for 27nm HP patterning.

*C. Koh et. al. EUVL 09 Poster*
Aerial Image Quality on Intel MET
NA = 0.30, On-Axis Dipole vs Quadrupole Comparison

Quadrupole

On-axis dipole

Resist F DOF: (Defined by LWR ≤ 6 nm) = 300 nm (On-Axis Dipole) vs. 50 nm (Quad)

*T. Younkin et. al, EUVL Oct. 19, 2009
Pattern Collapse improvement by New Developer

Pattern collapse was improved using New developer

TMAH
0.26N

TBAH
(Tetrabutyl ammonium hydroxide)
0.26N

SFET NA0.3
Resist : SSR4
Thick. : 50nm

X-slit

*K. Matsunaga et. al
IEUVI Oct. 18

2009 EUVL Symposium
Resist TWG 22nm hp Status Update

Progress

• Several resist vendors are now demonstrating 24-22nm hp resolution with CAR on all EUV Micro Exposure Tools
  – Good 24nm hp process windows at 50nm resist thickness have been demonstrated on METs
  – Under-Layer/Resist stack optimization improving process windows and helping LWR
  – Resist sensitivity improving with several ~10mJ/cm² resists with good resolution (26nm hp demonstrated)
  – SEMATECH relaxed resist outgassing Spec to 3x10¹⁵ for ADT, is now allowing best in class resist screening on full field tool
  – New resist platforms (Molecular glass) continue to improve but CAR resists continue to be best in overall RLS performance

Current Gaps

– Pattern collapse reduction work needed for 24nm hp and below
– LWR in resist only down to ~4.5nm at 24nm hp
– Post litho process combined with optimized pattern transfer work required to drive LWR below 2nm
– Understanding how MET imaging performance translates to full field tools is needed
– Higher NA & Sigma METs needed to push beyond 20nm hp
– 4-5x Masks with sub 22nm hp resolution needed for sub 22nm materials development
Reducing LWR Gap with Post Processing?

Post develop Rinse¹
- LWR reduced from 5.3-3.9nm @ 30nm hp
- Little to no resist CD change
- 25% reduction no throughput impact

Grazing incidence Ion Beam²
- LWR reduced from 9.7-5.5nm @ 40nm hp
- Less than 10% resist CD/Thickness change
- 30-40% reduction @ 300 wafer/hr

Pattern transfer Optimization³
- LWR reduced from 9.7-> 4.0nm in HM transfer
- LWR reduced further 4.7-> ~2.2nm at 32nm
- Greater than 10% CD change/trim
- 20-40% reduction with standard HM pattern transfer

Can various post processing methods combined with pattern transfer reduce LWR by 60-70% in final device features?

1) G. Vandentop, et al 2009 SPIE Keynote
2) David Ruzic et al. Proc SPIE Vol. 7273, 727346, 2009
3) Lam Research LWR proposal to SEMATECH RFI
Next IEUVI Resist TWG Meeting
Feb. 2010 @ SPIE
Outline

• Background and ITRS Lithography
• IEUVI Overview
• Source TWG
• Resist TWG
• Mask TWG
• EUV Mask Infrastructure Development
• Summary
Mask TWG: Mission & Objective

• Mission:
  Ensure EUV Mask Infrastructure Readiness for:
  • Pilot Line Production 2010 – 2012
  • High Volume Manufacturing 2013 - 2016

• Objectives:
  – Identify Required Standards
  – Coordinate industry-wide conversions, such as
    future mask incidence angle change.
  – Identify any gaps between current industry
    efforts and projected future needs
  – Highlight gaps to member organizations and
    IEUVI Board for action
Mask TWG: Members

- Alcatel
- AMD
- AMTC
- Asahi Glass Co.
- ASML
- Canon
- Carl Zeiss
- CSNE
- Corning Inc.
- Dai Nippon Printing
- Entegris
- Hanyang University
- Hoya Corp.
- IBM
- Intel
- IMEC
- KLA-Tencor
- Lasertec
- Lawrence Berkeley N.L.
- Nikon
- NuFlare Technology Inc.
- Ohara
- Photronics
- Qimonda
- Samsung
- SELETE
- SEMATECH
- SEMI
- Toppan Printing Co.
- Toshiba
- TOSO
- TSMC
- Veeco Instruments Inc.
- Wisconsin University
- UMC
Mask TWG: 2009 Accomplishment

- **SEMI Standard Accomplishment**
  - **E152** - Mechanical Specification of EUV Pod for 150 mm EUVL Reticles
    - Adjudicated in April 2009, published in July 2009
  - **P40** - Mounting Requirements for EUV Masks
    - Adjudicated on July 14, 2009, will be published this year
  - **P37** - Specification for Extreme Ultraviolet Lithography Substrates and Blanks
    - Adjudicated in September, 2009, will be published this year
  - Specification of **Fiducial Marks for EUV Mask Blanks**
    - Agreement made by taskforce to submit blue ballot in Q4, ‘09; yellow in Q1, ‘10

- **Dual Pod Status**
  - SEMI compliant Dual Pods arrived in SEMATECH in June
  - Particle protection testing is on-going

- **ITRS EUV Mask Specifics**
  - Team formed. Survey results rolled up.
  - 7 parameters with agreed changes. Six areas identified champions for next revision.
Mask TWG: Development Gaps
(to be discussed at Thursday TWG)

- **Pilot Line 2010-2012:**
  - **Substrate:** Polish defects, flatness, defect inspection & analysis
  - **Blanks:** ML deposition, reflectivity uniformity, defect inspection & analysis & repair
  - **Mask Writing:** Pattern defect inspection, full-field actinic inspection,
  - **Pattern Repair:** FIB Tool/process, small-field actinic inspection
  - **Fab use:** In-Fab inspection and cleans

- **HVM issues (> 2013)**
  - When does mask incidence angle change from 6º to ≥ 8º?
  - Mask defect printability and fiducial mark implementation
Challenges

• **Mask defect reduction** during mask make
  – Industrial consensus of inspection and defect review strategy and affordable path of implementation
  – Printability study
    • Size, Depth, Shape, Pattern
    • Defect printability mask availability and standardization
  – Blank defect inspection and reduction
  – ML defect inspection and reduction
  – Mask writing defect inspection and repair
  – Fiducial mark implementation
  – Mask surface roughness on resist LER and inspection sensitivity

• **Mask quality control** during mask use
  – Dual Pod compatible interface
  – Mask storage (defects and potential progressive growth prevention)
  – Cleaning
Plans

• **Short Term (Pilot Line 2010-2012)**
  – Refine/Update ITRS roadmap
  – Update/Establish SEMI standards
  – Address and take steps to close key mask infrastructure gaps (e.g. inspection) towards pilot line and HVM needs

• **Long Term (HVM > 2013)**
  – Mask defect reduction
  – Mask life time improvement
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SEMATECH EUV Mask Infrastructure Technical and Business Working Groups*

• In July, SEMATECH conducted a Workshop on EUV Mask Infrastructure
  – Attended by executives from over 20 EUV stakeholders including chip, mask, blank and tool makers
  – Consensus output from meeting was
    • Actinic tools will not be in time for 2011 Pilot Line
    • Existing mask metrology capability must be understood and extended to support through pilot line
    • HVM requirements must be specified and new tool needs identified
    • Funding for new tools must be obtained and pooled in a new consortium

• SEMATECH is leading the formation if this new mask infrastructure consortium
  – Formed Technical Working to specify requirements and gaps
  – Formed Business Working group to create workable funding models

*See Brian Rice’s presentation: Reticle Inspection Gap
SEMATECH EUV Mask Infrastructure (EMI) Consortium

- SEMATECH technical working group (EMI TWG)
  - Customers, suppliers, SEMATECH facilitation
  - Establish consensus on requirements (need, tool types, timing, initial specifications, ..)

- SEMATECH business working group (EMI BWG)
  - Suppliers, customers, consortia, funders
  - Consortia member LOI funding commitments by year end
SEMATECH Consortium Output

• The **Technical Working Group** has assessed the capability of a large number of metrology tools and has concluded pilot line needs can be met without actinic equipment:
  – Existing substrate and blank inspection capability exits down to ~40nm sensitivity and can likely to upgraded to 25nm sensitivity
  – Print testing can satisfy AIMS need in the short term
  – Optical patterned mask inspection can support 22nm pilot line
  – Actinic blank inspection and AIMS are critical for 22nm HVM
  – Advanced PMI is needed beyond 22nm (actinic/ebeam/etc)

• **The Business Working Group** has identified consensus funding models
  – Those who benefit from EUV pay mask metro NRE
    • Need $250M+ NRE to fund all three tools
  – NRE is recovered through royalties on tool sales and blank sales
  – Needed actinic tools would start becoming available in 2013
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Summary

• **Good progress overall!** Attention is shifting on cost of ownership, items missing in infrastructure and realistic insertion schedule (i.e., Pilot Line, HVM)

• Cooperation is even more relevant than ever before as EUV infrastructure development remains a major risk for EUV insertion (i.e., contact the IEUVI TWG Chairs if you have contributions!) [http://www.ieuvi.org](http://www.ieuvi.org)

• Sematech Mask Infrastructure Business Working Group (EMI BWG) proposed!

• Do additional BWGs need to be formed to address commercialization of EUV?

• There are not too many technology nodes left for EUV to make a difference!