EUV lithography at the 22-nm technology node

Obert Wood[1], Chiew-Seng Koay[2], Karen Petrillo[2], Hiroyuki Mizuno[3], Sudhar Raghunathan[2], John Arnold[2], Dave Horak[2], Martin Burkhardt[4], Gregory Mcintyre[2], Yunfei Deng[5], Bruno La Fontaine[5], Uzo Okoroanyanwu[1], Anna Tchikoulaeva[6], Tom Wallow[5], James H.-C. Chen[2], Mathew Colburn[2], Susan S.-C. Fan[2], Bala Haran[2], Yunpeng Yin[2], Christian Holfeld[7], Jens Techel[7] and Jan-Hendrik Peters[7]

GLOBALFOUNDRIES

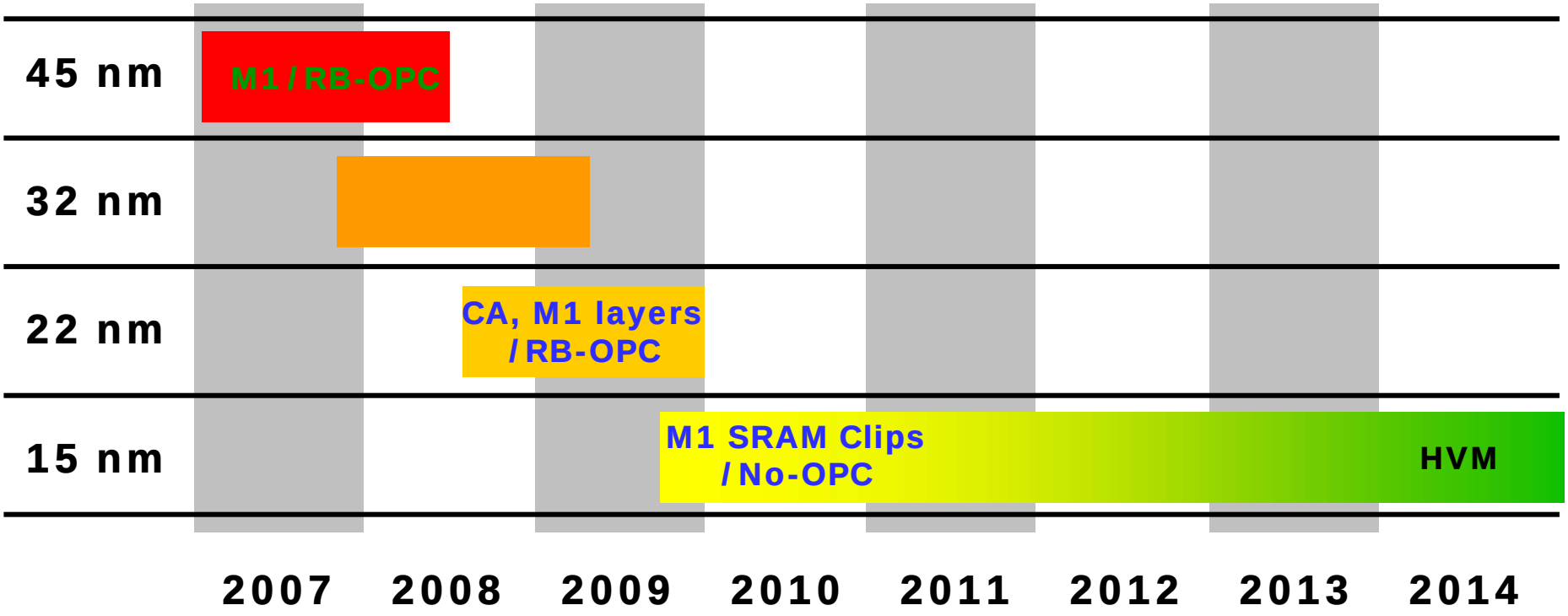
[1]GLOBALFOUNDRIES, 257 Fuller Road, Albany, NY 12203 USA
[2]IBM Corporation, 257 Fuller Road, Albany, NY 12203 USA
[3]Toshiba America, 257 Fuller Road, Albany, NY 12203 USA
[4]IBM Corporation, 2070 Route 52, Hopewell Junction, NY 12533
[5]GLOBALFOUNDRIES, 1050 E. Arques, Sunnyvale, CA 94088
[6]GLOBALFOUNDRIES, Wilschdorfer Landstrasse 101, D-01109 Dresden, Germany
[7]AMTC, Rahnitzer Allee 9, D-01109 Dresden, Germany

Outline of Presentation

- Introduction
- Small-Field 22-nm Node Test Chip
  - EUV lithography: CA level
  - EUV lithography: M1 level
  - Electrical testing
- Large-Field 22-nm Node Test Chip
  - EUV lithography: CA level
- Beyond the 22-nm Technology Node
- Conclusion

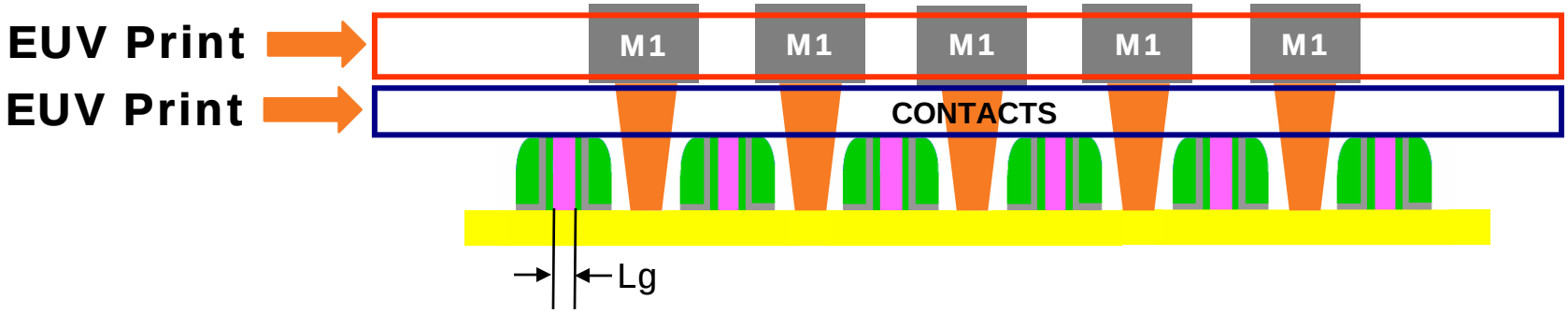
EUV Device Demonstration Roadmap

- Our goal is to test EUVL feasibility via device fabrication exercises
- This provides a true test of the readiness of the technology and highlights the remaining critical issues



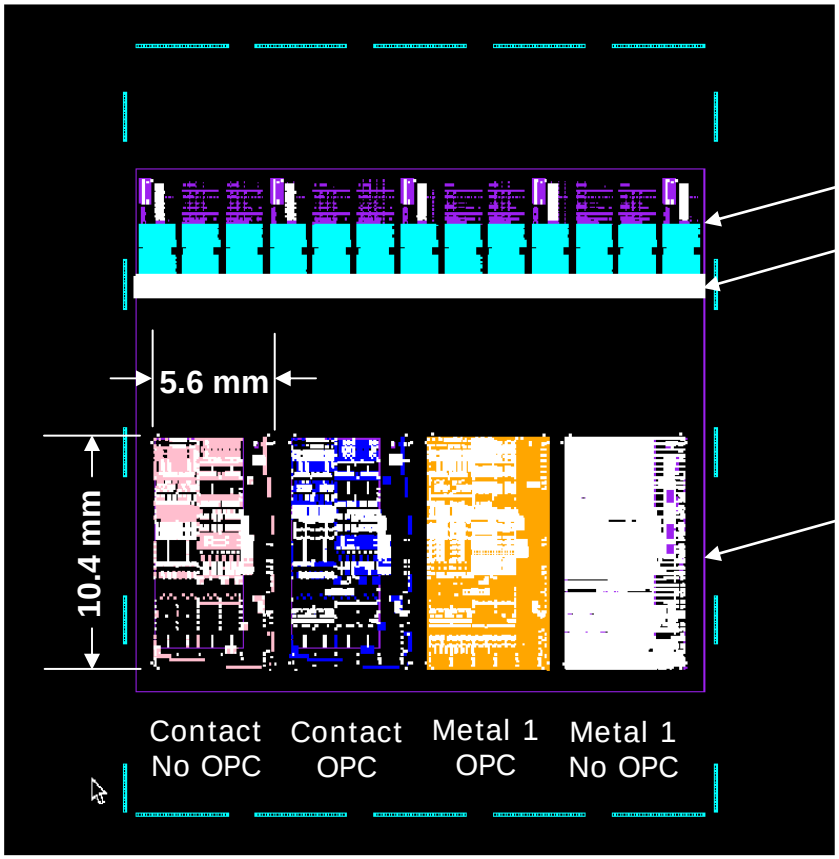
EUV Device Demo Overview

- 22 nm technology test chips
  - High-k metal gate transistors (Lg = 25 nm) printed with double-exposure double-etch (DE^2) 193i lithography
  - CA & M1 levels printed with EUV lithography
- All wafer processing carried out at the College of Nanoscale Science & Engineering's (CNSE) Albany Nanotech Complex



B.S. Haran, et al., Proc. IEDM (2008)

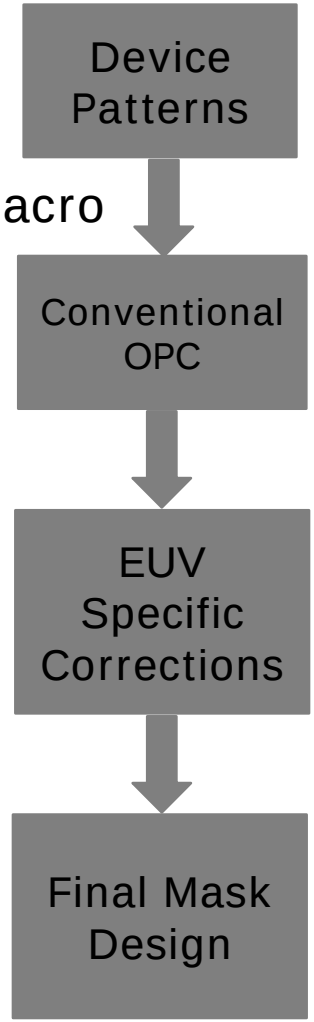
Small-Field 22-nm Node Test Mask



OPC Test Macro

Litho Diagnostics Macro

Contact & Metal 1 Levels



OPC Requirements

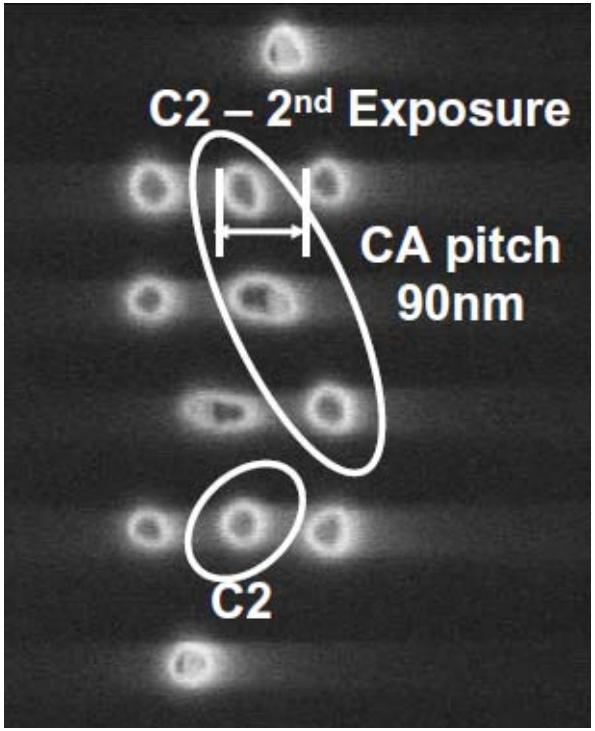
Contact Array : Conventional & HV Bias

Metal 1: Conventional, HV Bias & Flare

EUV Lithography: CA Level Resist Images

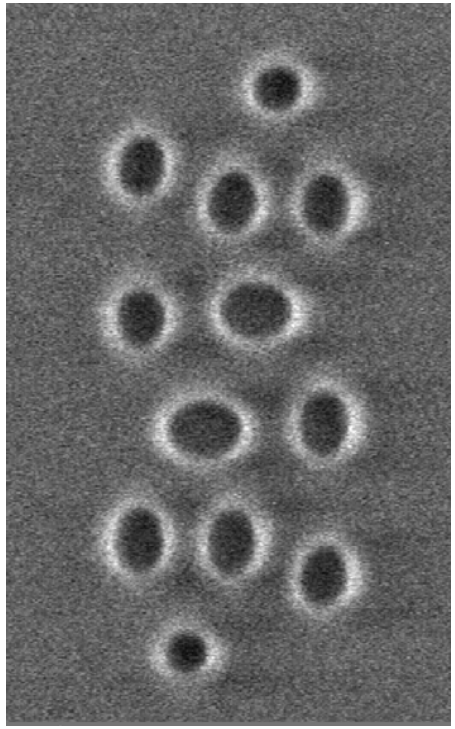
22-nm Node 6T SRAM Flycells

193i Pitch-Split DE[2]



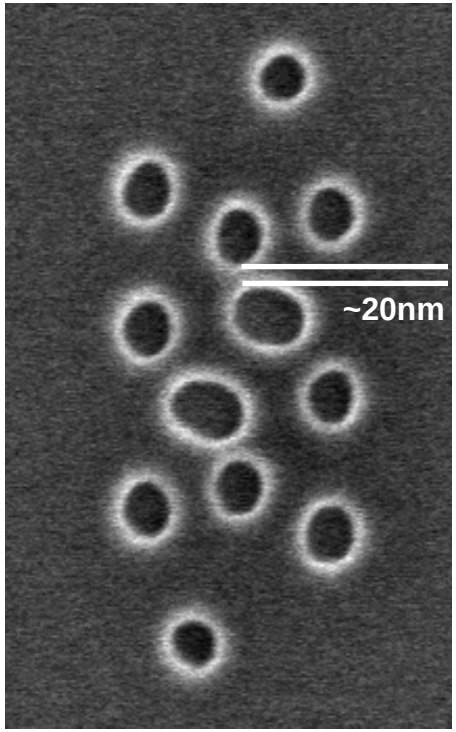
2008 IEDM
(0.100 µm²)

EUV SE Print



2009 SPIE
(0.080 µm²)

EUV SE Print



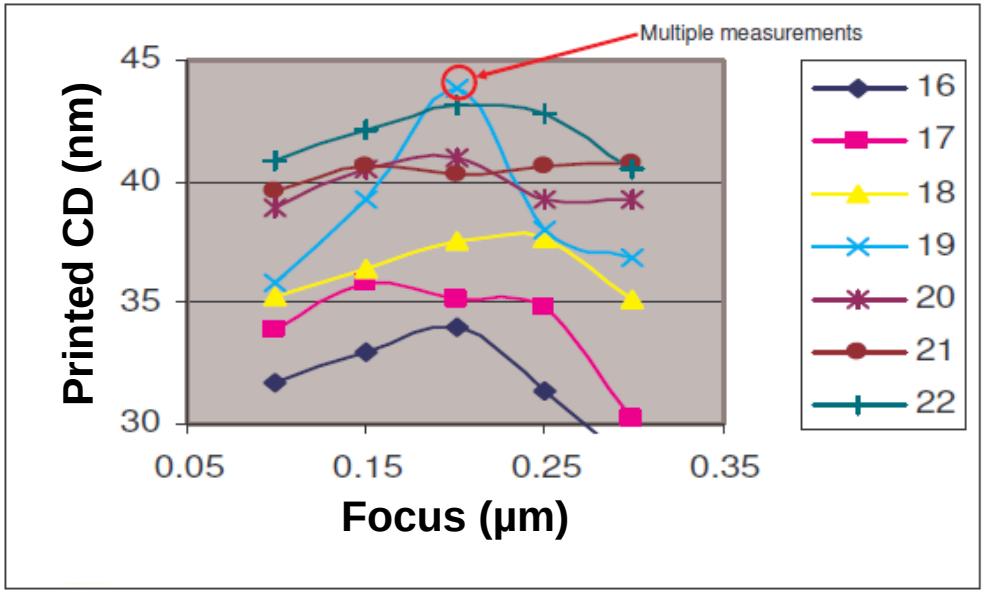
Today
(0.074 µm²)

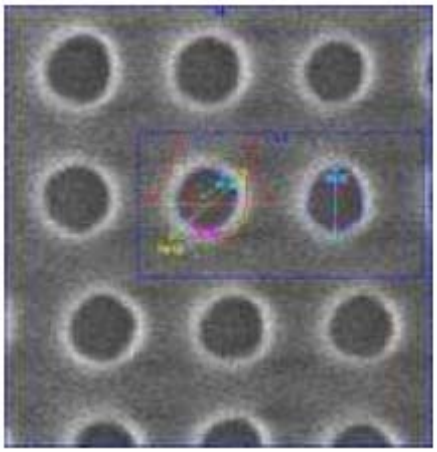
~ 20 nm space between contacts are consistently resolved!

EUV Lithography: CA Level Process Window

40 nm 1:1 Contact Hole Printing

SEVR-78 Resist, 100 nm Film Thickness



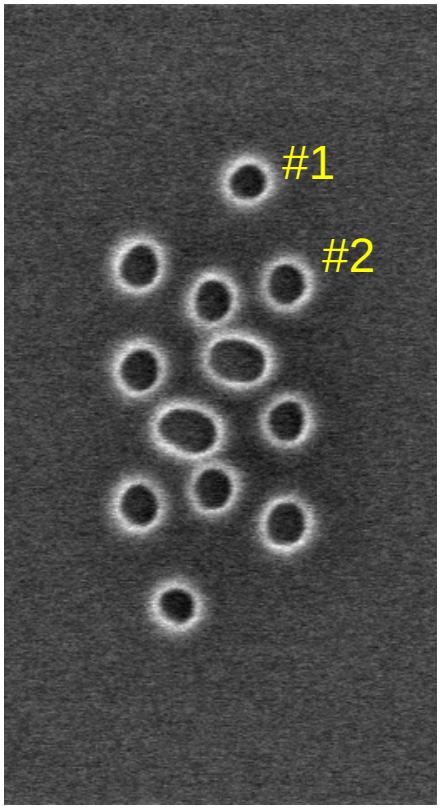


Exposure Latitude	DOF	Dose	CDU	Circularity	Eccentricity
33.9%	~200 nm	18 mJ/cm^2	4.7 nm	1.03	0.35

EUV Lithography: CA Level CD Control

0.074 μm^2 6T SRAM CA Flycell

SEVR-78 Resist, 100 nm Film Thickness, 18 mJ/cm^2 Dose

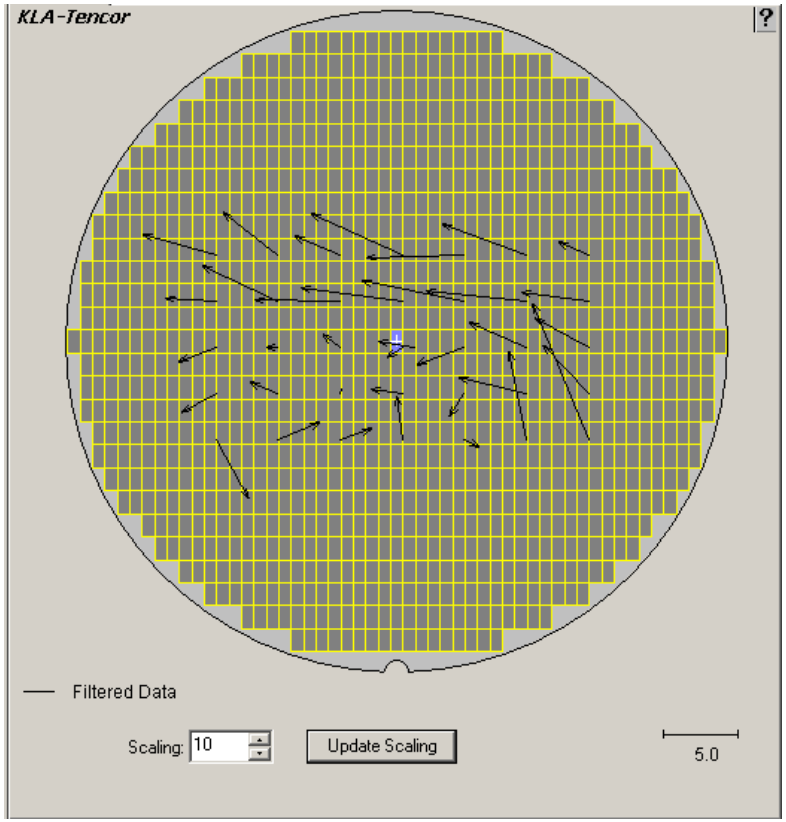


Contact #	Average CD	3 sigma
1	37.2 nm	4.1 nm
2	44.2 nm	4.0 nm

EUV Lithography: CA to PC Overlay

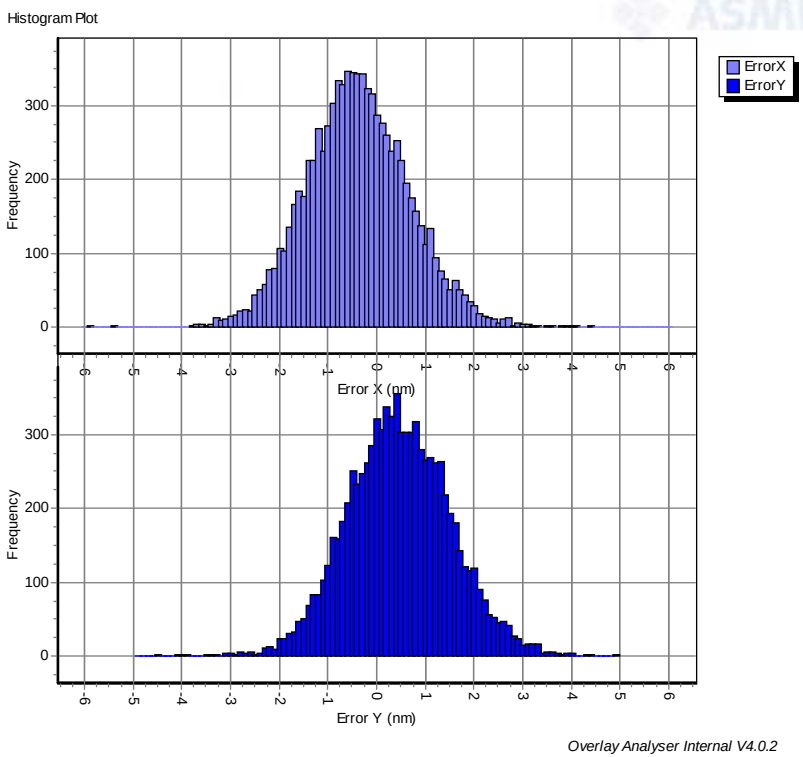
- On-product overlay: mean+3sigma = 10.2 nm (x) & 6.2 nm (y)

On-product overlay map



Single Machine Overlay

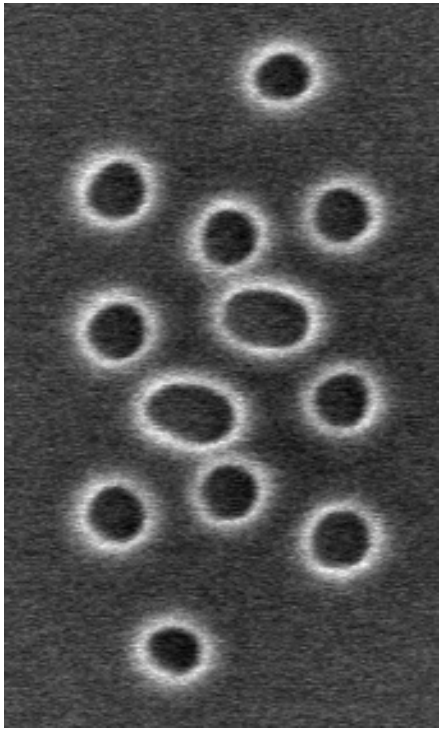
X = 2.2 nm, Y = 2.8 nm



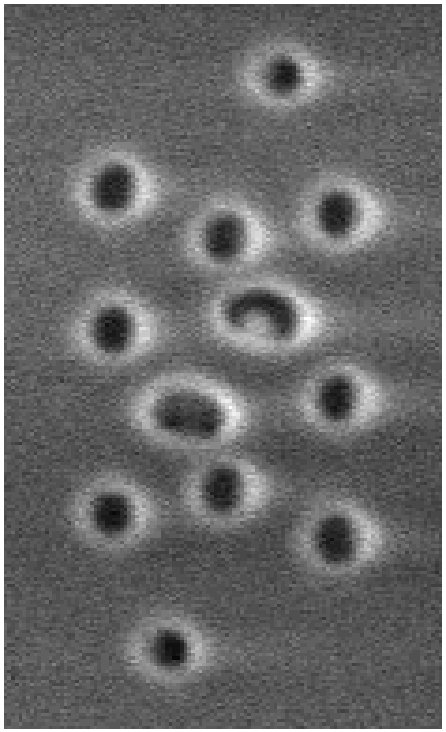
EUV Lithography: CA Level Resist Processing

0.074 μm^2 6T SRAM Flycell

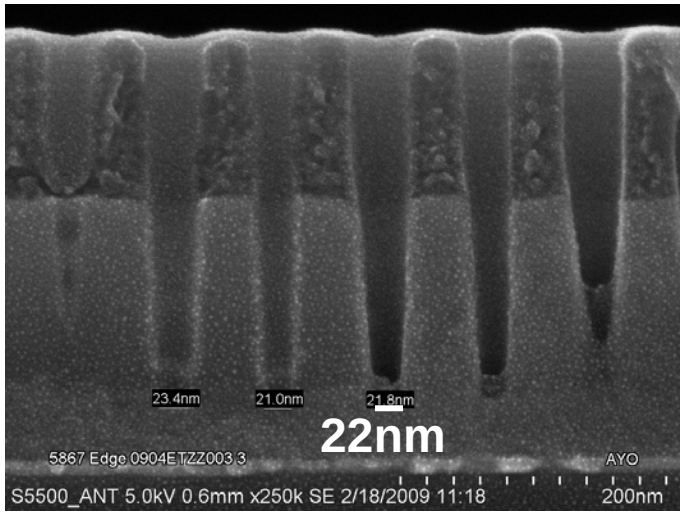
Post Litho



Post Etch



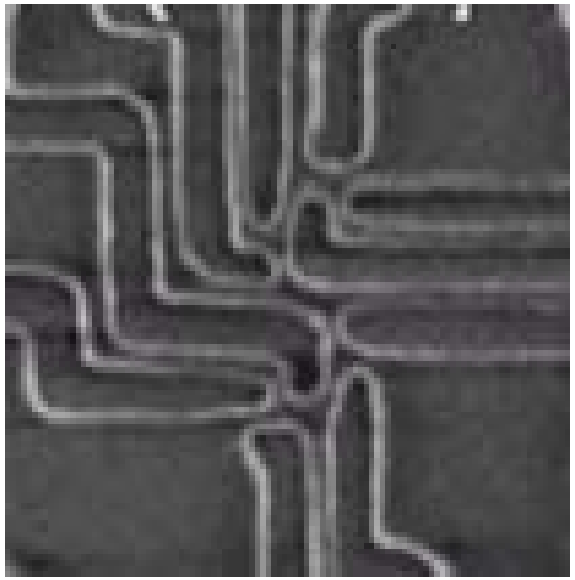
Post Etch Cross Sections



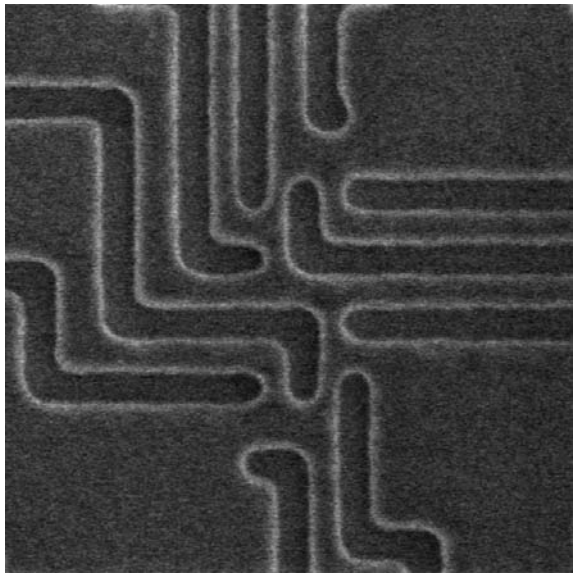
EUV Lithography: M1 Level Resist Images

0.08 µm² 6T SRAM M1 Flycell

193i Double Dipole

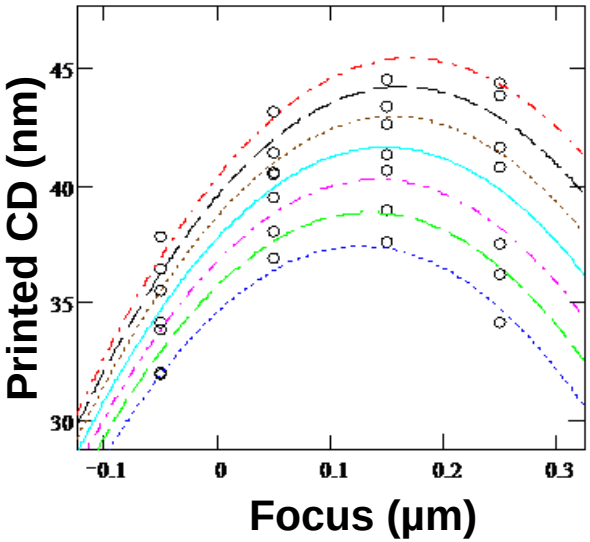


EUV SE Print



SEVR-40 Resist
100 nm Thickness
35 mJ/cm^2 Dose

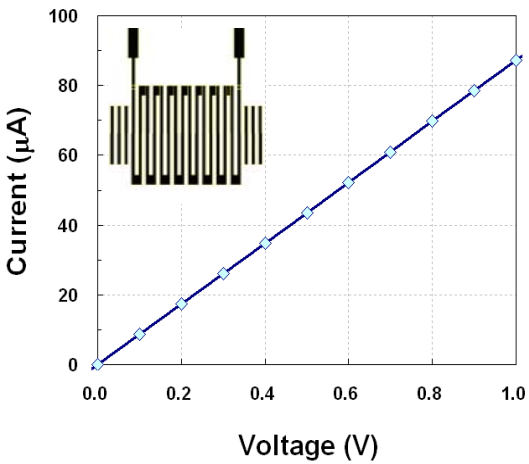
EUV Process Window



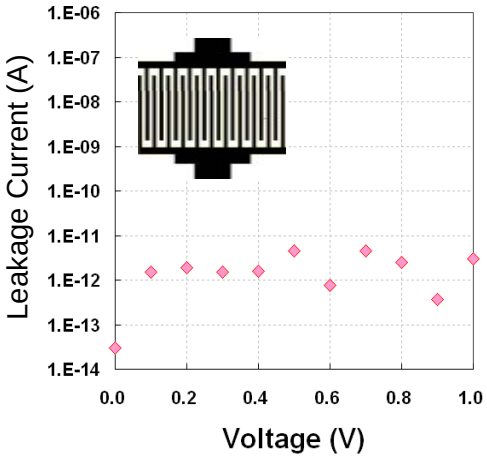
Electrical Test Results

- Good linearity on the resistance of 40 nm Cu lines.
- No leakage current between the 40 nm spaces.
- Measured I_{off} – I_{dsat} characteristics of L_g = 25 nm pFET transistors.

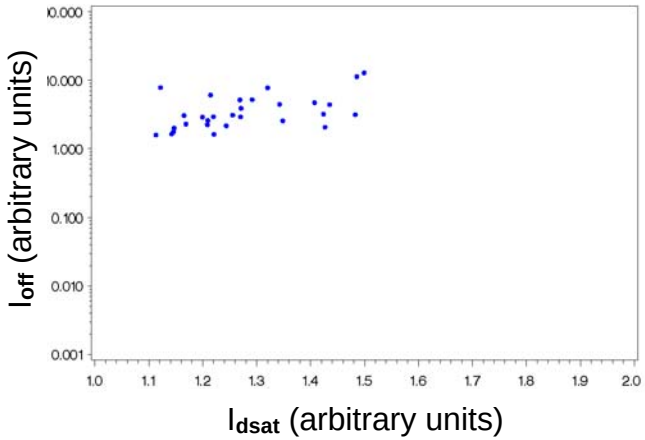
Two Point Resistance Macro



Two Comb Macro

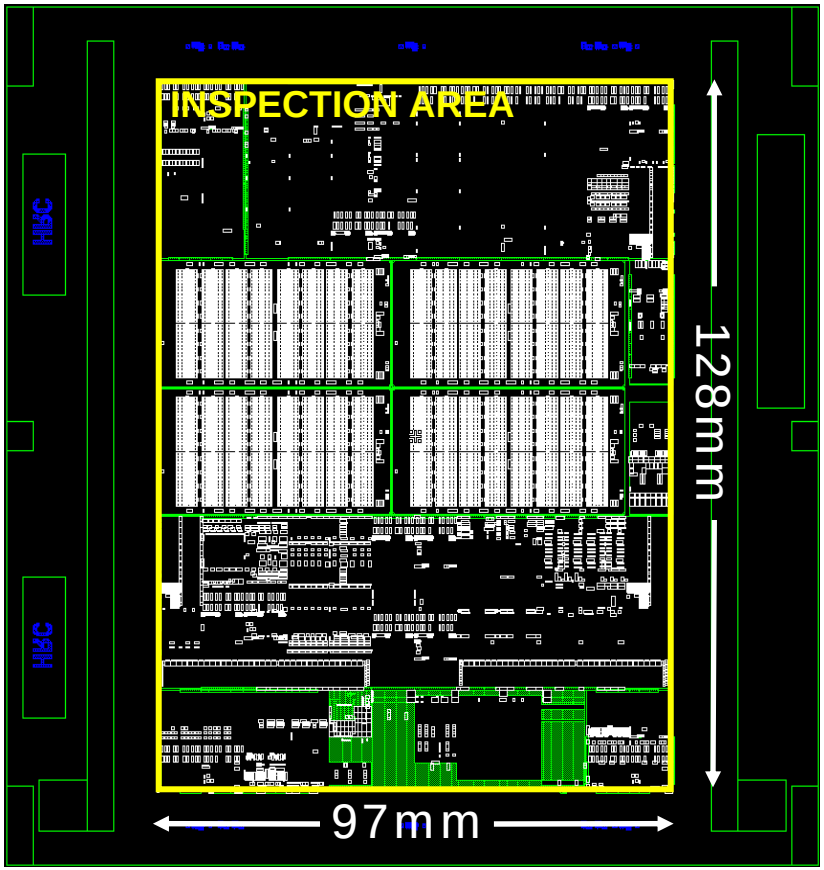


pFET Transistor Characteristics



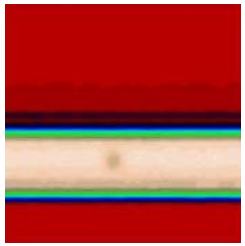
Large-Field 22-nm Node Test Mask

- Die-to-database inspection with KLA-Tencor 587 inspection tool located 34 defects > 60 nm size
- Defect density ~ 0.3 defects/cm^2

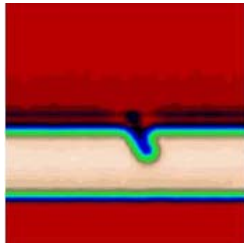


Defect Examples

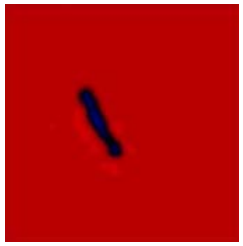
Blank Defect



Pattern Defect



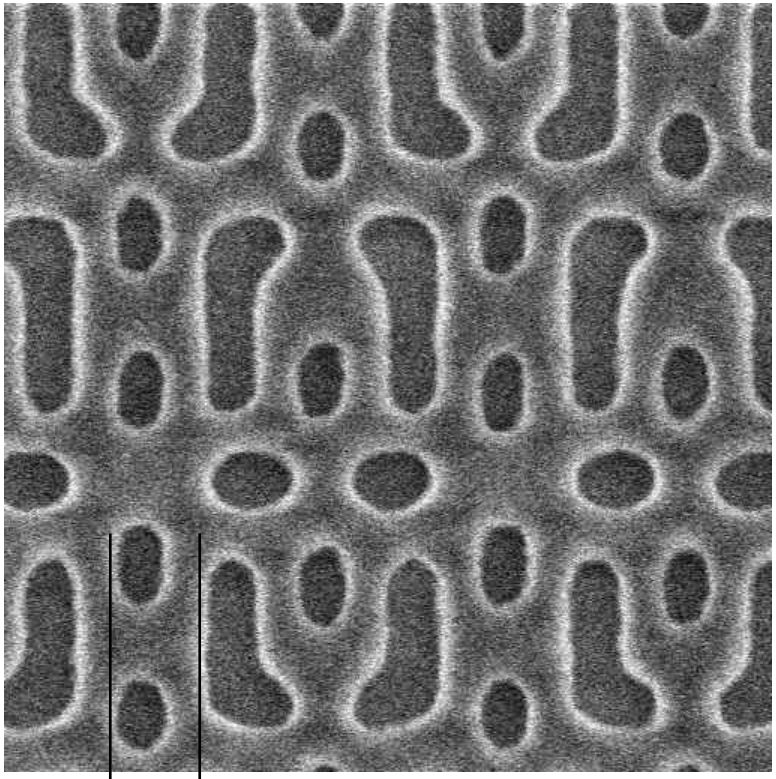
Particle



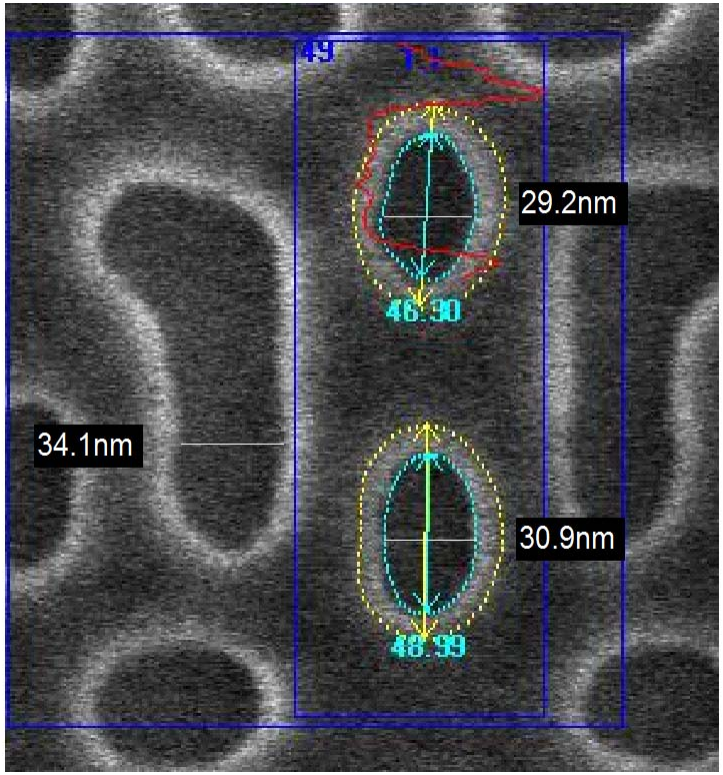
EUV Lithography: CA Level Resist Images

- Via and local interconnect (L-shape) printed with single EUV exposure at 80 nm pitch

0.076 µm² 6T SRAM Array



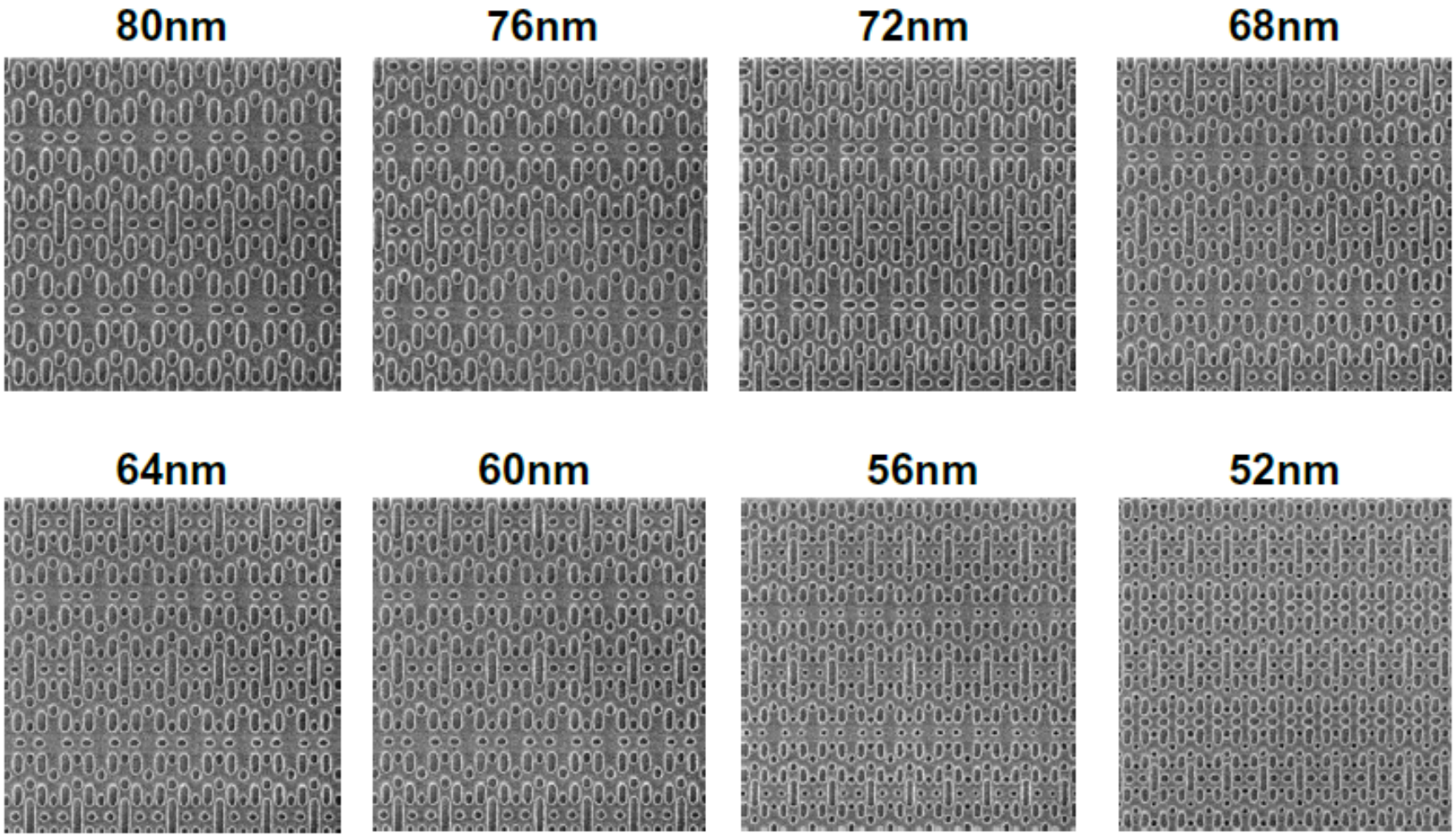
80nm pitch



width CD = 30 nm

EUV Lithography: Beyond the 22-nm Node

Scaled M1 SRAM Clips, SEVR-139 Resist, 75 nm Film Thickness



Conclusions

- EUV lithography with the ADT has successfully been used to print CA and M1 levels on 22 nm node test chips.
- Printing at the 22 nm node with EUV lithography is considerably easier than with double-exposure double-etch 193i lithography.
- Recent progress in EUV resist development has been outstanding and the performance of state-of-the-art resists is already sufficient for 22 nm node pilot production.
- EUV lithography with the 0.25 NA ADT will support some early device development work beyond the 22-nm node.
- Mask defectivity is the most serious remaining EUVL critical issue.
- Mask defectivity is not as bad as it might be expected given current blank defect levels, but is still considerably higher than the level needed for HVM.

Acknowledgements

- The authors grateful acknowledge the invaluable assistance of and extensive support from ASML's ALAR and CS Teams in Albany, New York.
- Device fabrication was carried out at the College of Nanoscale Science & Engineering's (CNSE) Albany Nanotech Complex.
- Portions of this work were performed by the Research Alliance Teams at various IBM Research and Development Facilities.