EUVL Projection on Memory Device Roadmap

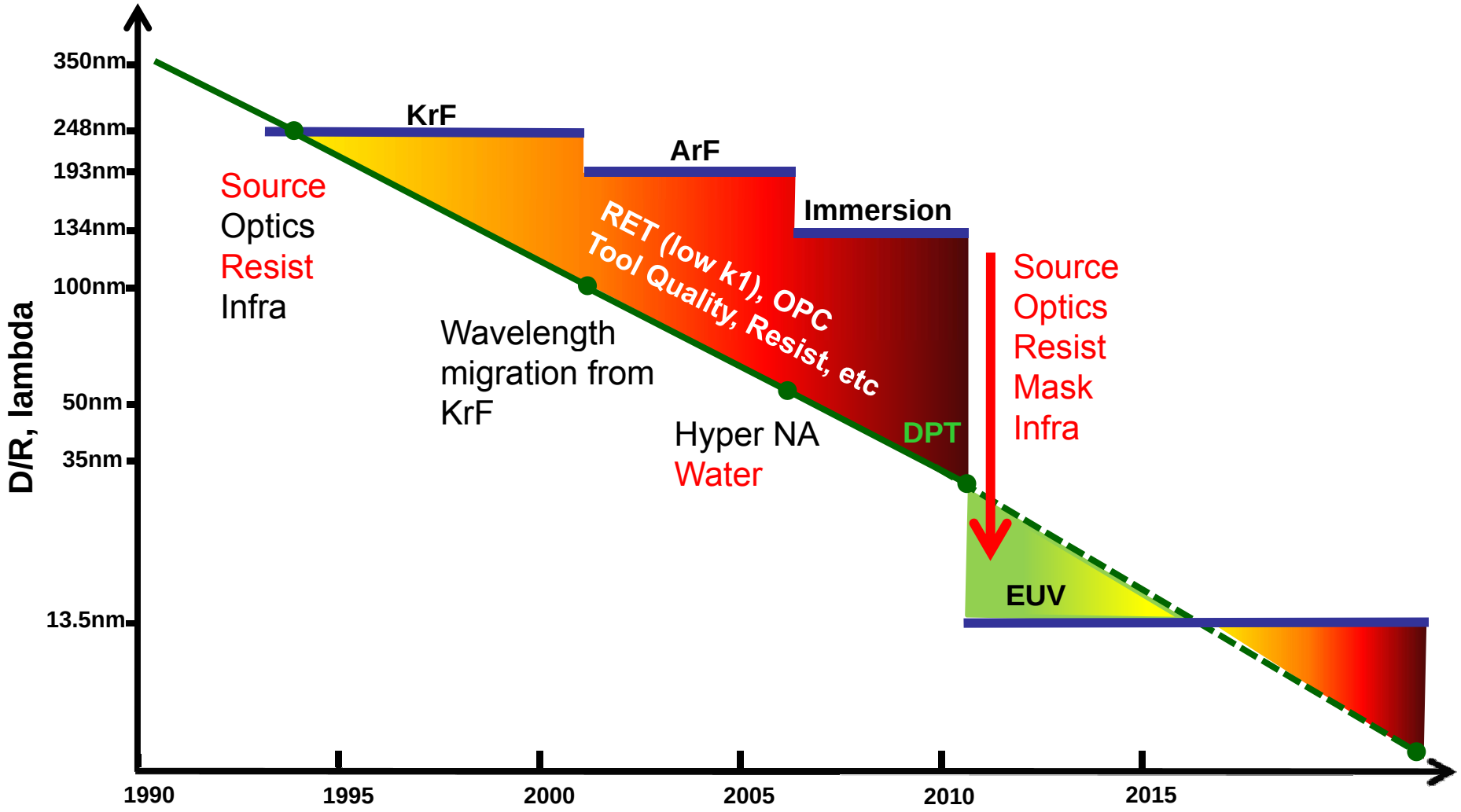
Jeong-Ho Yeo
Samsung Electronics Co., LTD.

Contents

- Litho Scaling History & Outlook
- EUVL Challenges
- Memory Device Scaling
- EUVL Full Field Performance
- EUVL & Memory Roadmap
- Conclusion

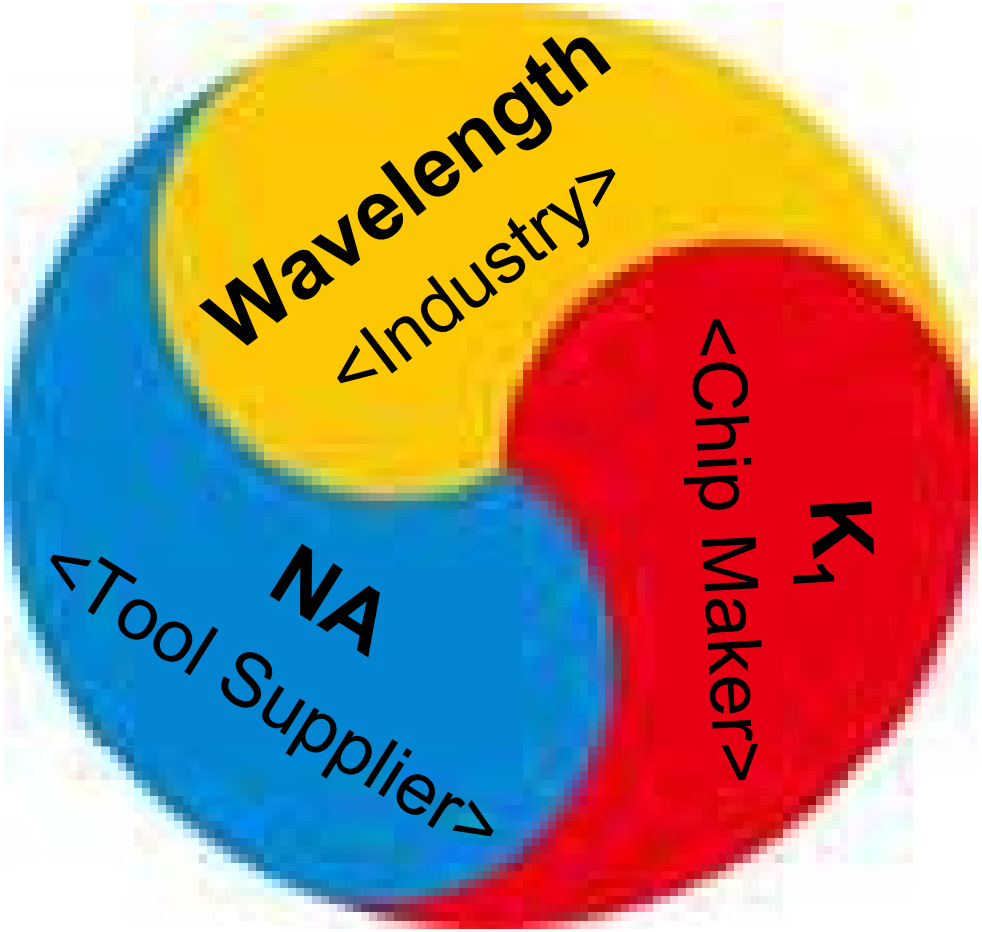
Litho Scaling History & Outlook

Continuous scaling on wavelength, NA and K_1



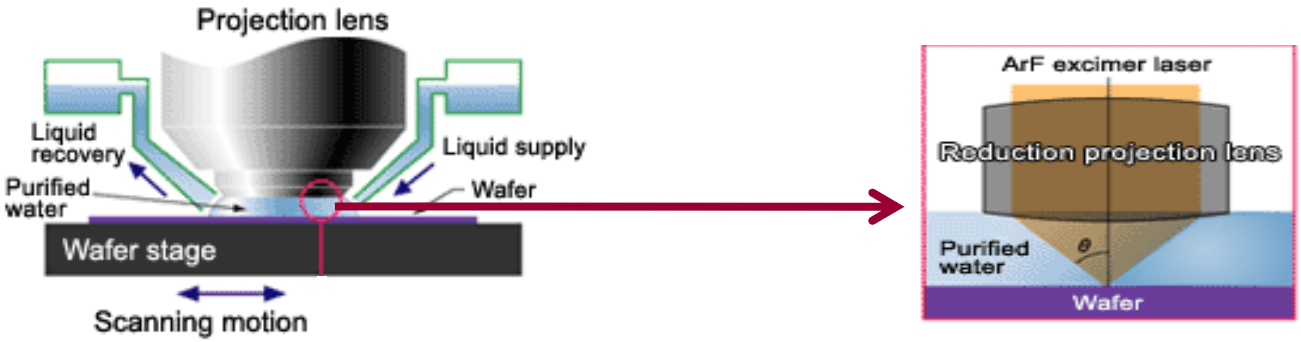
Scaling Challenges

Scaling through recycling of wavelength, NA & K_1

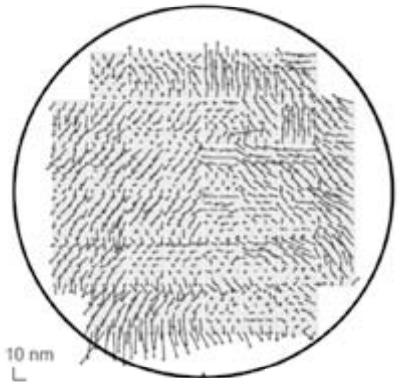


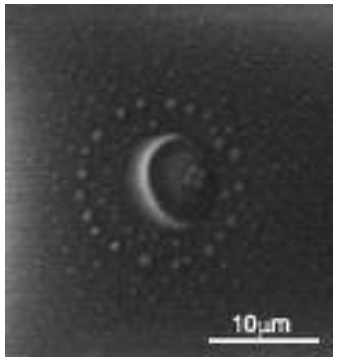
From Dry to Wet

- NA Scaling



- However, challenges were
  - Overlay control
  - Defect





From Wet to Vacuum

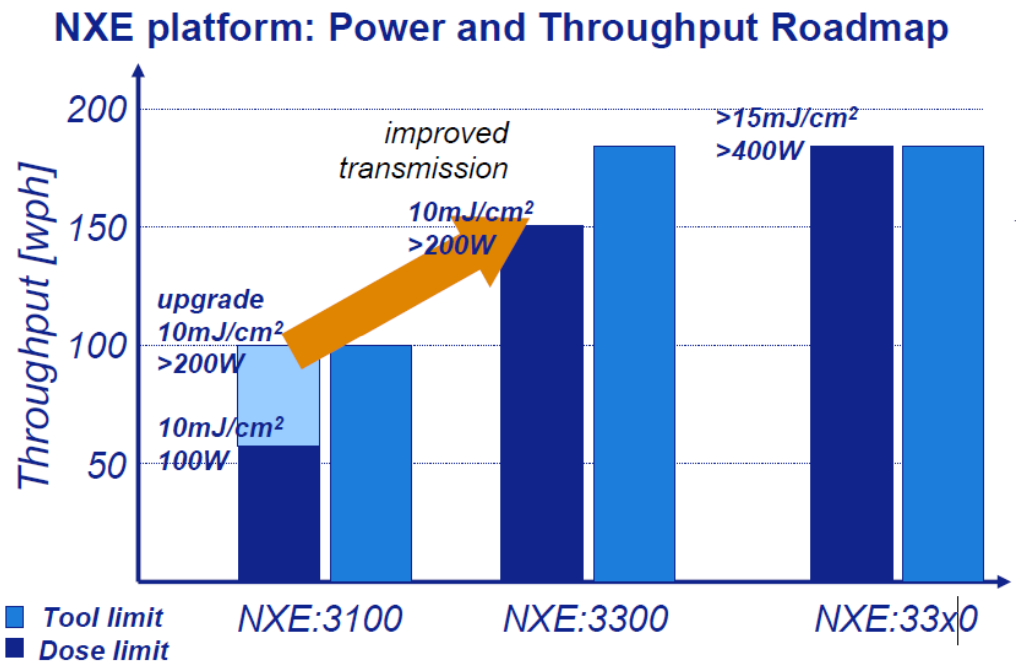
SAMSUNG DIGITall everyone's invited

- Wavelength Scaling
  - However, there are many challenges on industry wide

2003	2004	2005	2006	2007	2008
Source Power	Defect Free Mask	Resist Resolution	Source Power	Source Power	Source Power
Defect Free Mask	Collector Lifetime	Collector Lifetime	Resist Resolution	Resist Resolution	Defect Free Mask
Reticle Protection	Resist Resolution	Defect Free Mask	Defect Free Mask	Defect Free Mask	Resist Resolution
Collector Lifetime	Reticle Protection	Source Power	Reticle Protection	Reticle Protection	Reticle Protection
Resist Resolution	Source Power	Reticle Protection	Optics Quality	Optics Quality	Optics Quality
Optics Quality	Optics Quality	Optics Quality			

7th International EUVL Symposium Program Steering Committee. Lake Tahoe, October 1, 2008

Challenges in EUV Source



Timing
T'put >150 WPH
Source should be delivered by 2012

Reliability
MTBF should be longer than Excimer laser

CoO
Power consumption, SoCoMo lifetime, etc

Challenges in EUV Mask

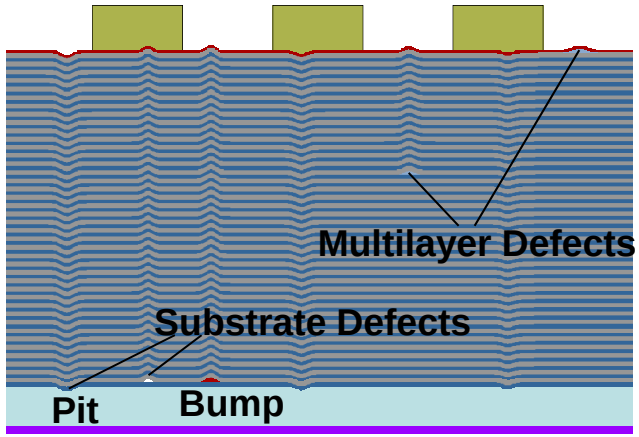
Availability of Defect-Free EUVL Mask

Achieving zero defect for EUVL masks in the next few years is extremely challenging.

Blank's Defect Level required for HVM
< 0.003/cm^2 @25nm

Large GAP

Current Status (2009)
~ 1/cm^2 @18nm



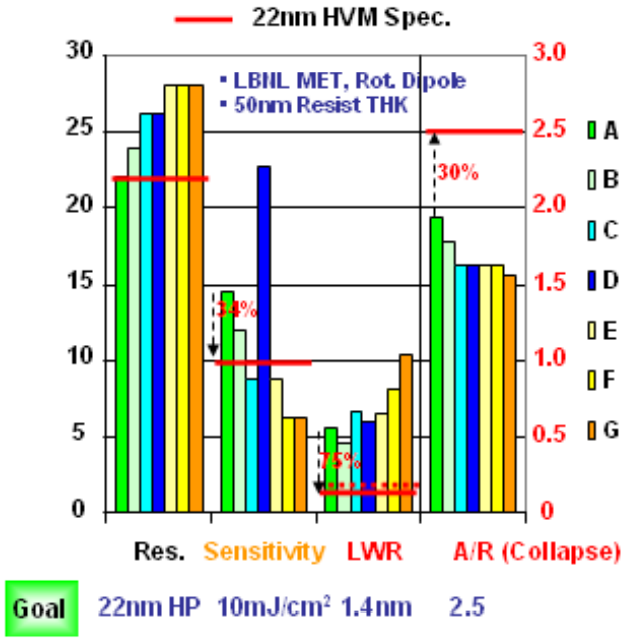
Defect free blank	Blank inspection	Pattern inspection	Tentative solution
Collaborate with supplier	DUV Inspection Actinic Blank Inspection Actinic Defect Review	DUV Inspection Actinic Pattern Inspection Actinic Defect Review	Layout Disposition Wafer inspection

Industry wide collaboration is required.

Challenges in Resist

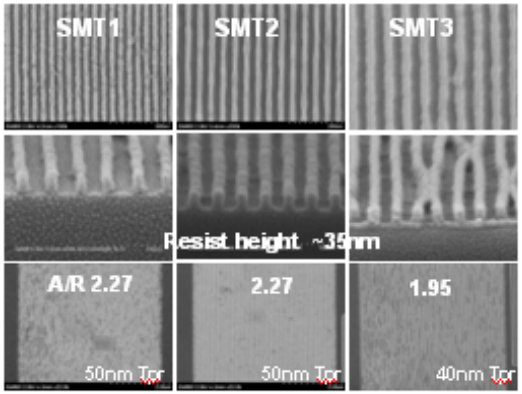
Challenges and Priorities for 22nm HP resist

Pattern Collapse (Resolution) > LWR > Sensitivity



▪ Key Gaps for 22nm HP Patterning

1. Resist Collapse (30%)
2. Resolution (10%)
3. LWR (75%)
4. Pattern transfer with thin resist (35nm remained resist pattern height with 50nm coating resist thickness)
5. Defect (*Bridge/ Scum*)
6. Sensitivity

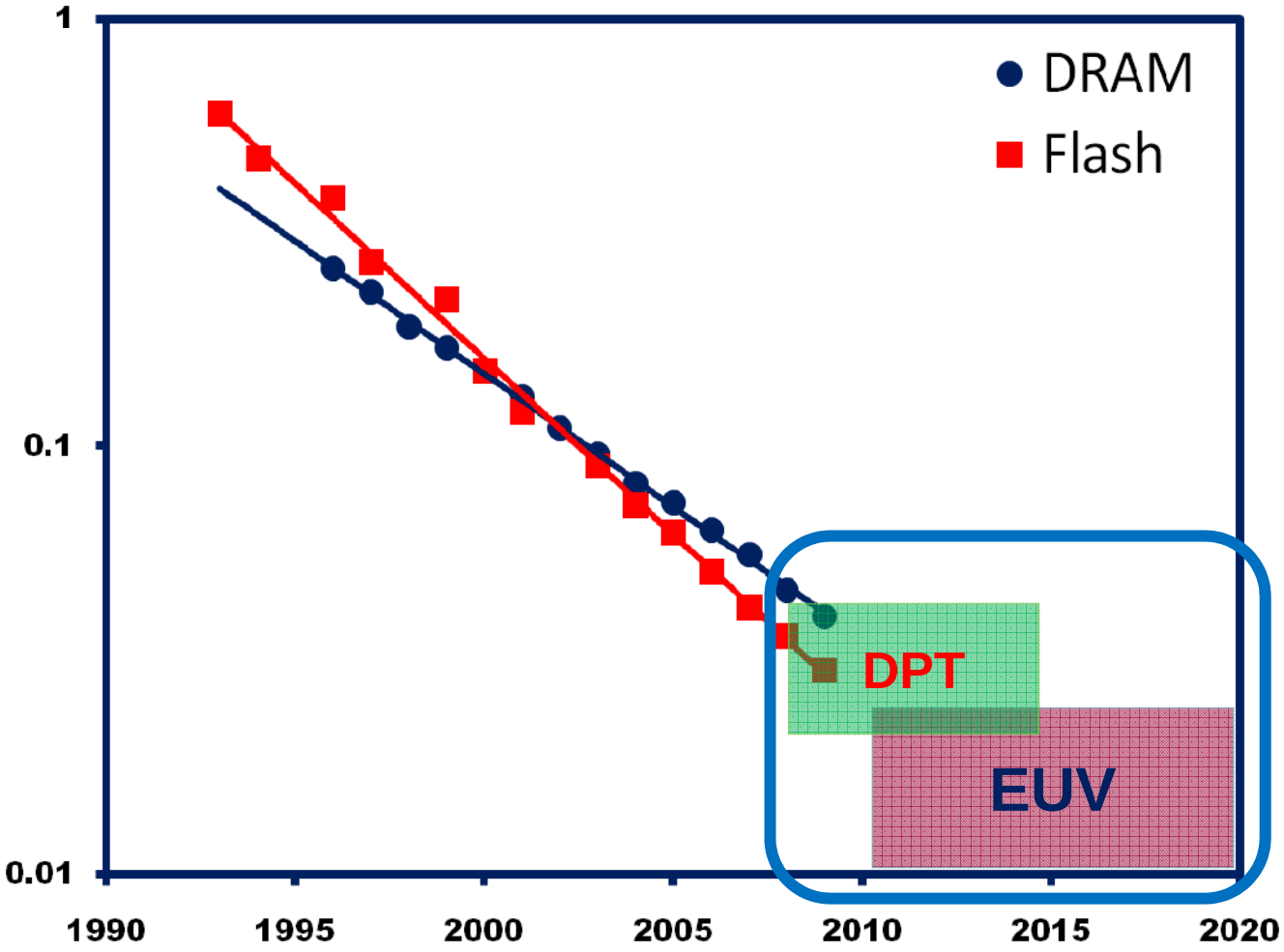


EUVL Symposium 2009, C.Koh, et al

Litho material breakthrough is required.

Memory Device Scaling

Memory Device Scaling will be continue with DPT & EUV



Near Future Scaling

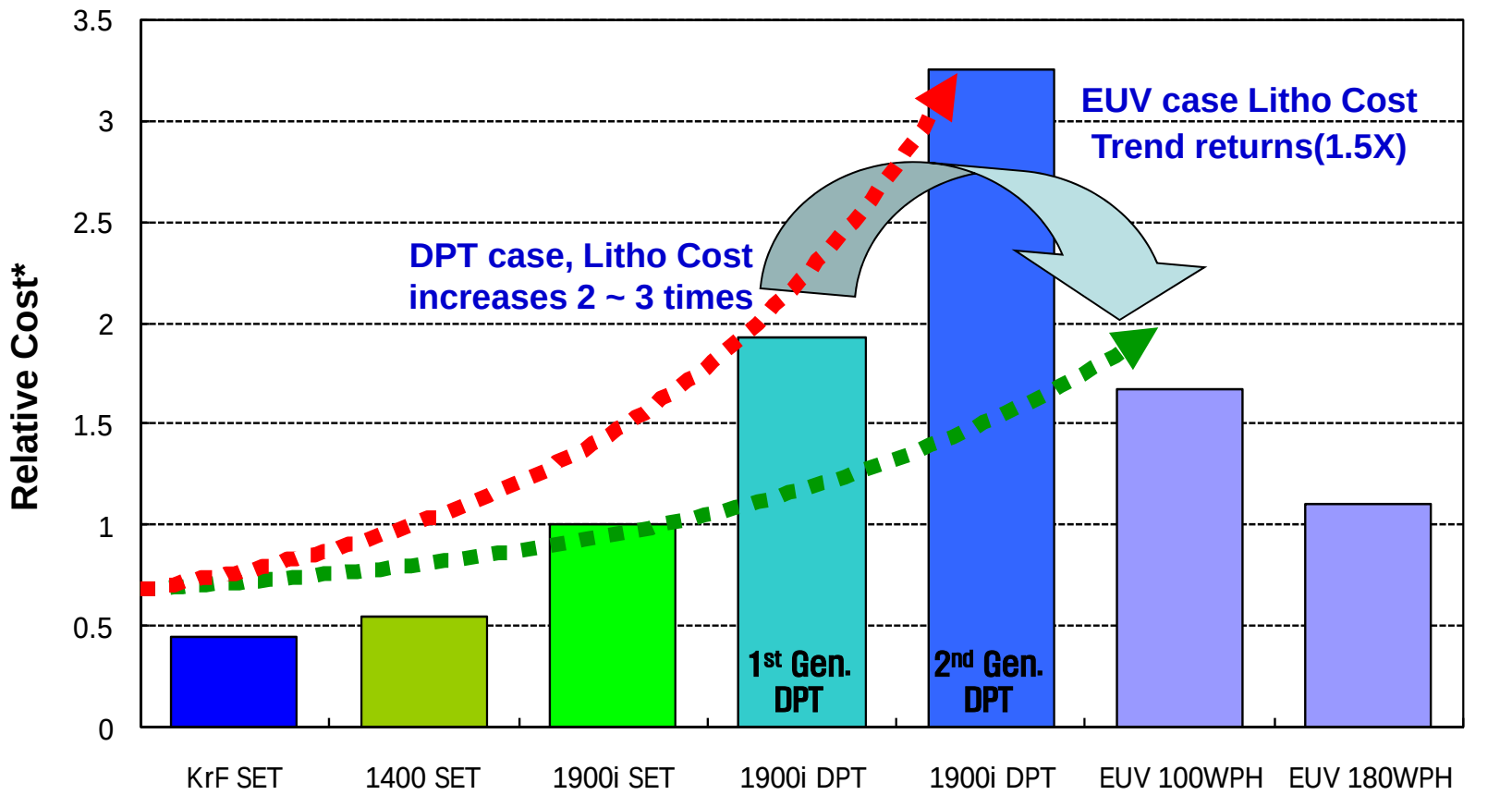
- DPT vs. EUV

Consideration	EUV	DPT
Technical Challenges	High	Low
Sub-20nm Extendibility	Yes, but many technical hurdles	Conceptually Yes, Practically ?
CoO	Good if high TPT can be achieved	Bad with new investment
Timing	Challenging	Exist

- Below 22nm HP, EUV might be only solution
- If EUV would not be available, other way is required to develop to continue CMOS scaling

Litho CoO Analysis

Litho Cost Trend returns to normal with > 100WPH



* Cost per Wafer

EUV Success Criteria

- EUVL success criteria for Memory
  - Throughput (> 150WPH) with reasonable CoO
  - Timing (2012)
  - K_1 Scalability

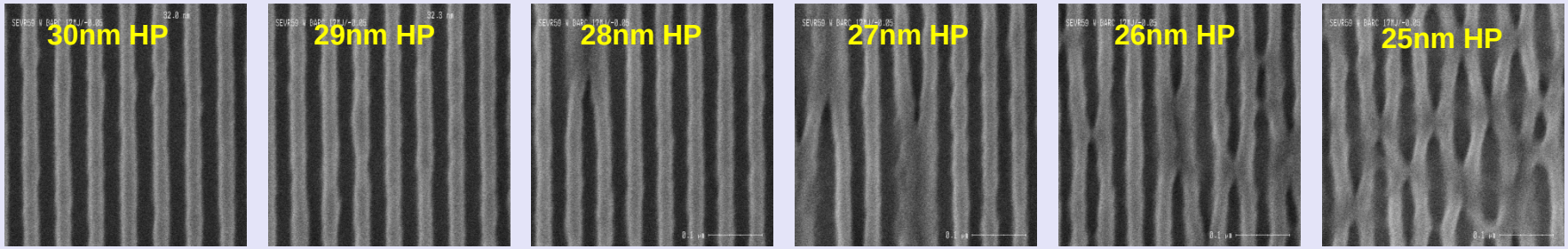
Full Field Performance

Result – ADT Resolution

SAMSUNG DIGITall everyone's invited™

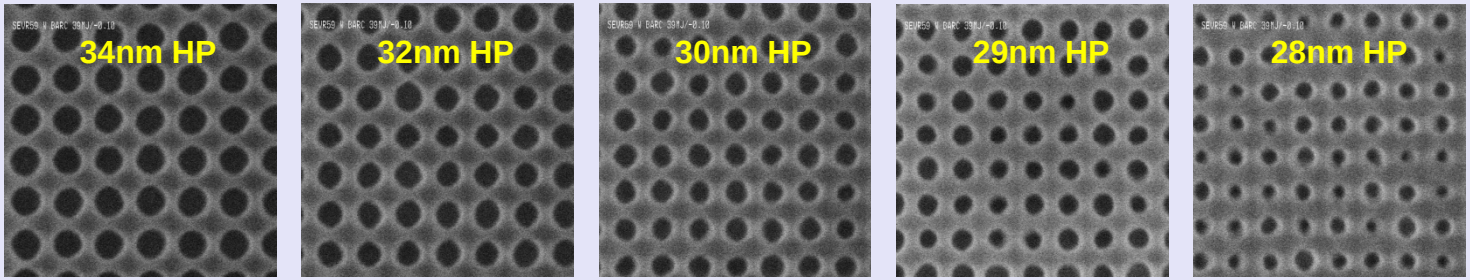
Sub 27nm HP L/S pattern was successfully defined.

Solution for pattern collapse should be delivered.



32nm HP C/H pattern was successfully demonstrated.

CD Uniformity improvement is required.



Resist Thickness: 65nm
Underlayer: 24nm

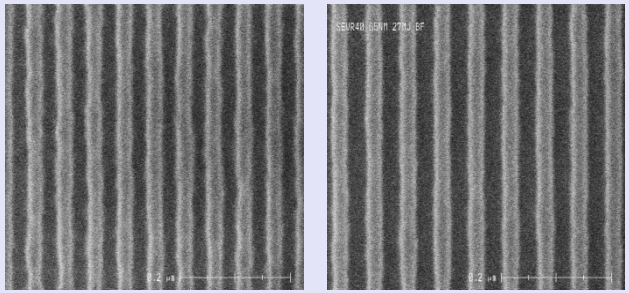
Summary of ADT Imaging

SAMSUNG DIGITall everyone's invited™

Stable 32nm HP patterning is proved with full field

Line & Space

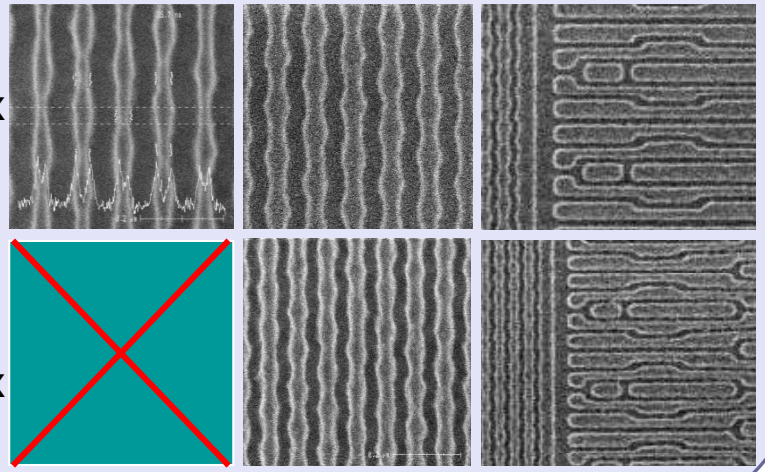
27nm HP **32 nm HP**



Imm. Cell **EUVL Cell** **EUVL Core**

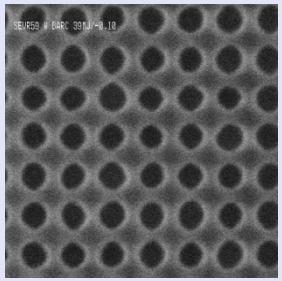
D3x

D2x



Contact

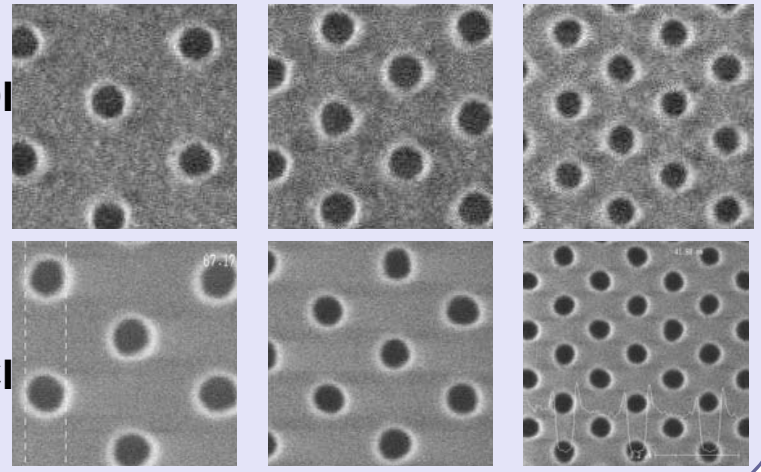
32 nm HP



D4x **D3x** **D2x**

ADI

ACI

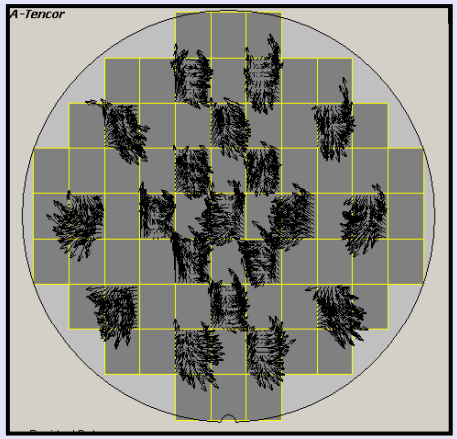


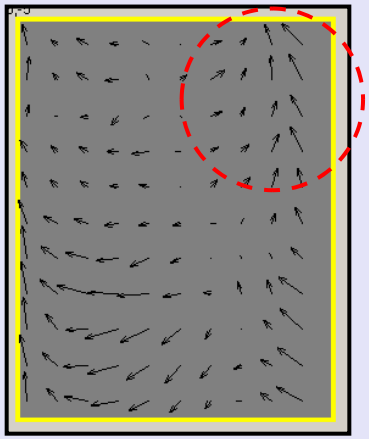
Result – MMO to ArFi

MMO shows similar results although ADT shows different shot distortion at upper right position.

ADT1

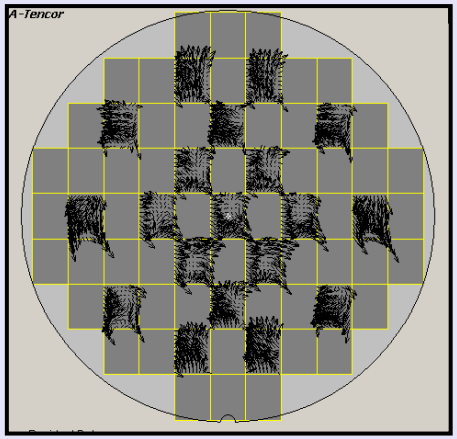
X	Y
15.0nm	17.3nm

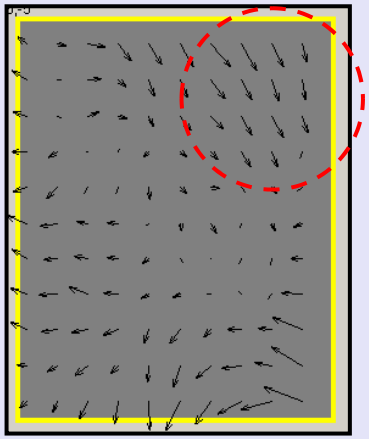




ADT2

X	Y
15.0nm	17.0nm

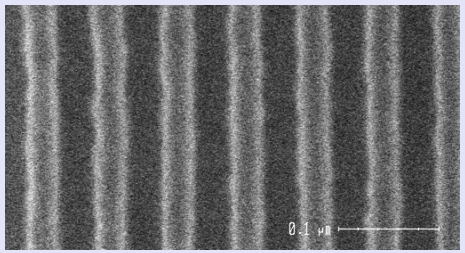
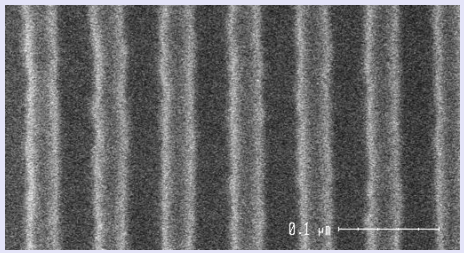
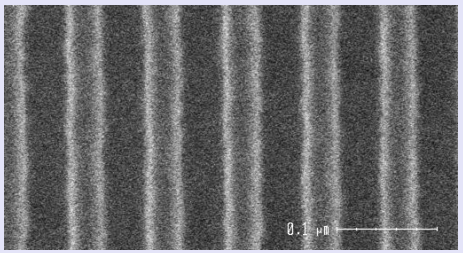
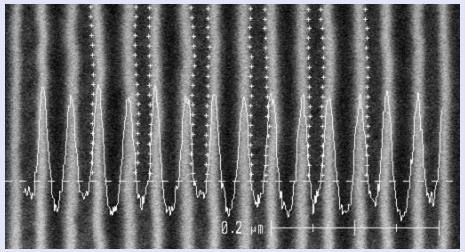
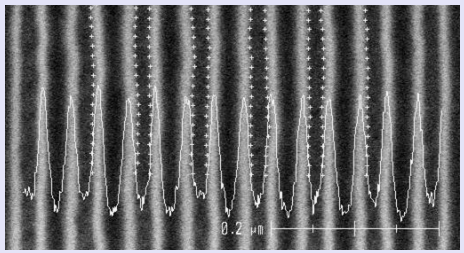
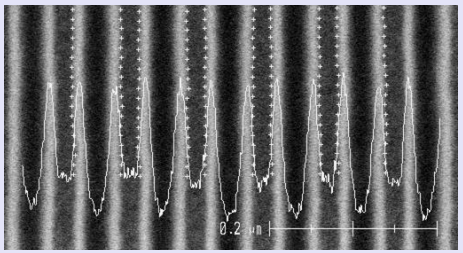
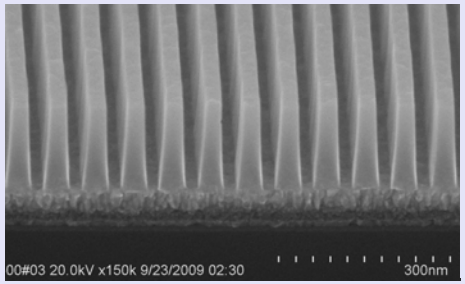
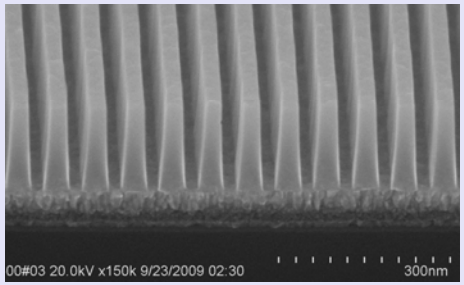
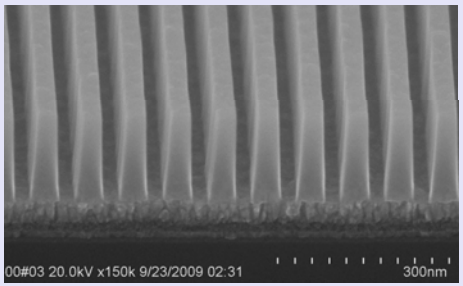




Result – Line & Space Etch

SAMSUNG DIGITall everyone's invited™

Successfully demonstrated pattern transfer of 32nmHP L/S

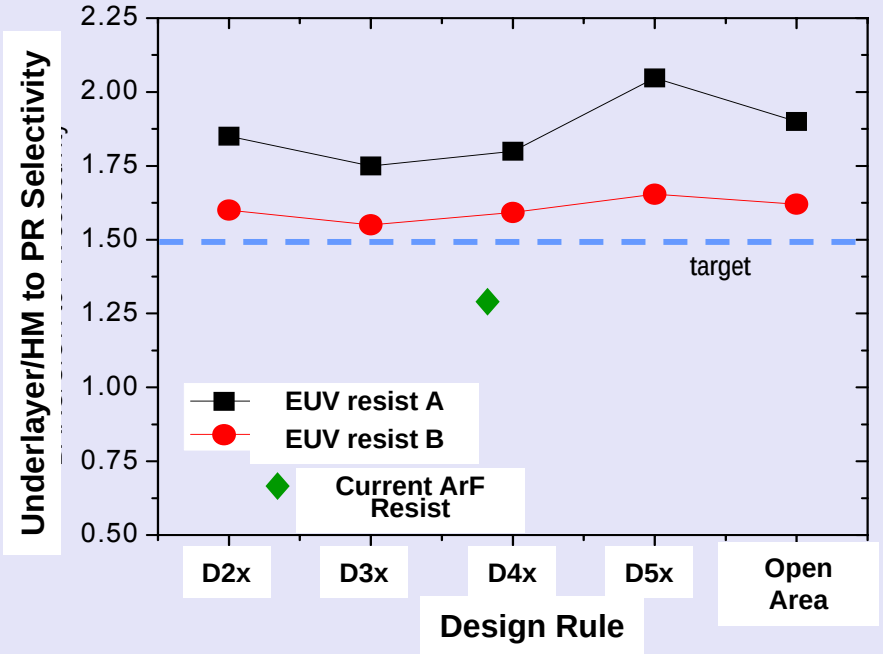
	HP 32nm	HP 34nm	HP 39nm
Resist Pattern			
Hard Mask tch (Top View)			
Hard Mask Etch (Vertical View)			

Result – Etch Selectivity

SAMSUNG DIGITall everyone's invited

EUV resists show higher selectivity than current ArF resist.

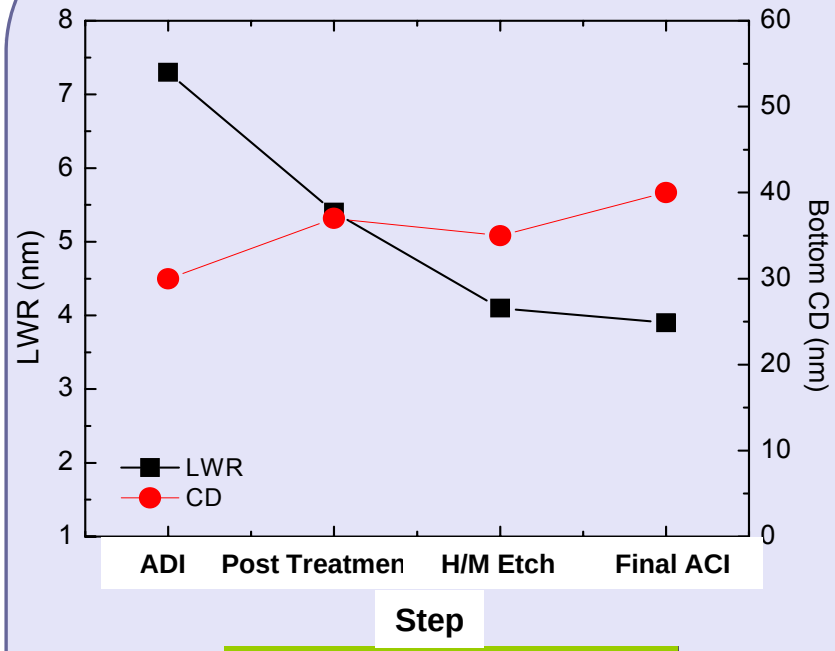
Etch Selectivity



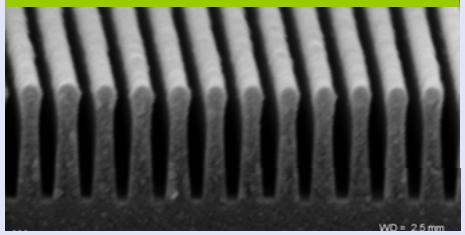
Underlayer/hardmask to EUV PR selectivity

	Target	Underlayer	Hardmask	Underlayer /Hardmask
Selectivity	> 1.5	1.8	2	1.9

LWR @ 30nm HP



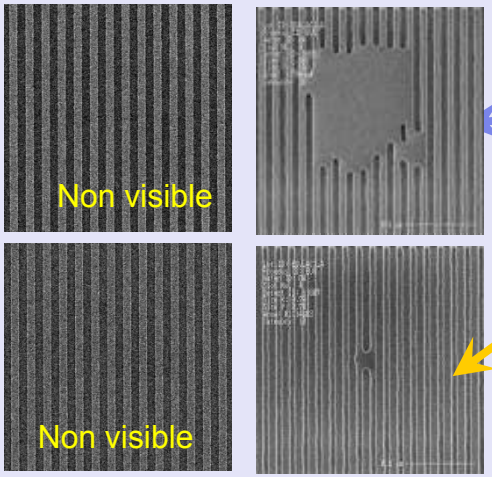
LWR 3.9nm



EUV Defect Study

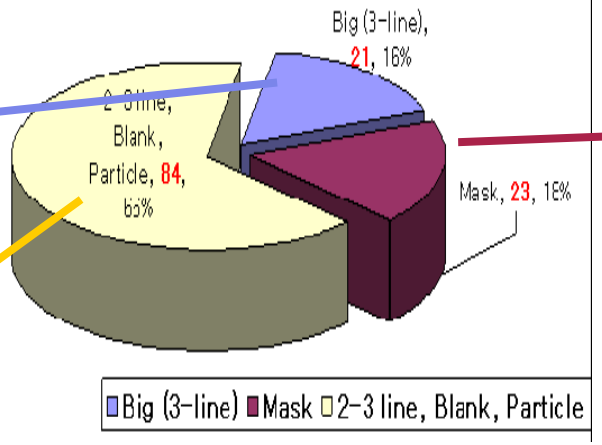
Type I

Mask Wafer



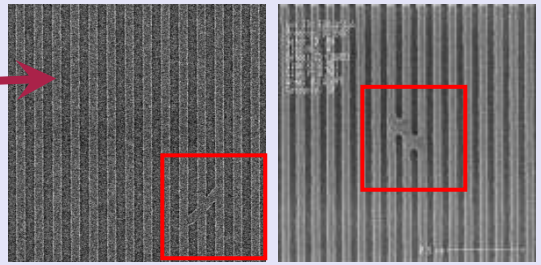
Phase Defect??

Defects caught by WPI reviewed on Mask



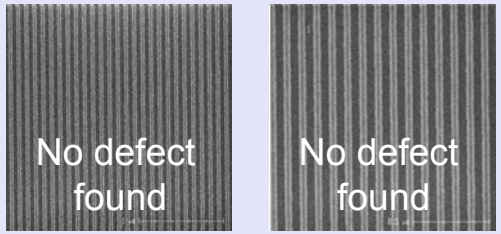
Type II

Mask Wafer



Mask Cleaning

2nd Exposure wafer



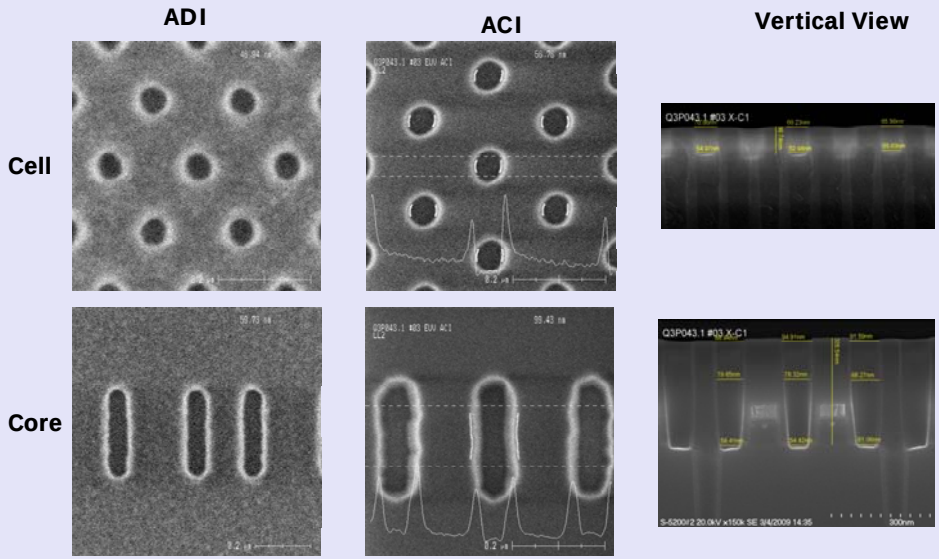
- Are type I phase defects?
- Type I defects were **<u>not found at the same position</u>** after: Mask cleaning → Expose → Review.
- Therefore, the source of type I defects seems to be from fallen particles during mask handling.

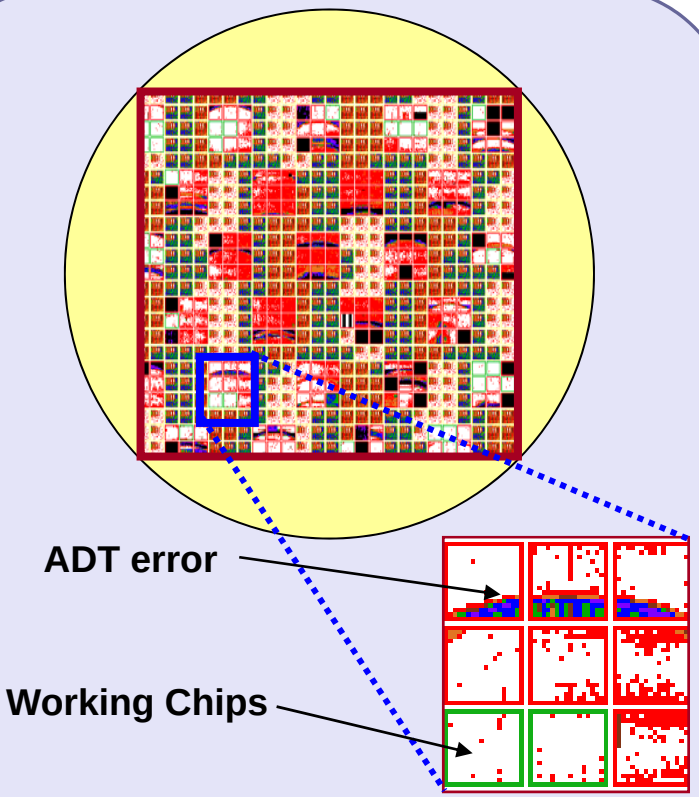
Result – DRAM Integration

SAMSUNG DIGITall everyone's invited™

4x DRAM contact layer was successfully integrated with EUVL

In-fab. monitoring result





* Check board Exposure due to ADT throughput issue

Conclusion

- Memory device scaling will be continue
  - Litho scaling should be supported with a technology

- Timing, Throughput (>150WPH), K1 scalability is Key for successful EUV introduction to memory production.

- ADT full field integration result shows promising EUVL capability even though there still remains lots of engineering challenges.

- Litho scaling should be continued.

Acknowledgement

We appreciate the support for ADT full field result to

- IMEC EUV Team
- SEMATECH EUV Team
- ASML EUV Support Team
- Samsung Mask Shop EUV Team
- Samsung R&D Pilot Process Development Team