

Future of Memory devices and EUV lithography

Hyeong Soo Kim

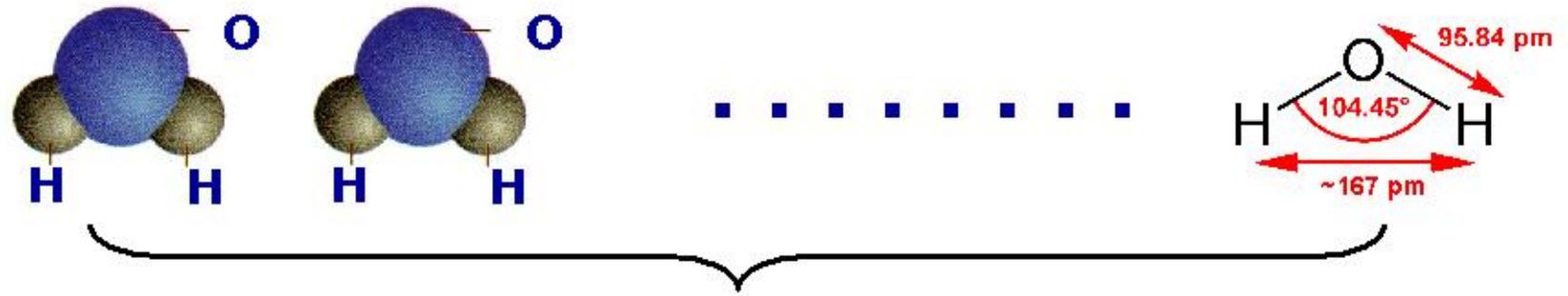
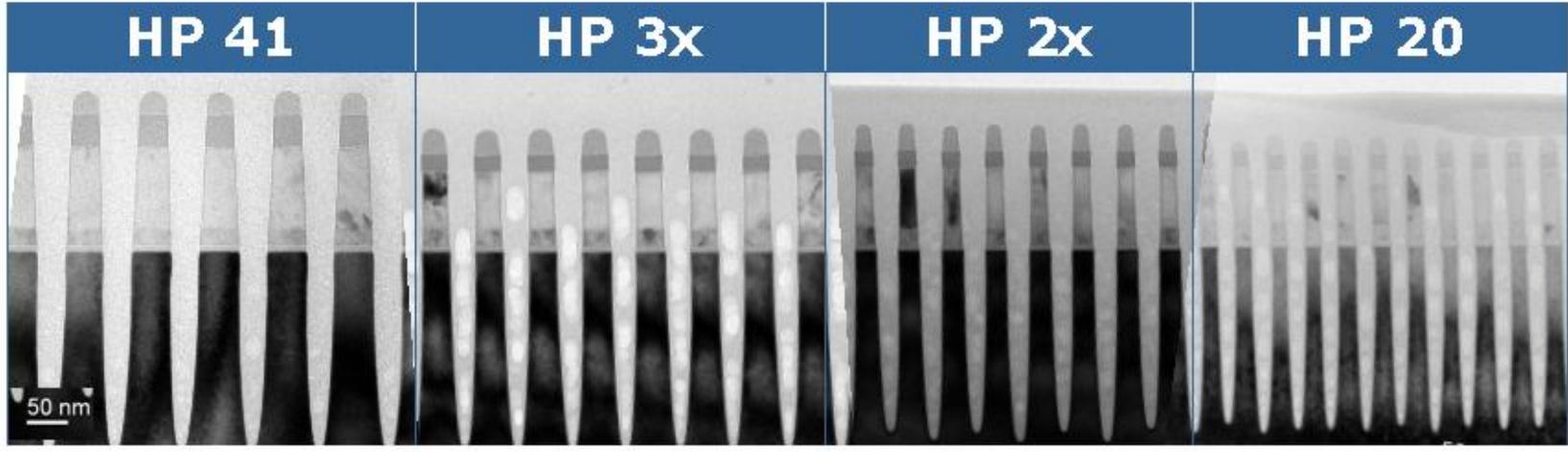
Hynix Semiconductor Inc.

Outline



- ❑ Demand for finer patterning continued
- ❑ What are candidates for future patterning ?
- ❑ Progress on major issues
 - Can EUV be ready in time ?
- ❑ Risks
- ❑ Summary

ArF SPT can be extended to 20nm HP

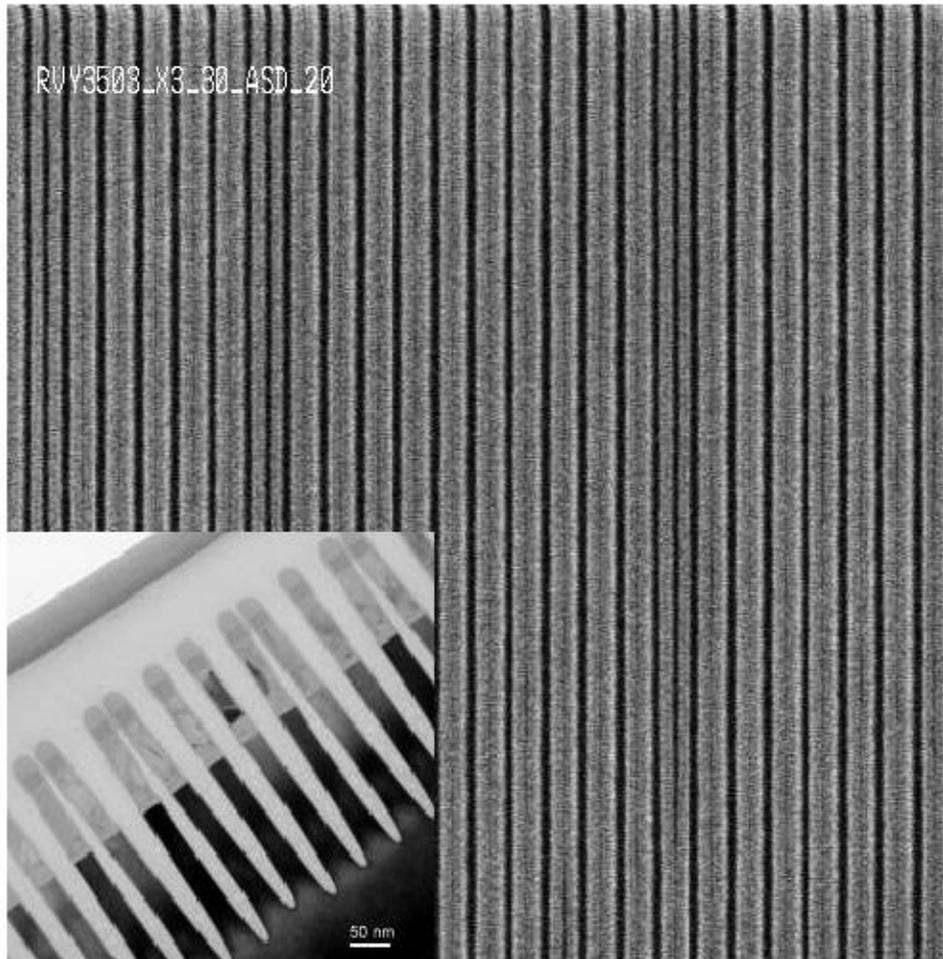


HP 20 nm = 125 molecules of H₂O

Patterning barrier over the resolution



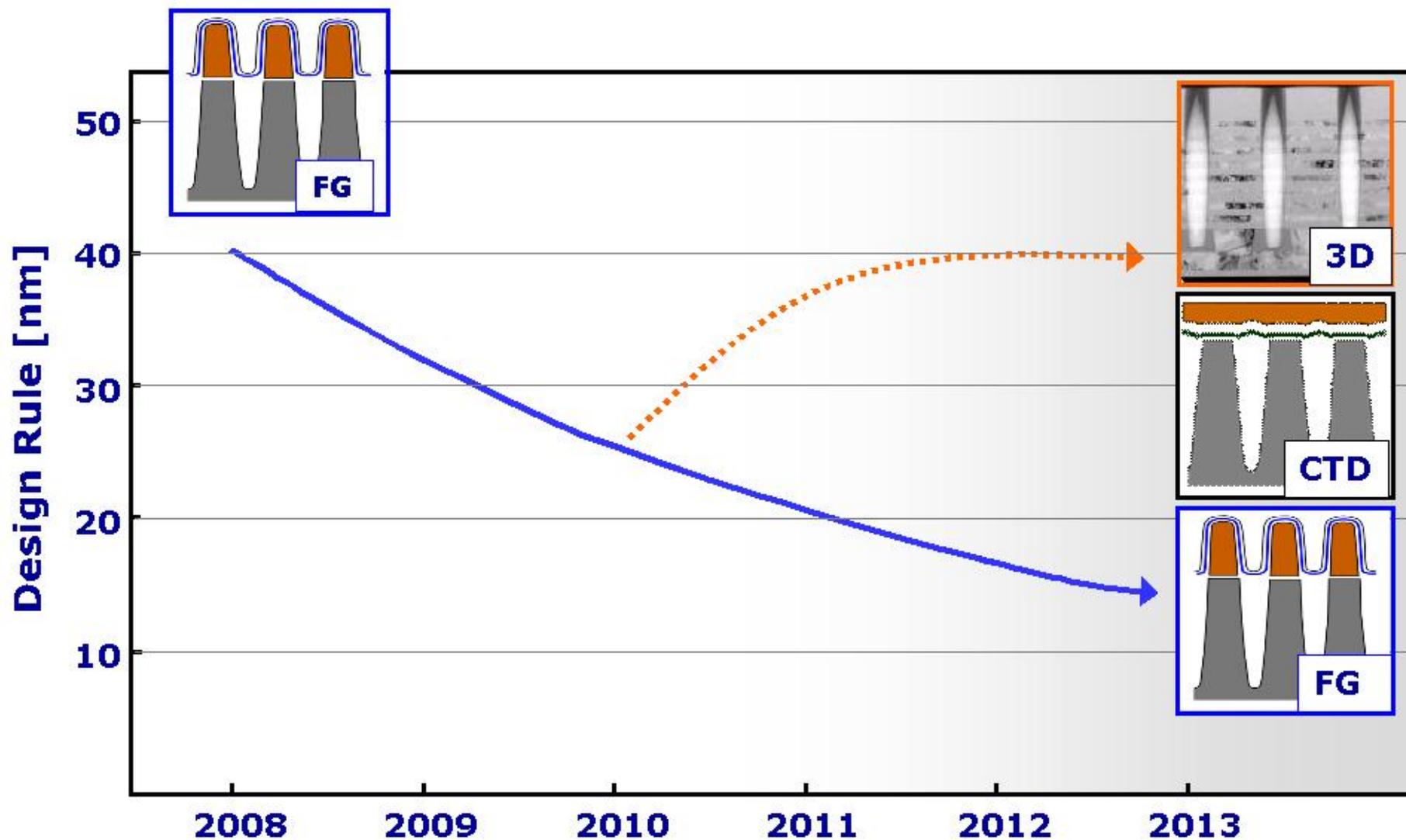
- High A/R pattern leaning during wet cleaning



If we don't figure out the collapse problem, then HP 20nm will be **the first hurdle** in developing HP 20nm and beyond

3D flash can relax design rule and avoid process difficulties

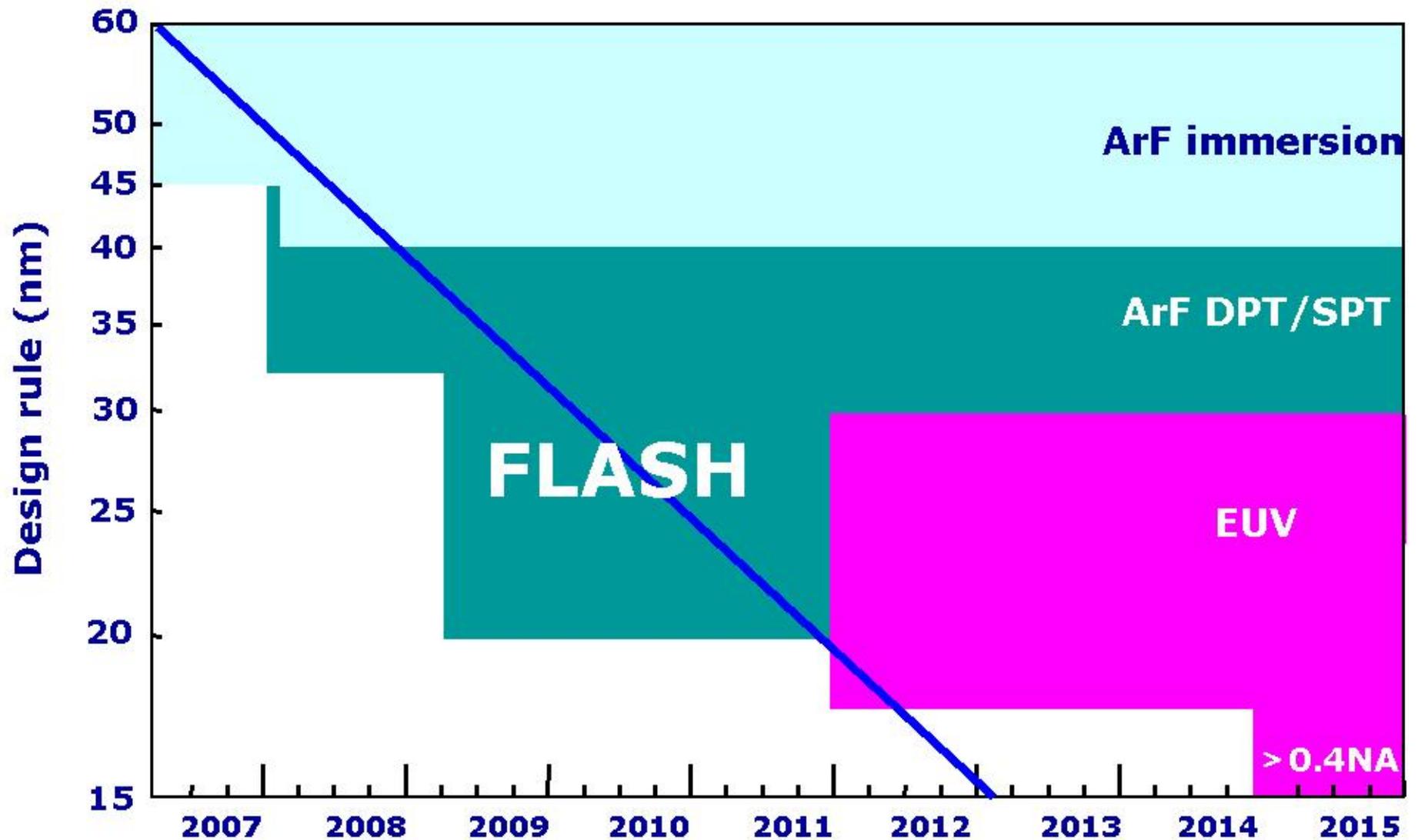
Pursue 20nm Planar and 40nm 3-D Flash



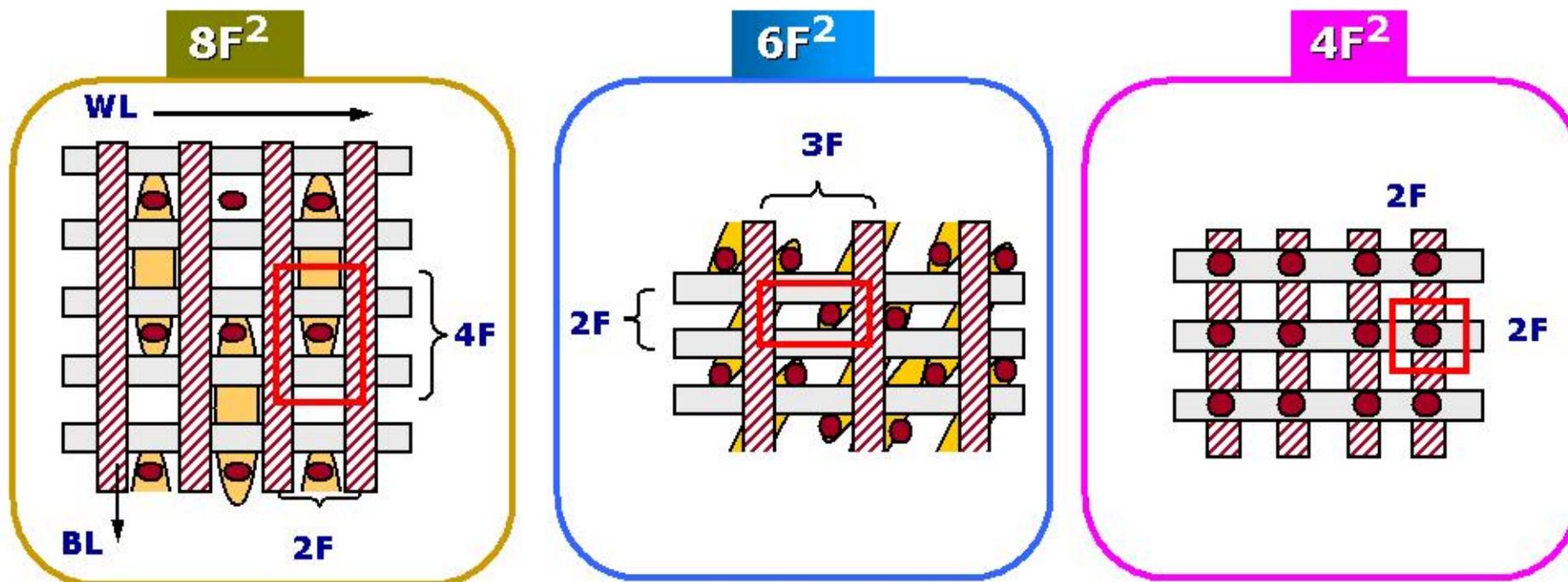
EUV mis-matches FLASH roadmap



EUV Symposium (2009, Oct.)



Design rule relaxed by architecture

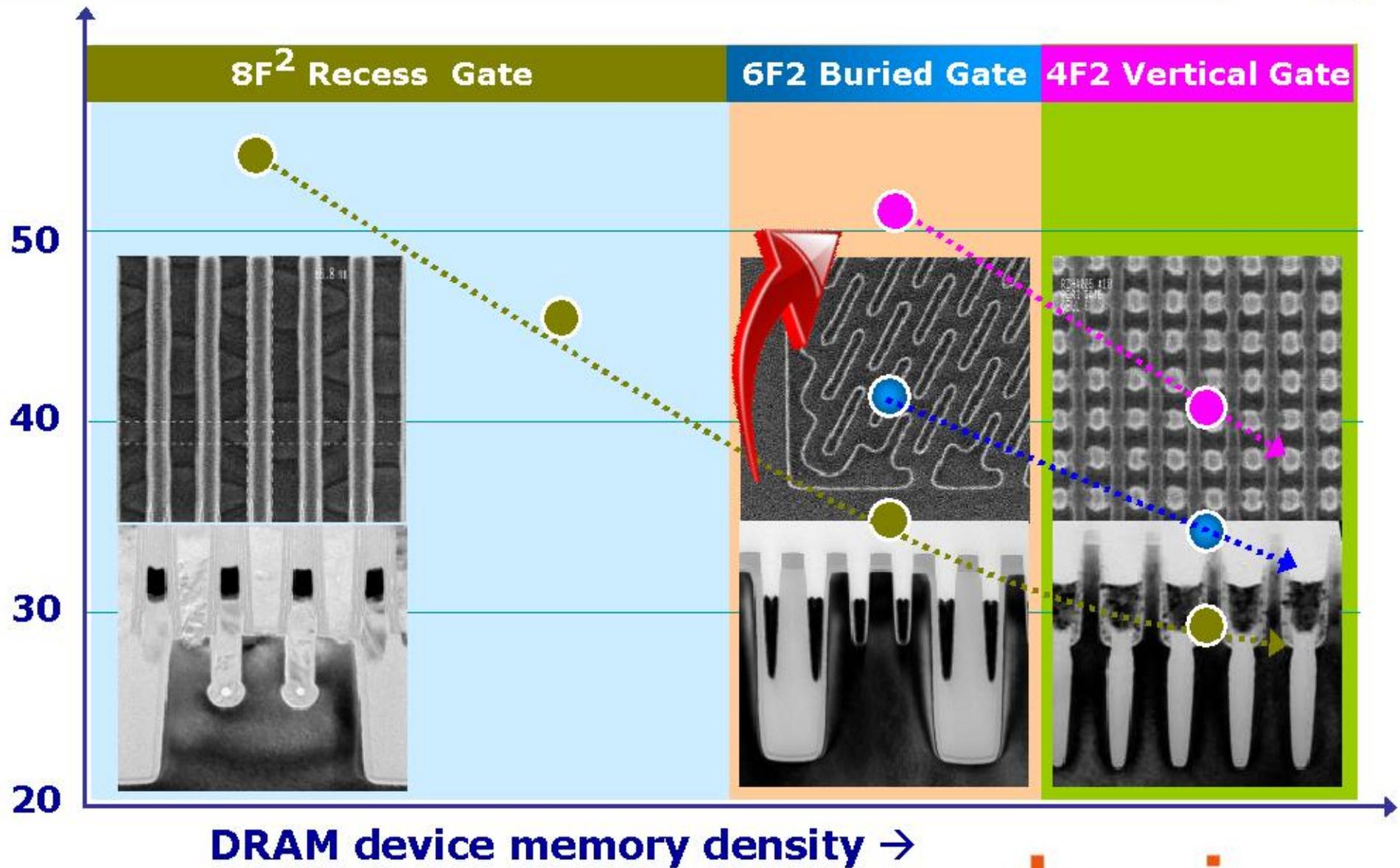


Pattern Size $\doteq 1 / \sqrt{k}$

where k is area factor 8, 6, 4

$8F^2$ 30nm \doteq $6F^2$ 35nm \doteq $4F^2$ 42nm if cell efficiency are same

Architecture Change in DRAM



Typical 6F2 DRAM Layout



Isolation

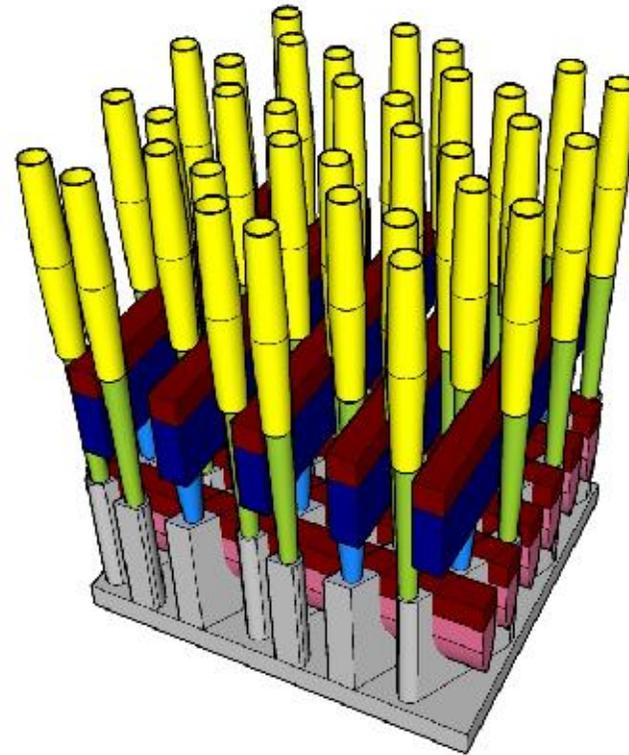
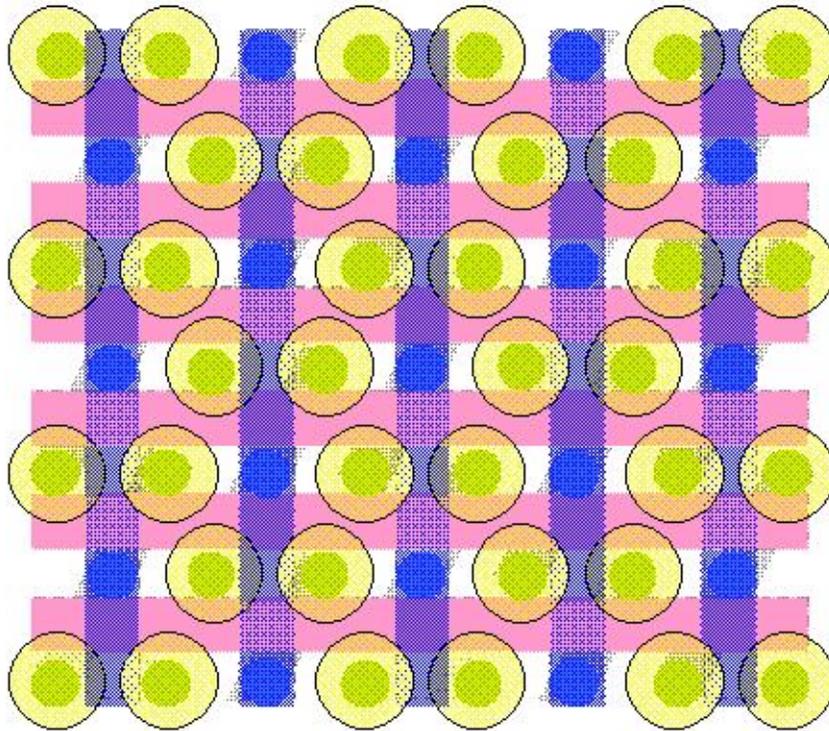
Gate Line

Bit Contact

Bit Line

Cell Contact

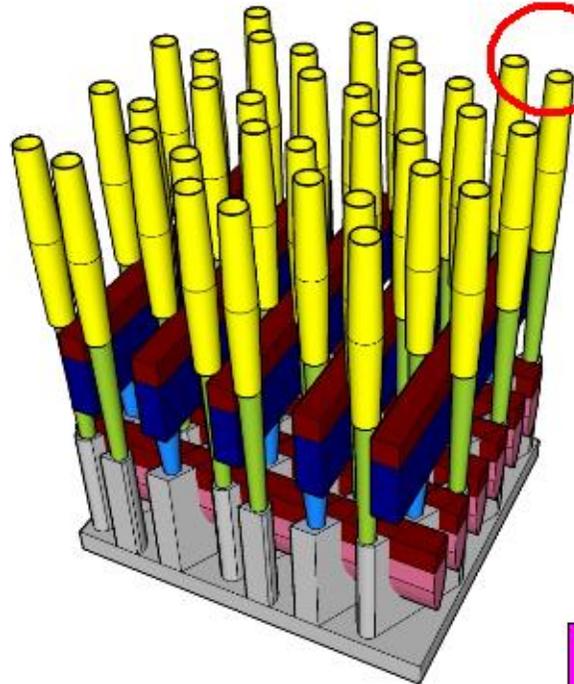
Capacitor



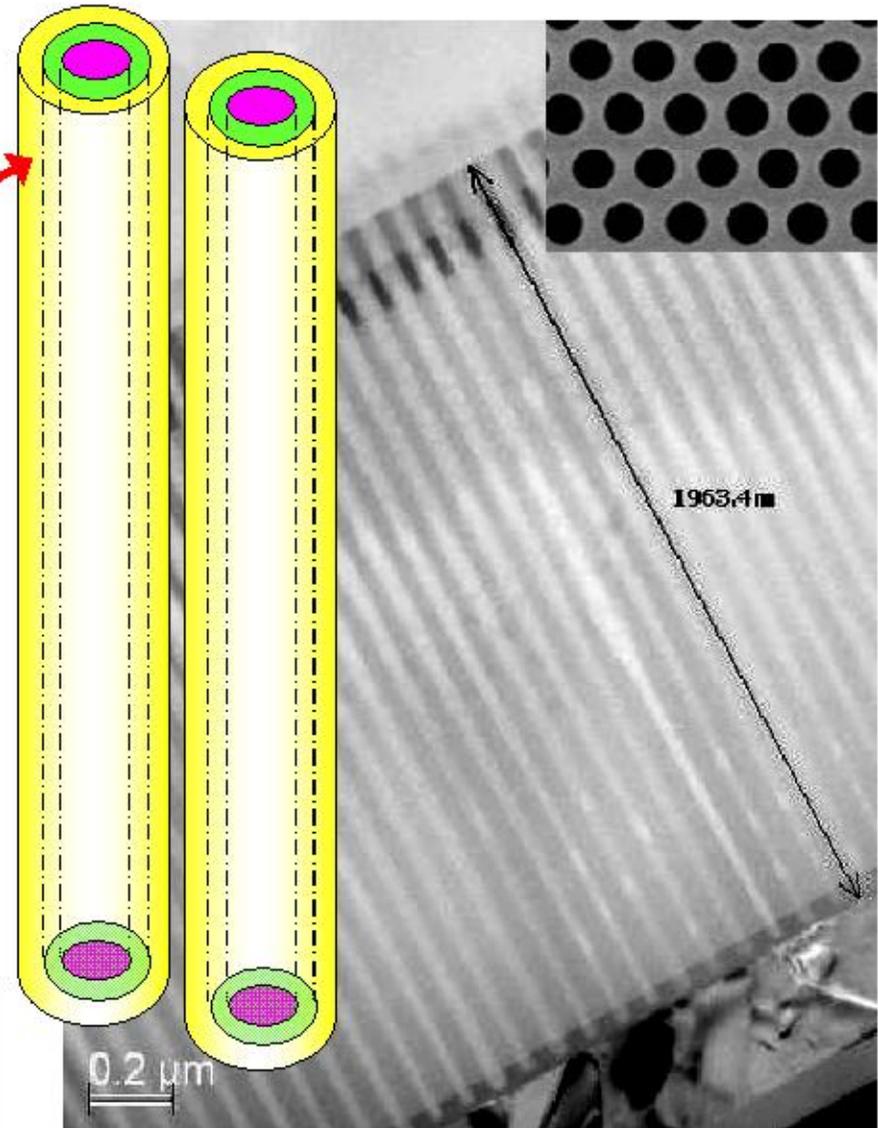
DRAM 3x nm, Capacitor Challenge !



- How to print HP 32nm contact hole pattern for DRAM 3x nm Storage Node ?



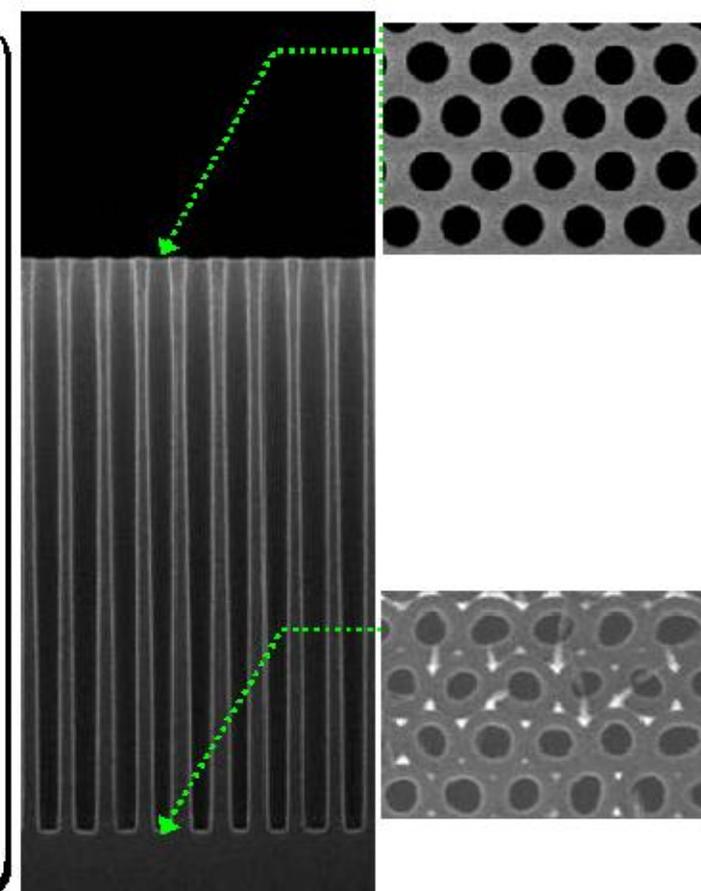
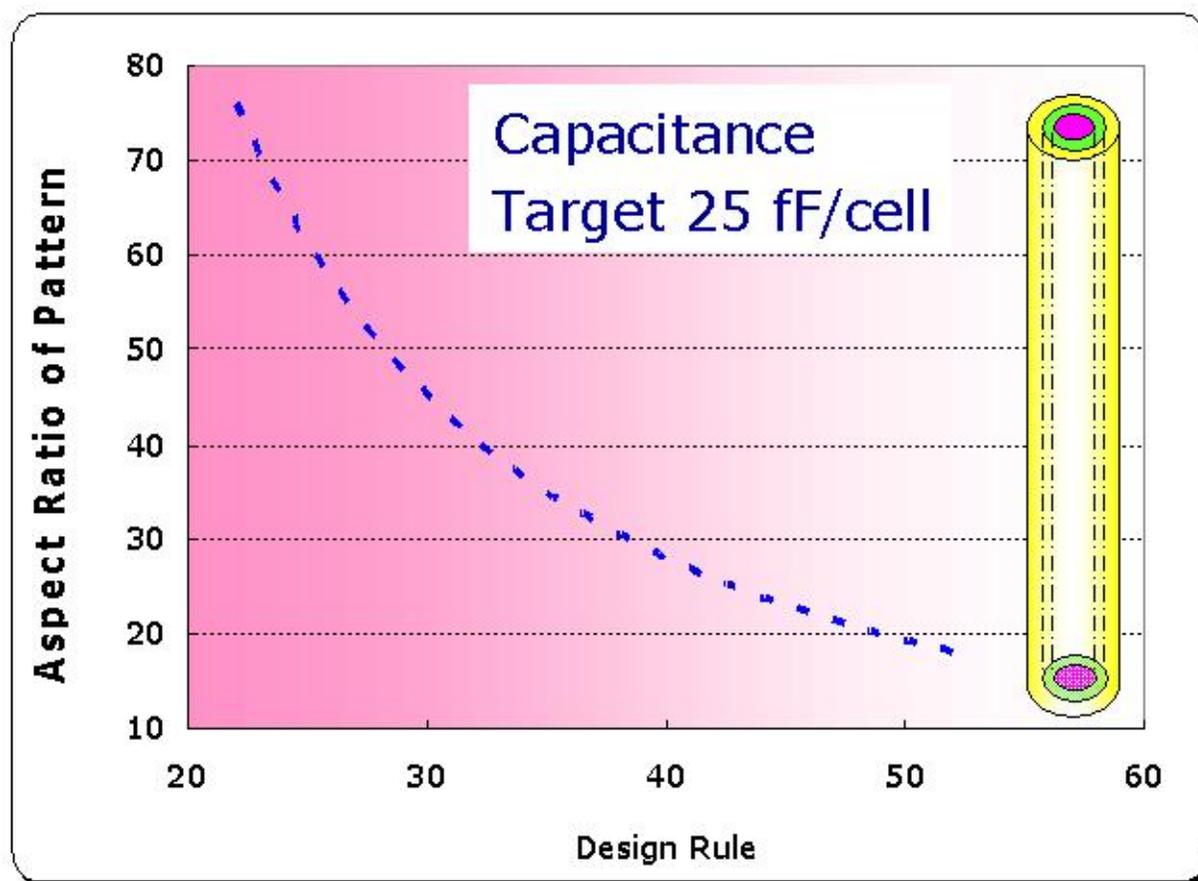
Bottom Electrode
CAP Dielectric
Top Electrode



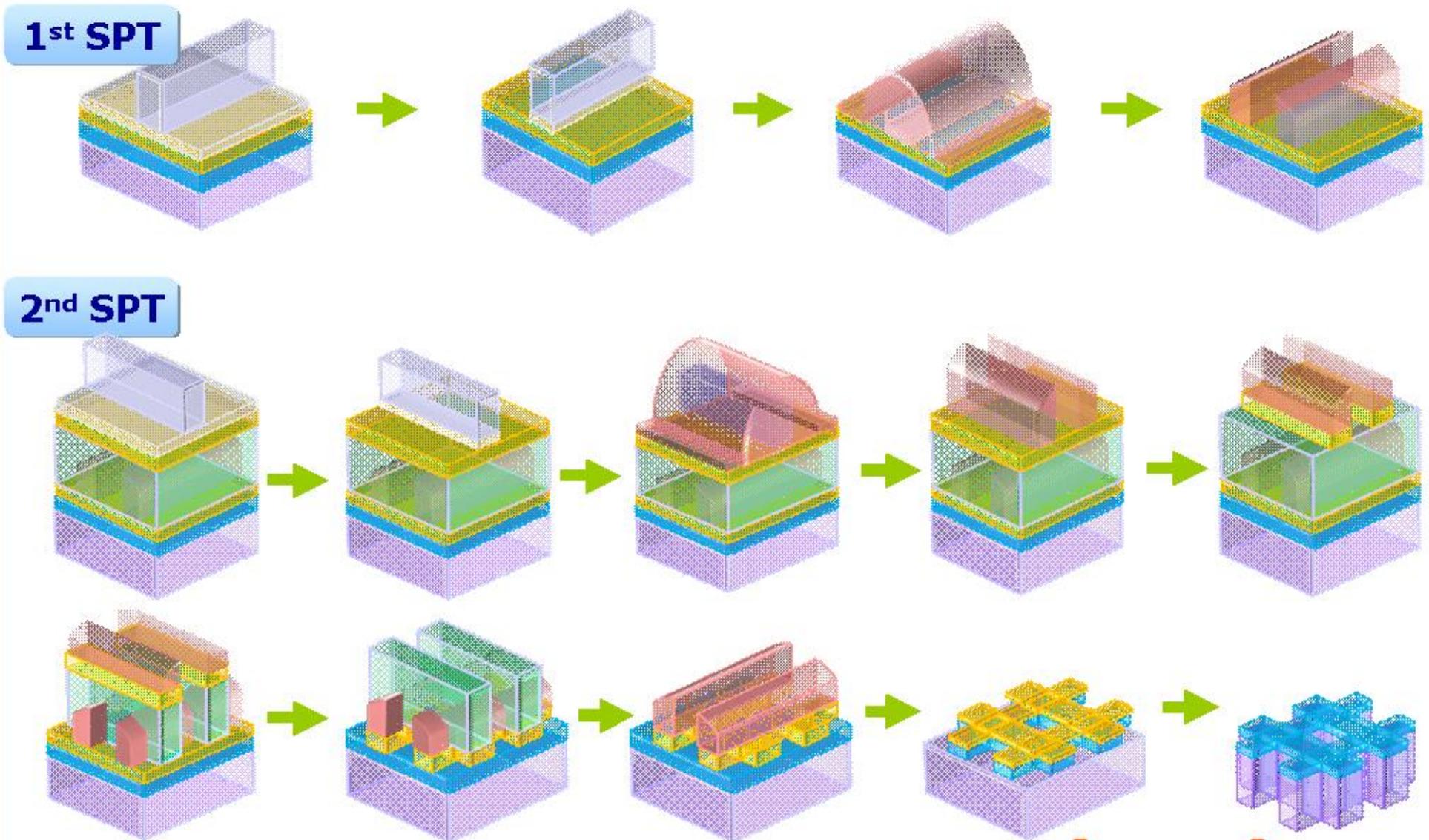
Capacitor Technology – Beyond 30nm?



- ❑ TiN/ZrO₂ capacitor can be extended up to 30nm device
- ❑ Need new high-k dielectrics and electrode beyond 30nm



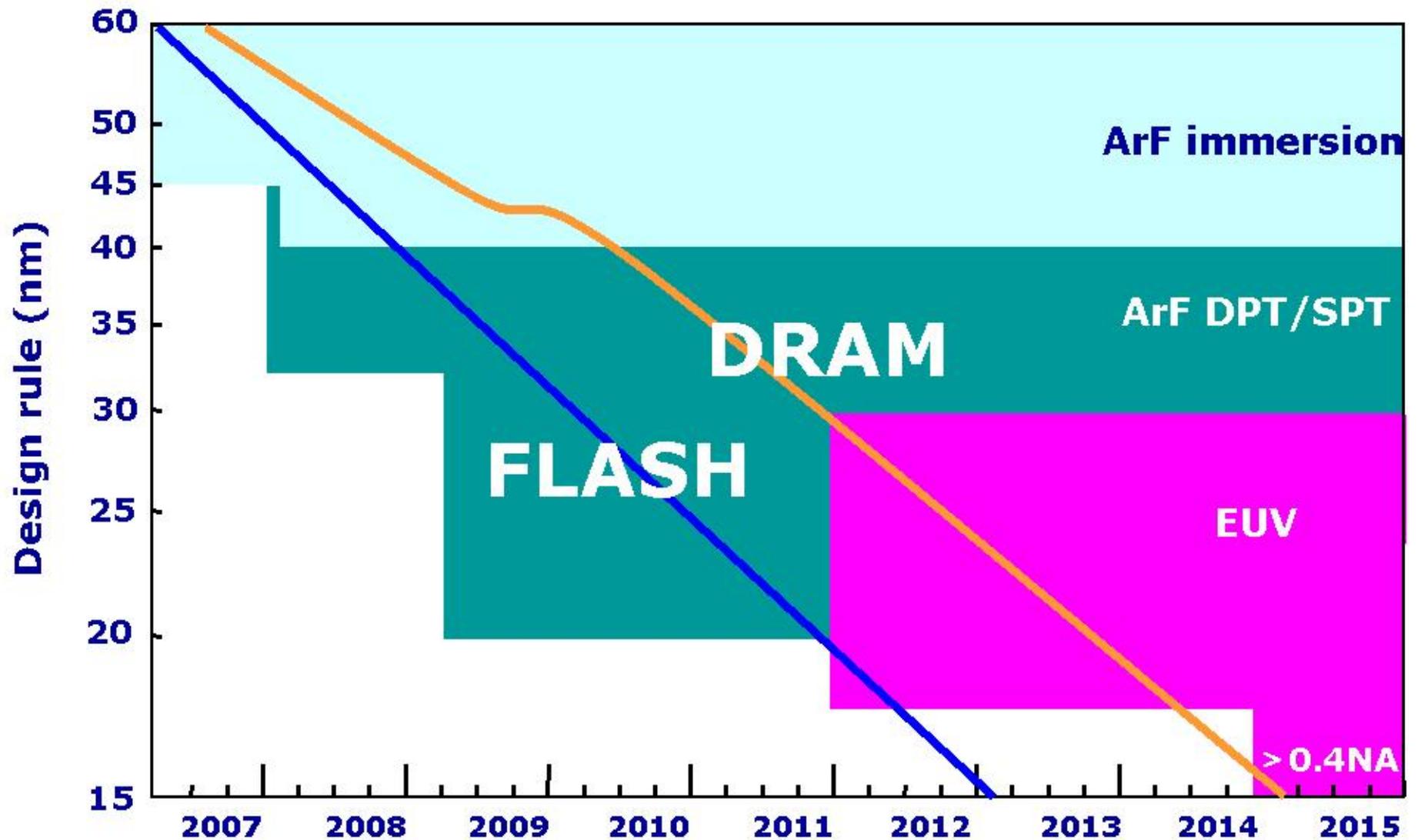
To get contact hole of HP 32nm with ArF



Roadmap & Lithography availability



EUV Symposium (2009, Oct.)



Demand for fine patterning continued



□ Flash

- ✓ Tech shrink will be continued until physical barriers are demonstrated fully or alternative is found
- ✓ EUV readiness will be too late and ArF SPT would be a viable option

□ DRAM

- ✓ Lithography will be the main factor together with capacitor issues
- ✓ Chance for EUV from sub-30nm node production in 2013 at least

Candidates for the future patterning



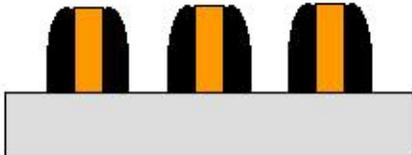
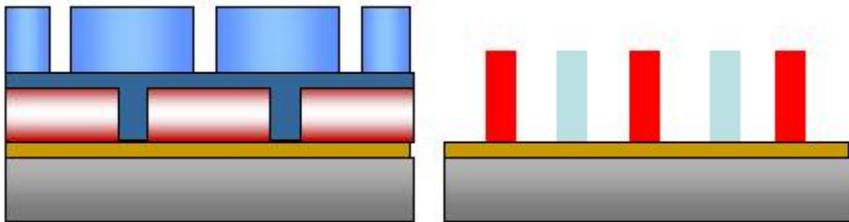
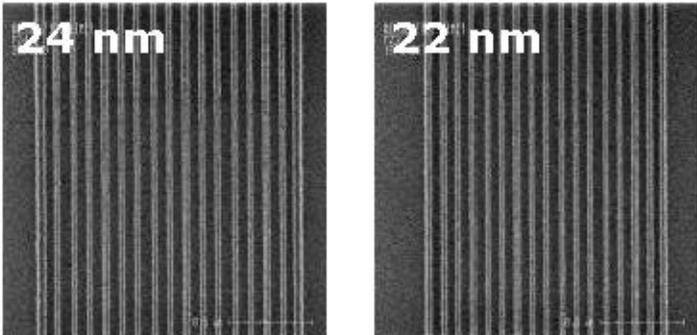
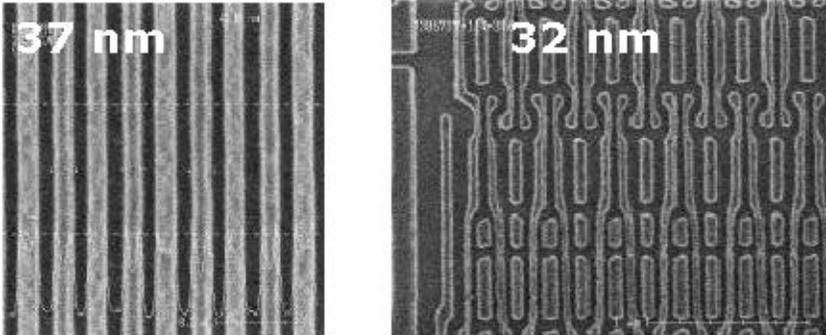
- Is that a real treasure hunt or just trace illusion?



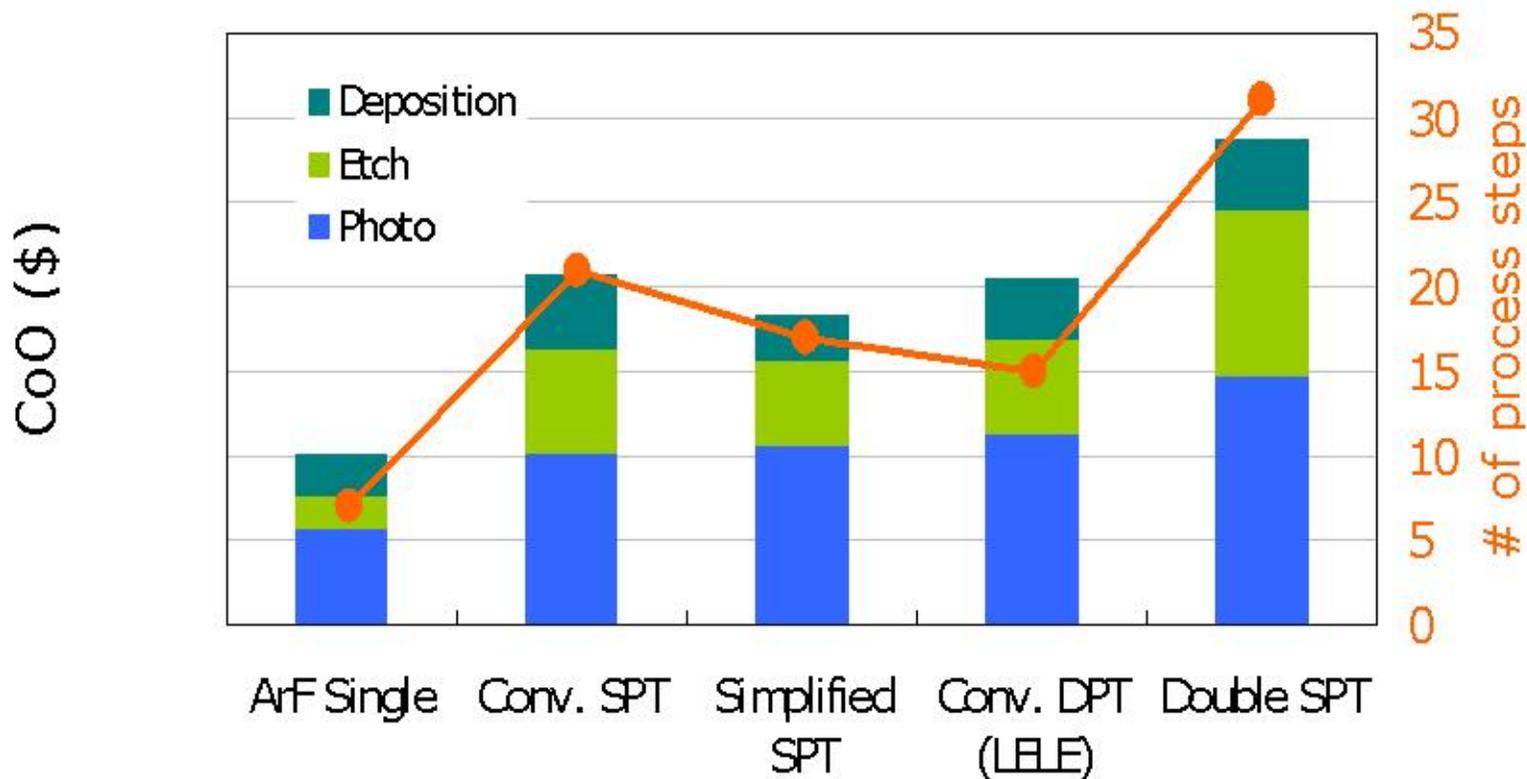
Double patterning



Resolution reached to half of single lithography limit

Spacer patterning	LELE(LPPE) Double patterning
 <ul style="list-style-type: none"> • Hard mask deposition • Partition Litho/Etch • Spacer Deposition/etch • Pattern Etch 	 <ul style="list-style-type: none"> • Hard mask deposition • Litho • Etch (or Process in track) • Litho • Pattern Etch
	

Cost & complexity of double patterning



Will EUV prevail ?



EUV Symposium (2009, Oct.)

Big Match @ 2013

Ready, Set, Go !



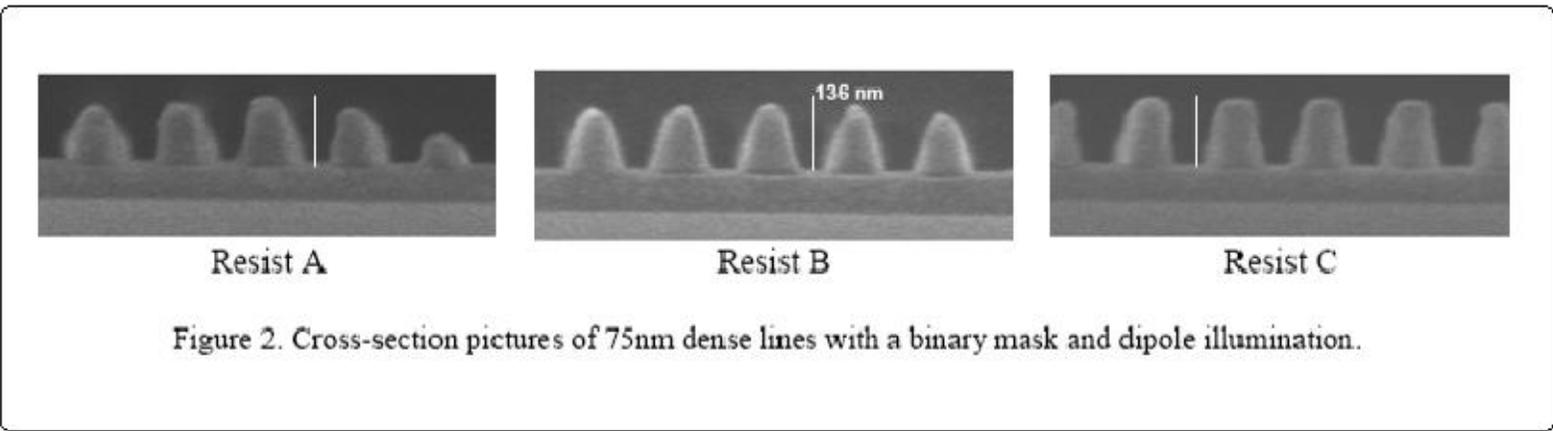
Back to SPIE 2004



- ❑ **157nm session in SPIE disappeared since 2005**
so as the interest in the technology → **It is the Resolution !!**

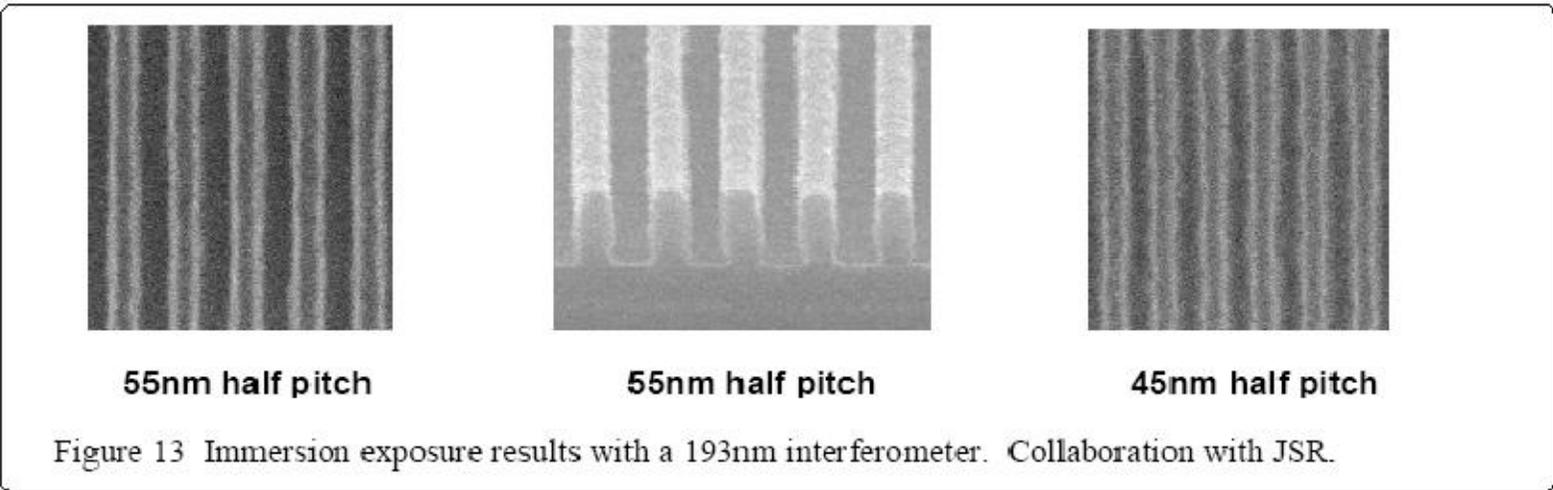
157nm Dry
@ 75 nm

SPIE 2004
5377-170



ArF
Immersion
@ 55 nm

SPIE 2004
5377-24



SPIE 2009 for EUV



EUV Symposium (2009, Oct.)

Advanced Lithography 2009

ArFi vs. EUV @2X DRAM

Brick Wall

ArFi (1.35NA) EUV (0.25NA)

Double Patterning

L&S (Cell)

Double Patterning

L/S (Periphery)

No Data Not OPCed

Contact Hole

Double Patterning

ArFi @0.20k1 << EUV @0.51k1

attenn

Block edge of D1X

w/ OPC w/o OPC

32nm 1:1

No Image

EUUV-55 resist dose 18.2 mJ/cm² F1=60nm

28nm

SPIE Advanced Lithography

22.2mJ	25.8mJ	28.2mJ	30.6mJ	32nm
38nm	35nm	32nm	33nm	33mJ

hynix



imec

imec confidential

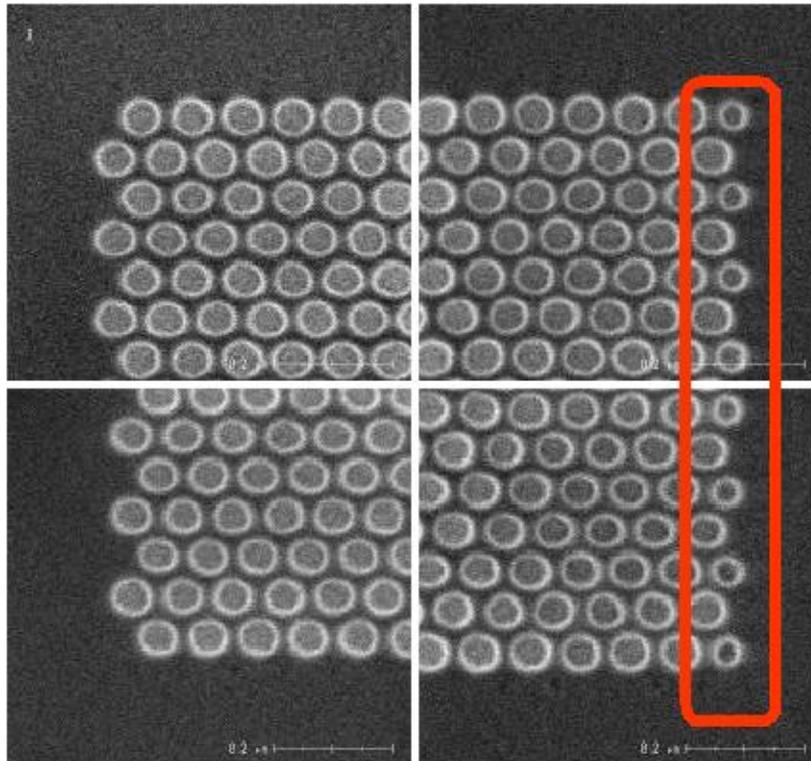
Geert Vanpenhooch
© imec 2009 48/75

hynix

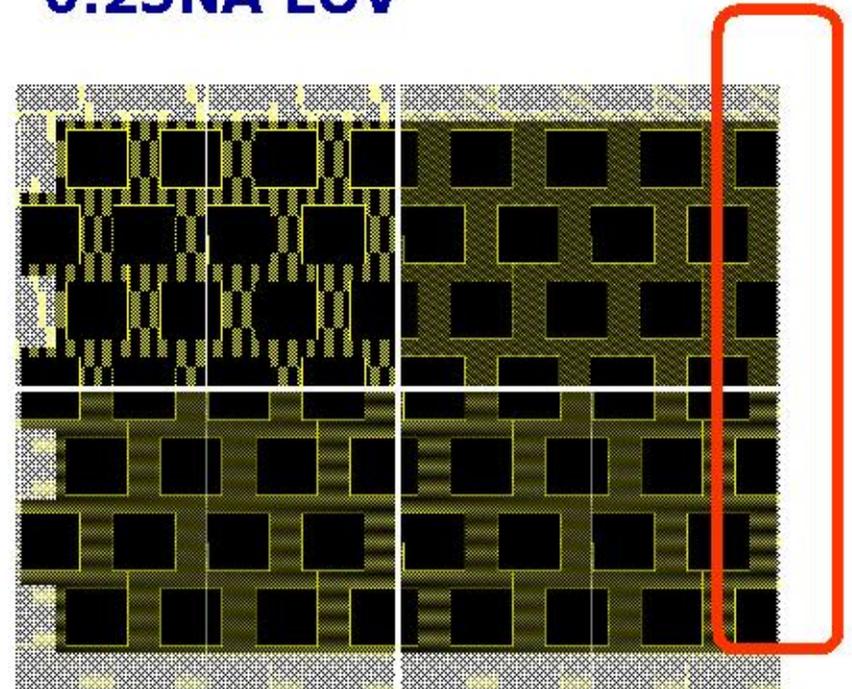
Resolution is not an issue to EUV



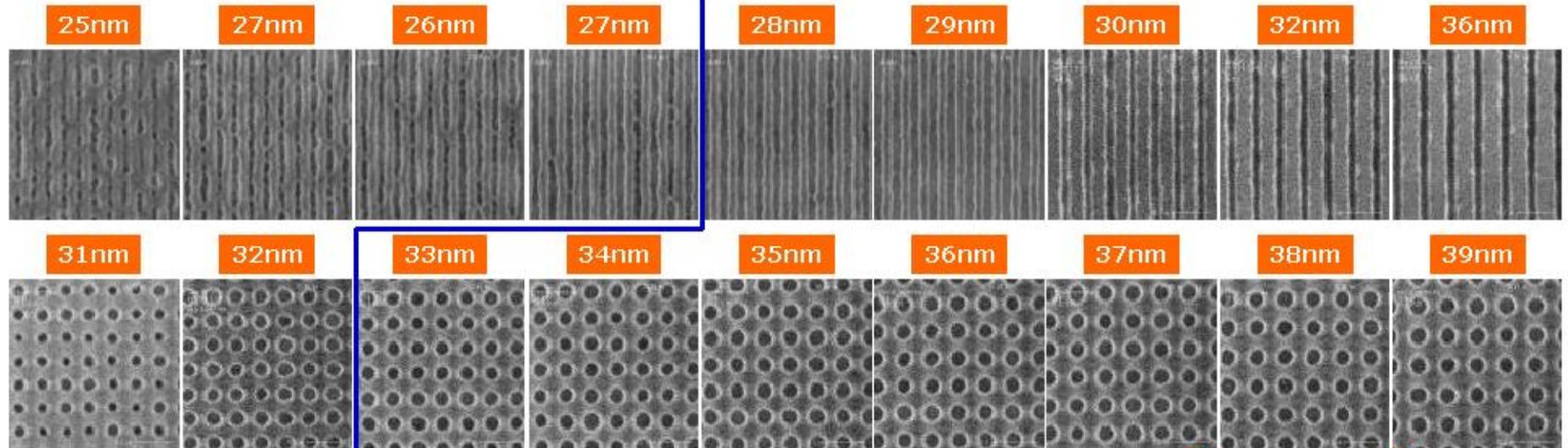
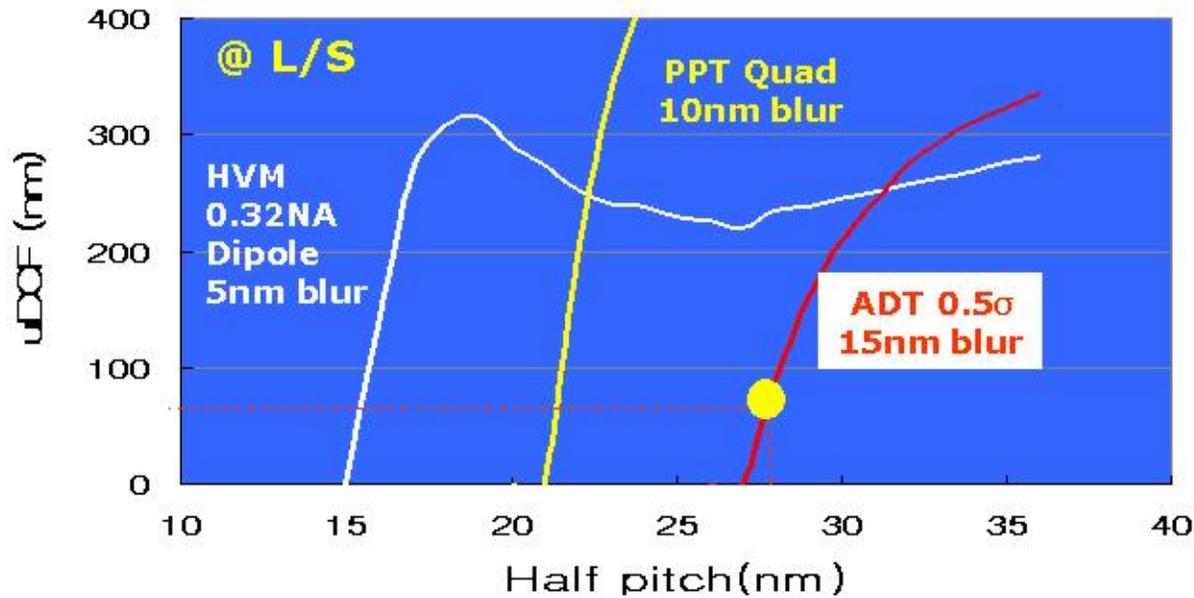
- Amazing... Partially drawn C/H patterned !! (3x nm)
Block edge contact holes are good without OPC !



0.25NA EUV



and progress continues though slow

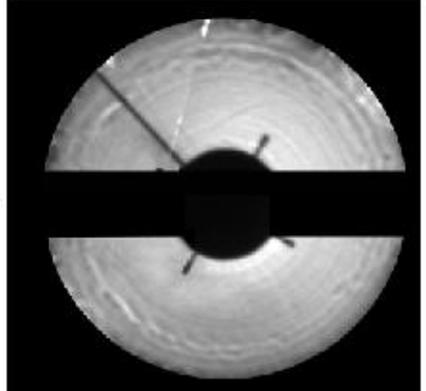
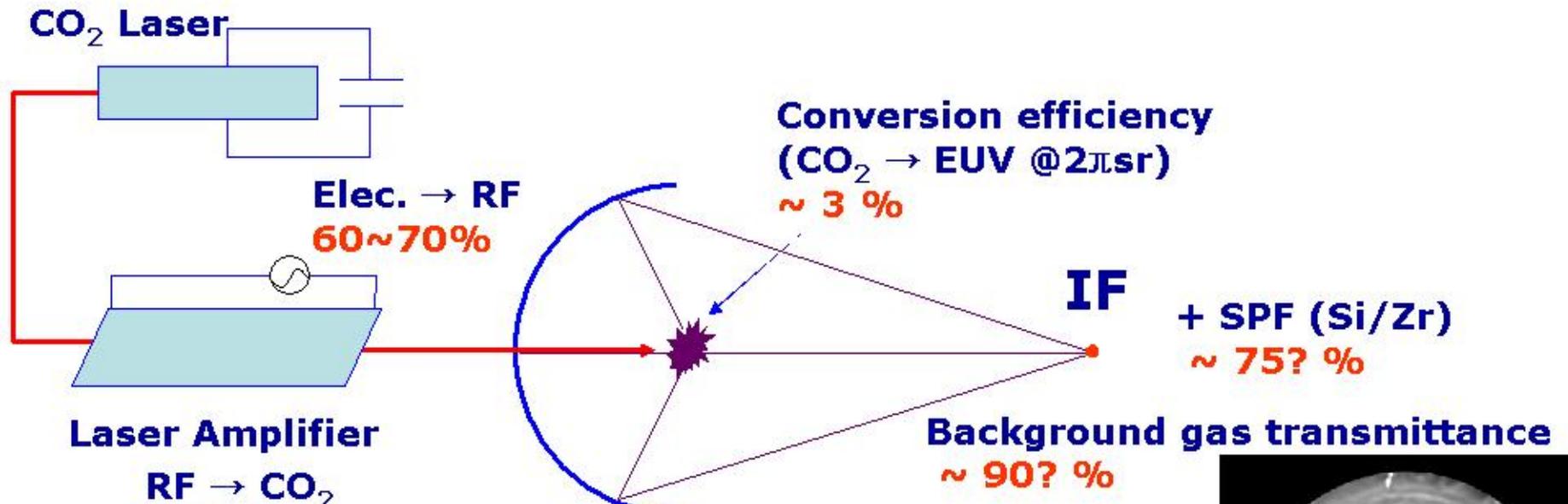


Experiment @0.25NA EUV

Conversion of Electricity to EUV



□ Conversion efficiency from wall plug to EUV at IF: **~0.02%**



Electricity consumption



$$1000 \text{ kW} \times 0.02 \% = 200 \text{ W}$$

Of course expensive, but manageable electric power !

IF Power in band	Throughput (wph)	Input Electricity	EUV Source for 10 tools
100 W	60	500 kW	5,000 kW
200 W	100	1,000 kW	10,000 kW
400 W	150	2,000 kW	20,000 kW

※ ArF Immersion Scanner ~ 165kW

12" fab. 130k wafers per month: **50,000kW**

... and it might not be the worst case estimation !

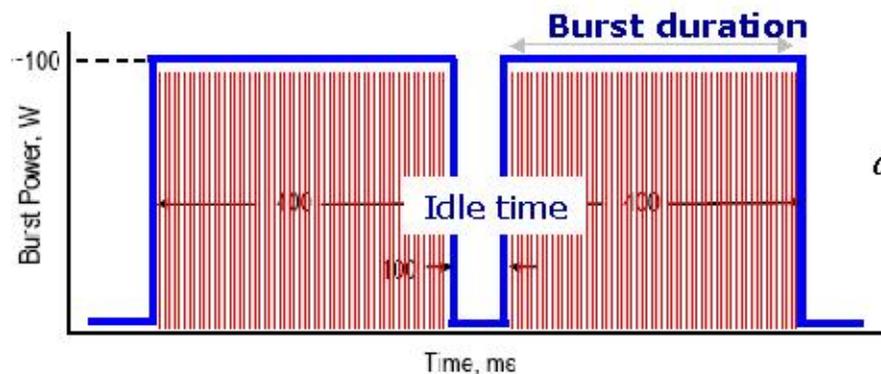
A good sign of power reduction in EUV HVM

LPP source progress



	Cymer LPP progress				
	'07. 4Q	'08. 4Q	'09. 1Q	'09. 3Q*	PPT target
Power @IF	100W	50W	15W	75 W	100W
Duty cycle	5%	8%	40%	60%	80%
Burst duration	1ms	1ms	400ms	400ms	400ms
Dose Stability	-	-	-	± 0.35% (at 50W)	± 0.20%
Continuous Operation	few sec	10hrs	50hrs	1hr	> 50hrs

* Data courtesy of Cymer

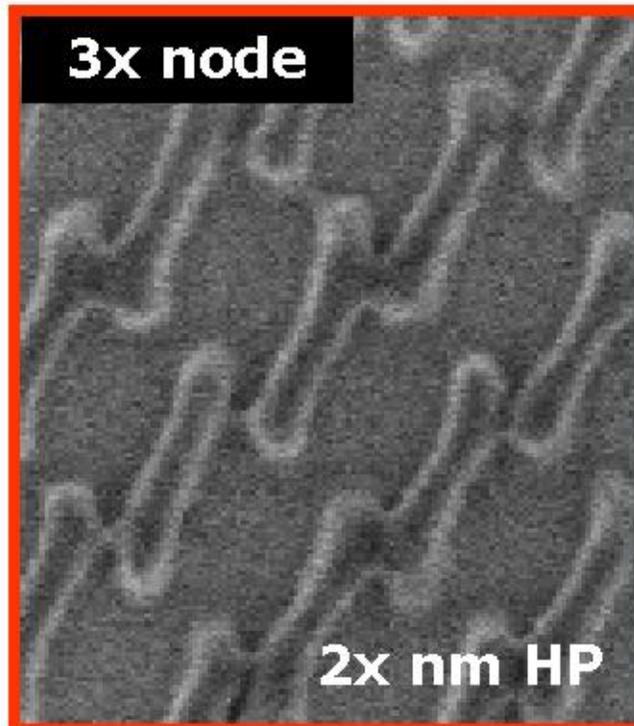
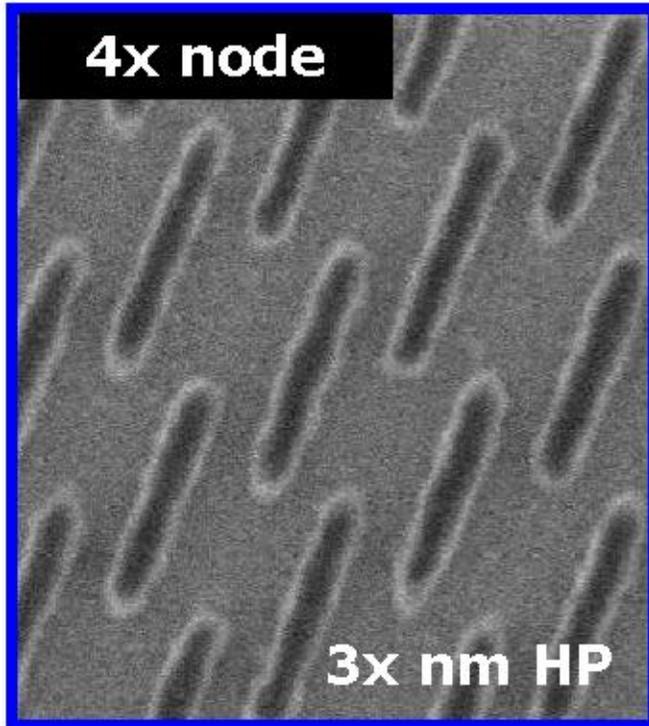


$$duty\ cycle = \frac{burst\ time}{burst\ time + idle\ time}$$

Can 0.32NA be a solution ?



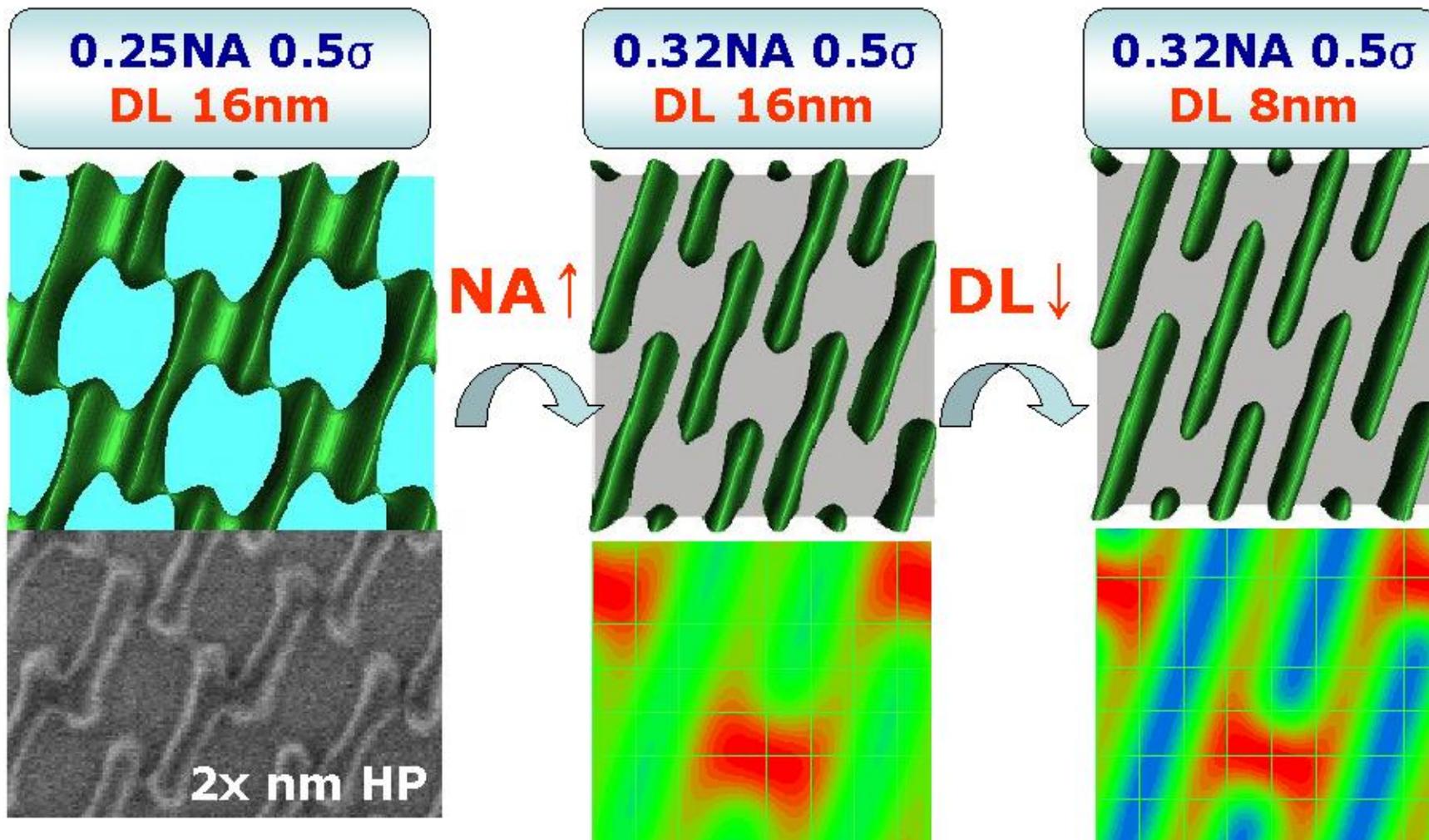
- DRAM Active Patterning with EUV 0.25NA, 0.5σ



EUUV 0.32NA

Can 0.32NA solve it?

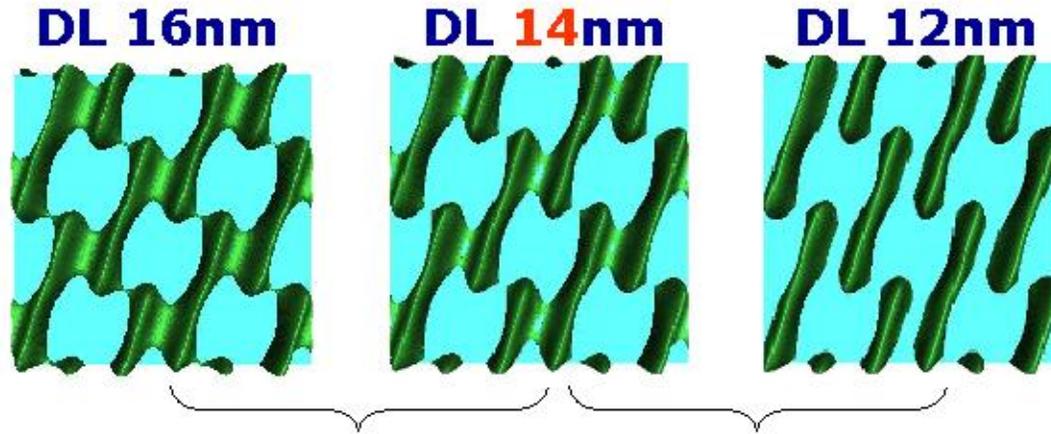
□ DRAM 3x simulation @ EUV



w/ Slitho-euv

XINIX

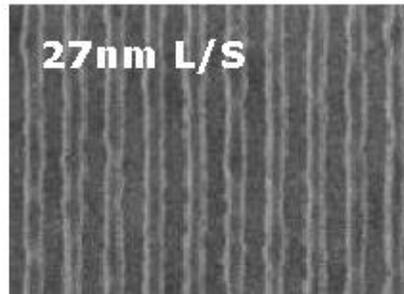
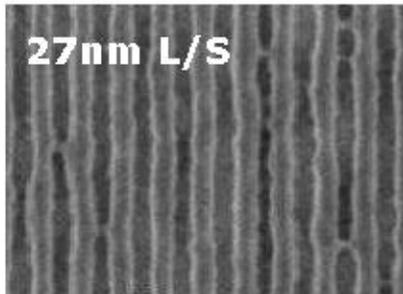
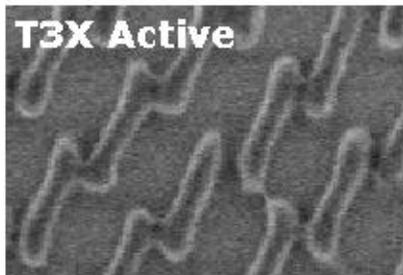
Where are we ?



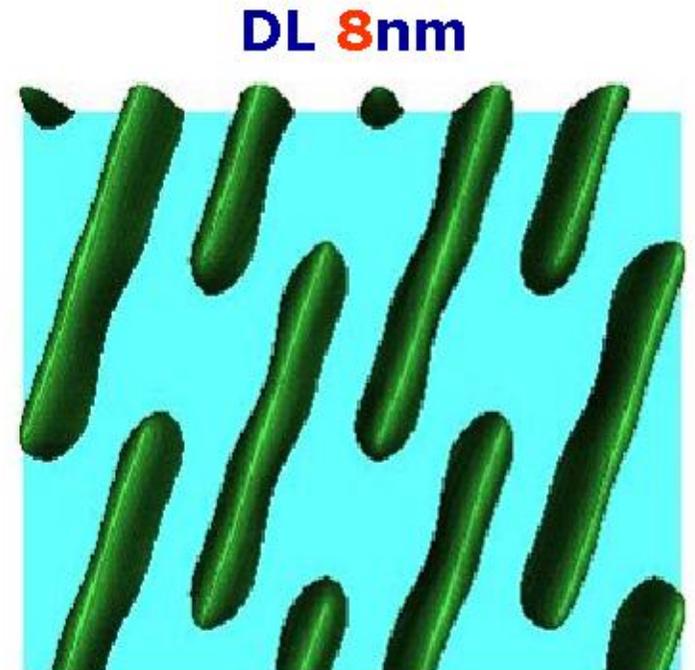
Resist Diffusion Control is Key !!

Old Resist

New Resist



0.25NA EUV

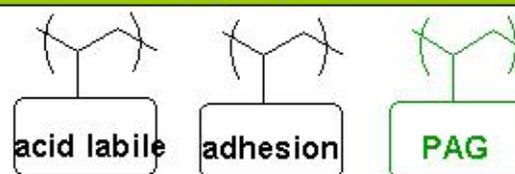


Required DL @ 2x nm HP = 8 nm

Acid diffusion length roadmap



HP (nm)	Resist Blur @ 60% Contrast	Resist Acid Diffusion (nm)				theoretical limit
		conventional	current	advanced	extreme	
			2007	2009	2012 (plan)	
32 ²⁾	12.8	32 ¹⁾	13 ¹⁾			
22	8.8			10		
16	6.4				7 ³⁾	
11	4.4					5 ⁴⁾
Resist Chemistry		Blend PAG	Bound PAG			Non CAR

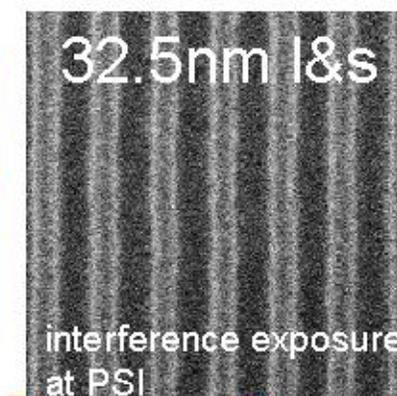


1) Acid diffusion length, L_d , comparison between blend and bound PAG resists

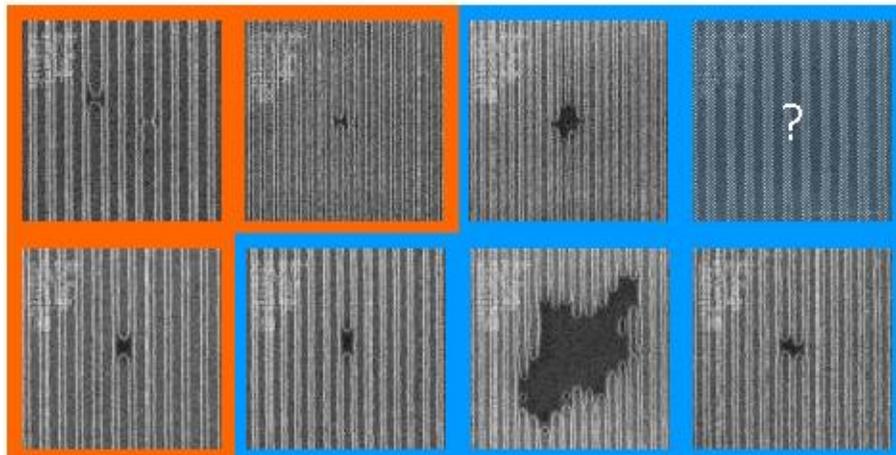
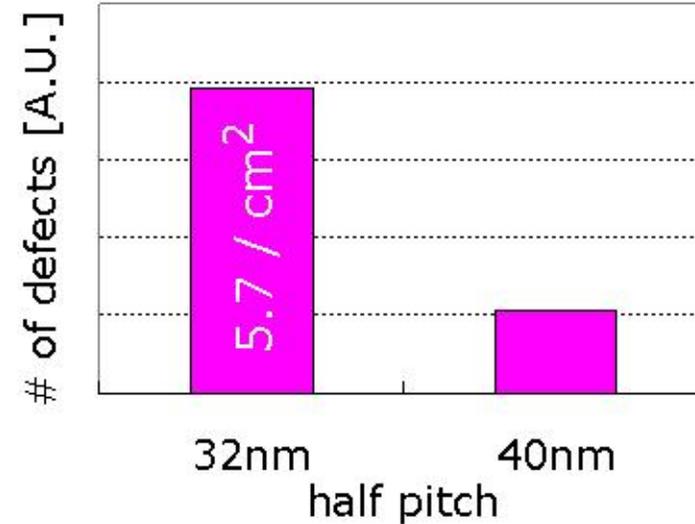
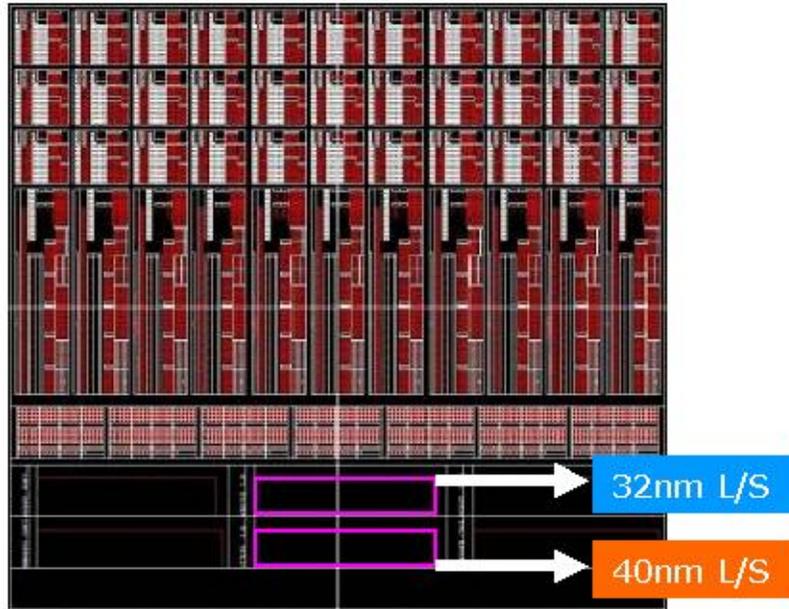
	p (nm)	λ (nm)	ν (s ⁻¹)	E_s (mJ/cm ²)	d (nm)	EL	LWR (nm)	L_d (nm)	K_{LUP}
MET-2D	100	13.4	2.24E+16	22.7	90	0.12	8.1	32	0.73
	90	13.4	2.24E+16	24.6	90	0.11	8.7	32	0.83
Blend A	100	13.4	2.24E+16	22.8	80	0.17	8.3	26	0.62
	90	13.4	2.24E+16	25.0	80	0.16	6.1	26	0.66
EUV-B	100	13.4	2.24E+16	41.1	80	0.21	4.9	17	0.43
	90	13.4	2.24E+16	45.2	80	0.23	4.4	17	0.49
EUV-C	100	13.4	2.24E+16	37.7	80	0.23	4.6	13	0.28
	90	13.4	2.24E+16	42.0	80	0.24	4.8	13	0.36

Courtesy of IMEC & Shinetsu

2) 32nm resolution on Bound PAG



Repeating defect vs. Design rule



For Defect Density 1/cm²
 ≙ **707 defects [per wafer]**

For Defect Density 0.1/cm²
 ≙ **71 defect [per wafer]**

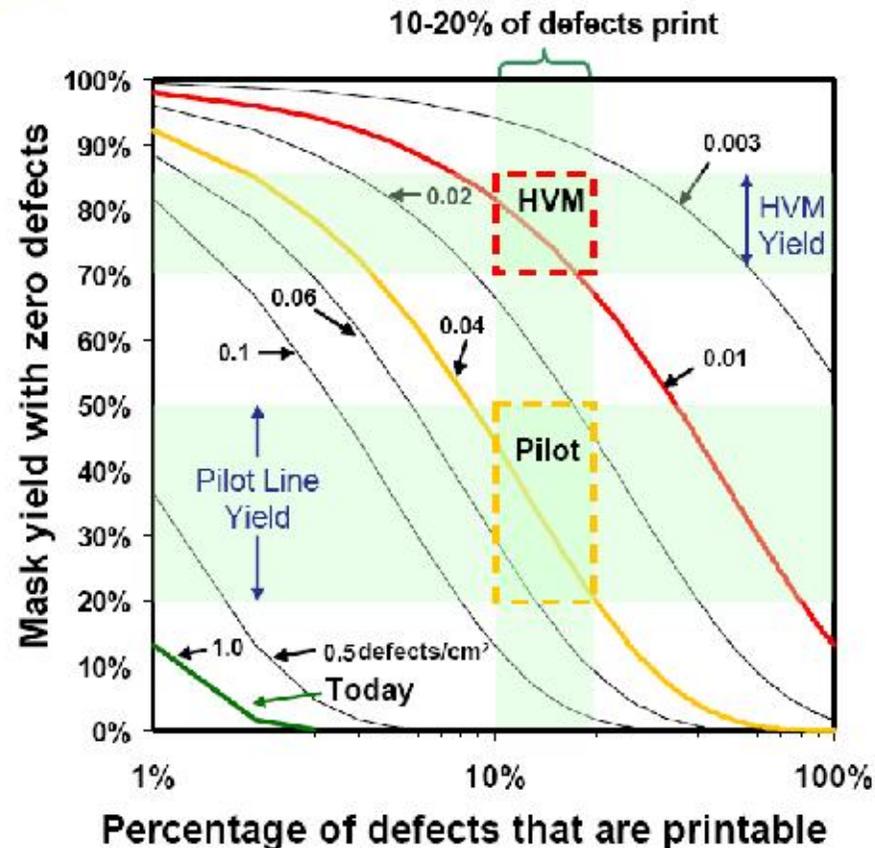
Mask Blank Yield Gap by Sematech



Mask Blank Yield Gap for Pilot Line and HVM Introduction



- **Best Mask Blank Data**
 - 0.4 defects/cm² @ 25 nm (mid-cycle insertion at 27-28 nm hp)
 - 1.0 defects/cm² @ 18 nm (22 nm hp insertion)
- **Gap to Pilot Line Yield (0.04 defects/cm²)**
 - Mid-cycle insertion: ~10X
 - 22 nm hp insertion: ~25X
- **Gap to HVM Yield (0.01 defects/cm²)**
 - Mid-cycle insertion: ~50X
 - 22 nm hp insertion: ~100X



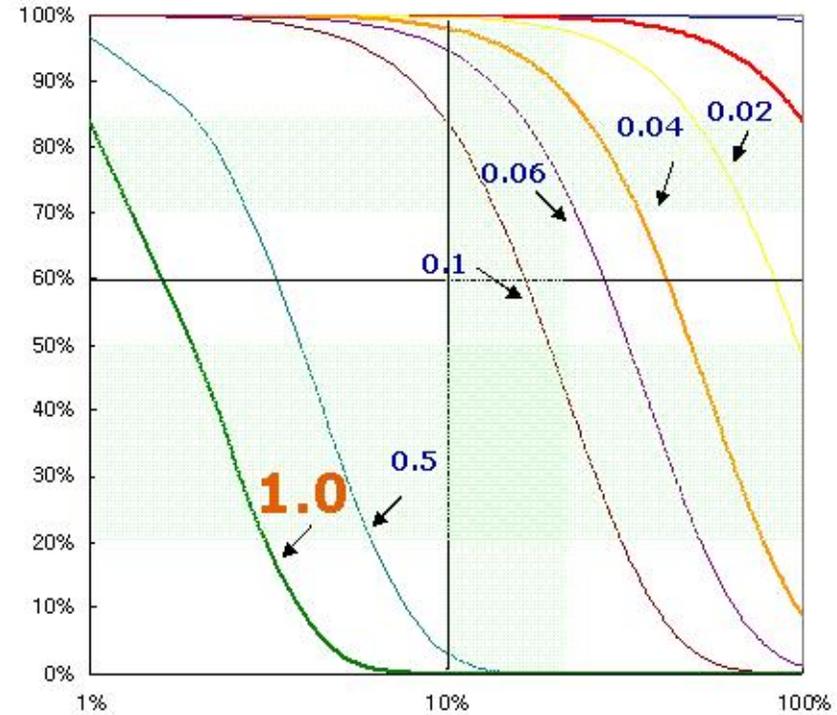
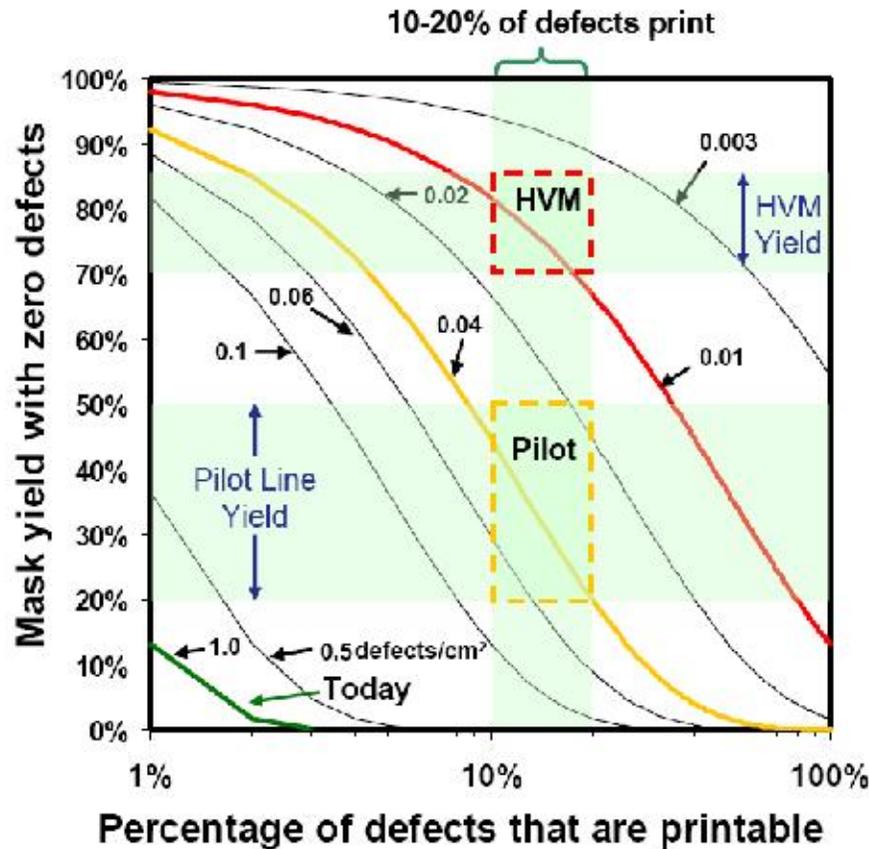
If I soothe myself a little bit,



If no RD allowed

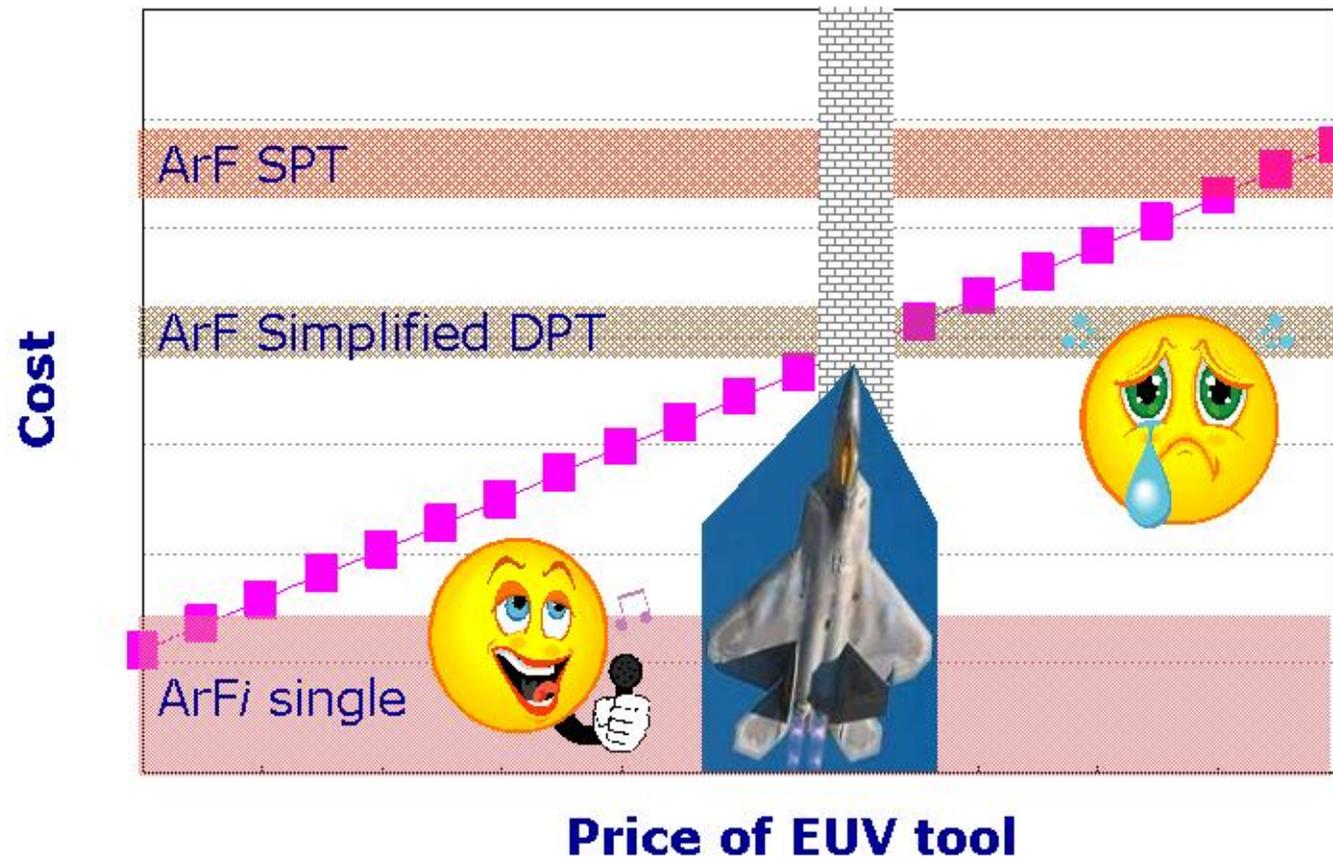


If 2 RDs allowed



Still 10X... but much closer

EUV cost is still big concern



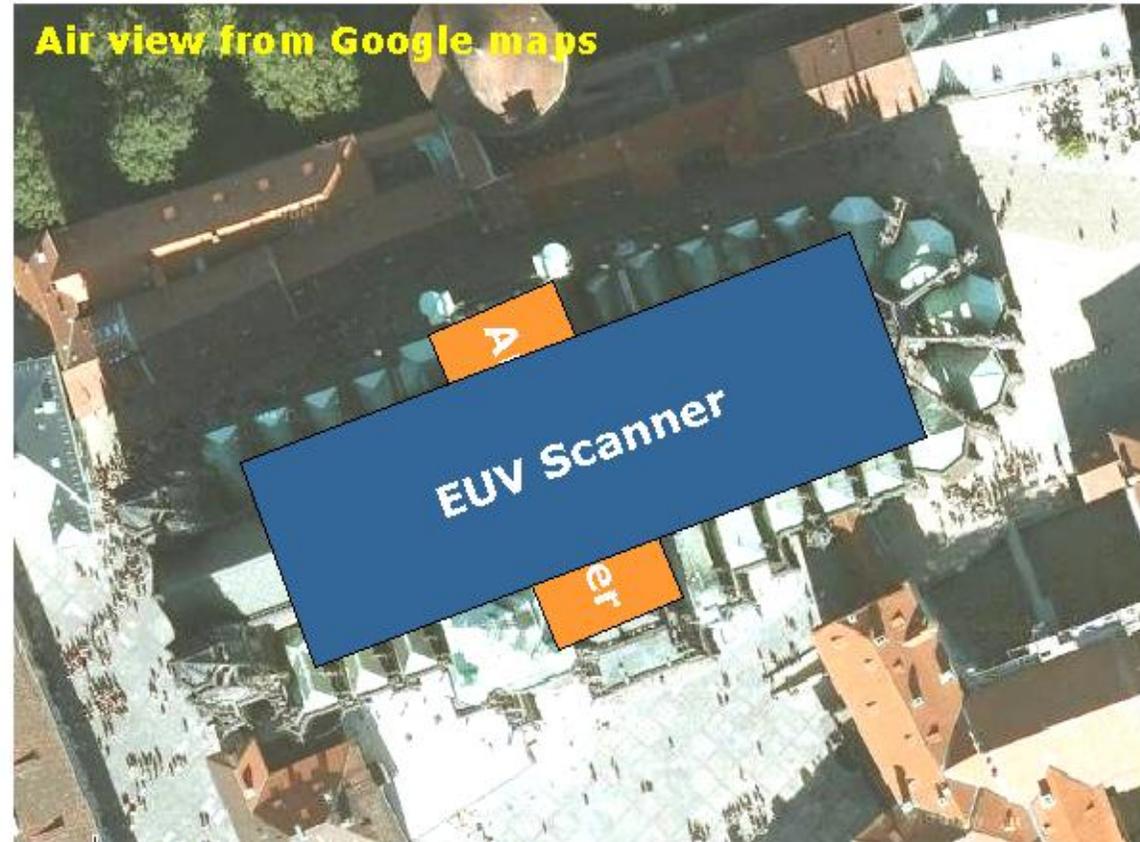
- Price/Throughput of EUV should have cost competitiveness ;
ArFi single < EUV << ArFi Double !!!

St. Vitus Cathedral in Praha Castle



- ❑ **If both are same throughput, EUV will lost productivity**

$$Productivity = f (throughput * MFS * ... \div foot print)$$



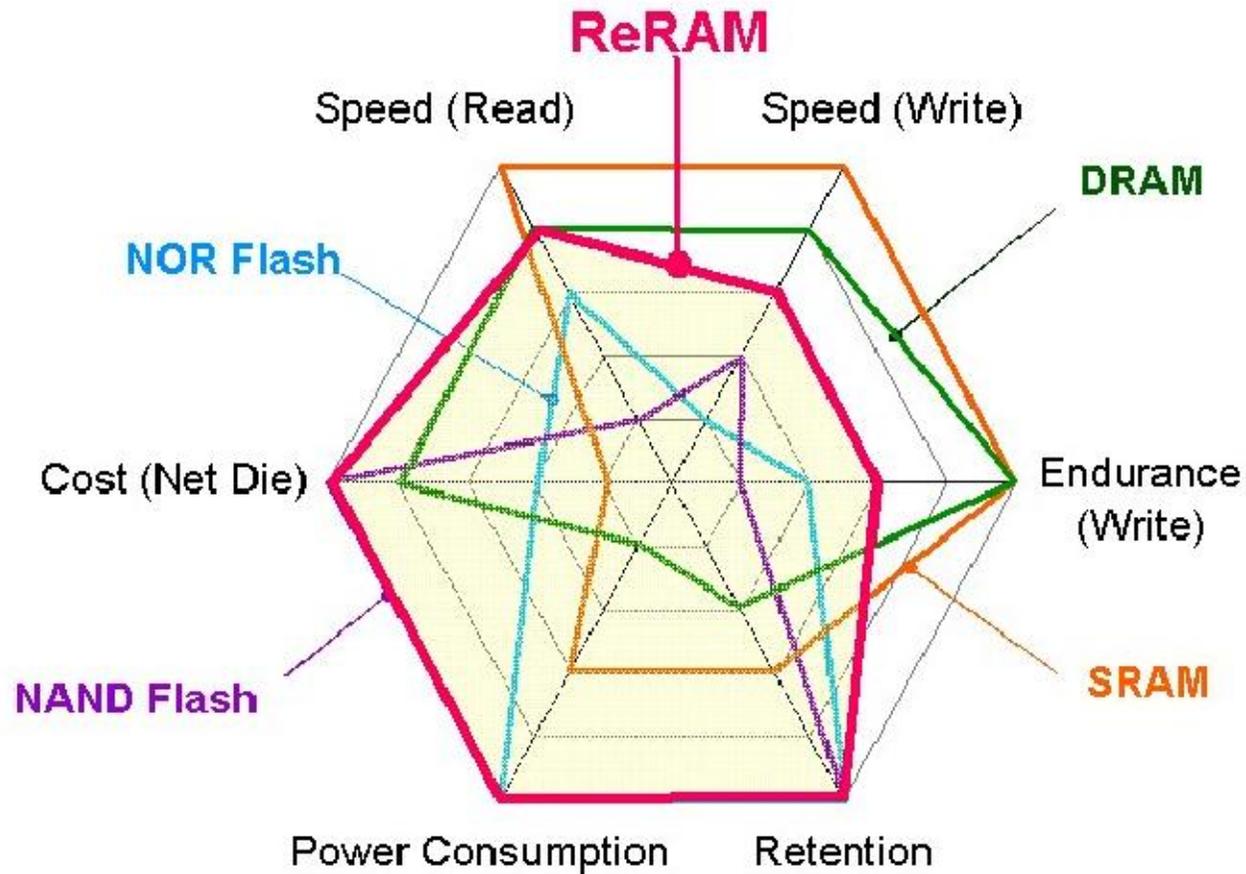
ArFi: 2 Transepts

EUV: Nave + Aisles

Future of Memory Devices



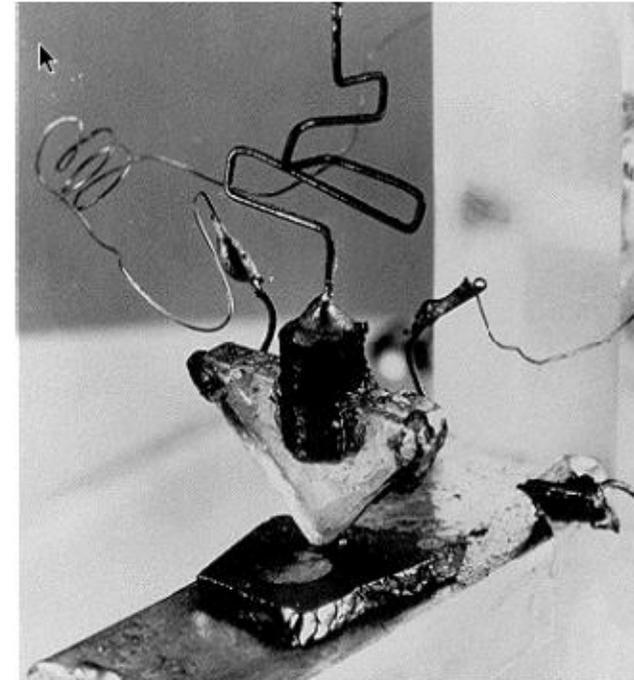
EUV Symposium (2009, Oct.)



Desire for memory, Desire for invention

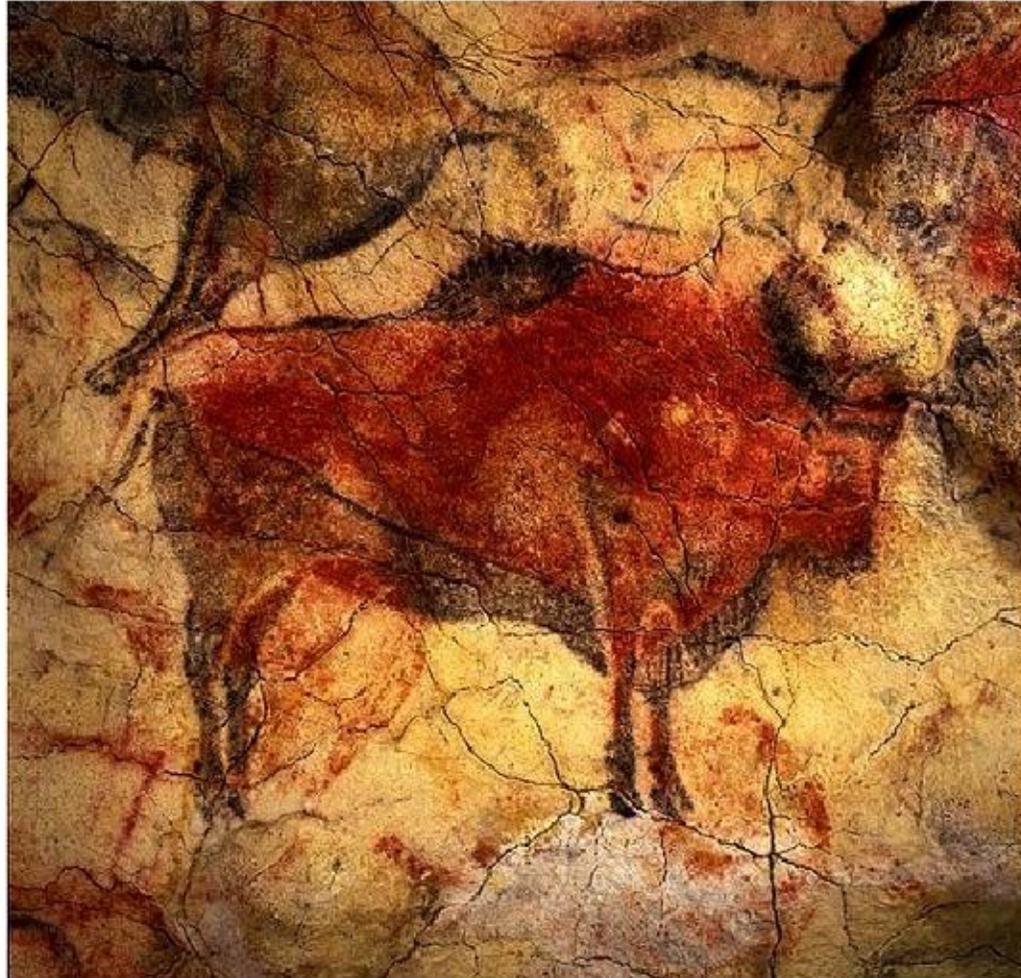


EUV Symposium (2009, Oct.)



1947

Future of Memory Devices



in Cave of Altamira

Cave of Altamira

Old Stone Age...
13,000 year ago...

Memory devices has been developed since the beginning of history

So my answer to questions asked before is "Future of Memory will always be **Bright**"

Summary



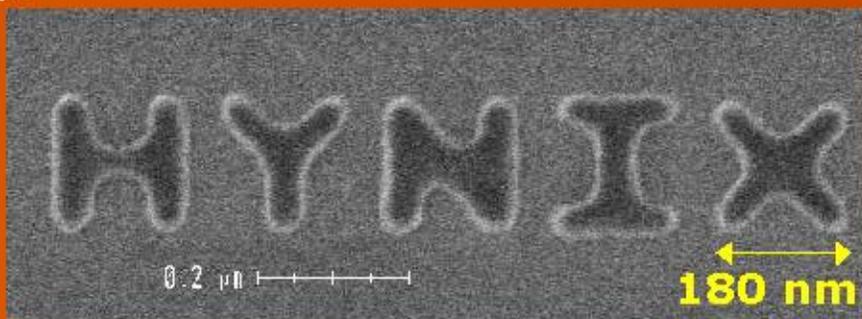
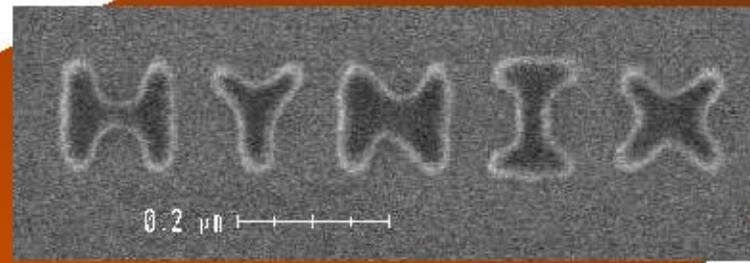
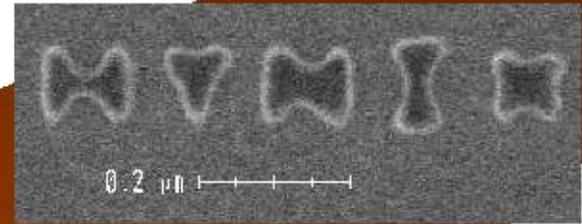
- For Flash, tech shrink will be continued by ArF spacer patterning. EUV readiness is not matched to roadmap
- Pattern with high aspect ratio would be a big concern
- 2-dimensional Lithography patterning will be a hurdle in DRAM integration and EUV has a chance at sub-30nm node in 2013
- Resist diffusion length should be controlled within 8nm
- Much efforts should be placed on masks

HYNIX with EUV



The smallest logo ever !

HYNIX patterned by EUV ADT



Hynix wants to make good memory with EUV

EUV Symposium (2009, Oct.)



Thank You.....

