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Property

Towards High-Volume Manufacturing of Logic Devices Using EUV Lithography

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Taiwan Semiconductor Manufacturing Company

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TSMC Fabs Around the World

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6“ Fab in Taiwan

Fab 2

8“ Fabs in Taiwan

Fab 3

Fab 5

Fab 6

Fab 8

8“ Fabs Overseas

Fab10 (China)

Fab11 (USA)

SSMC (Singapore)*

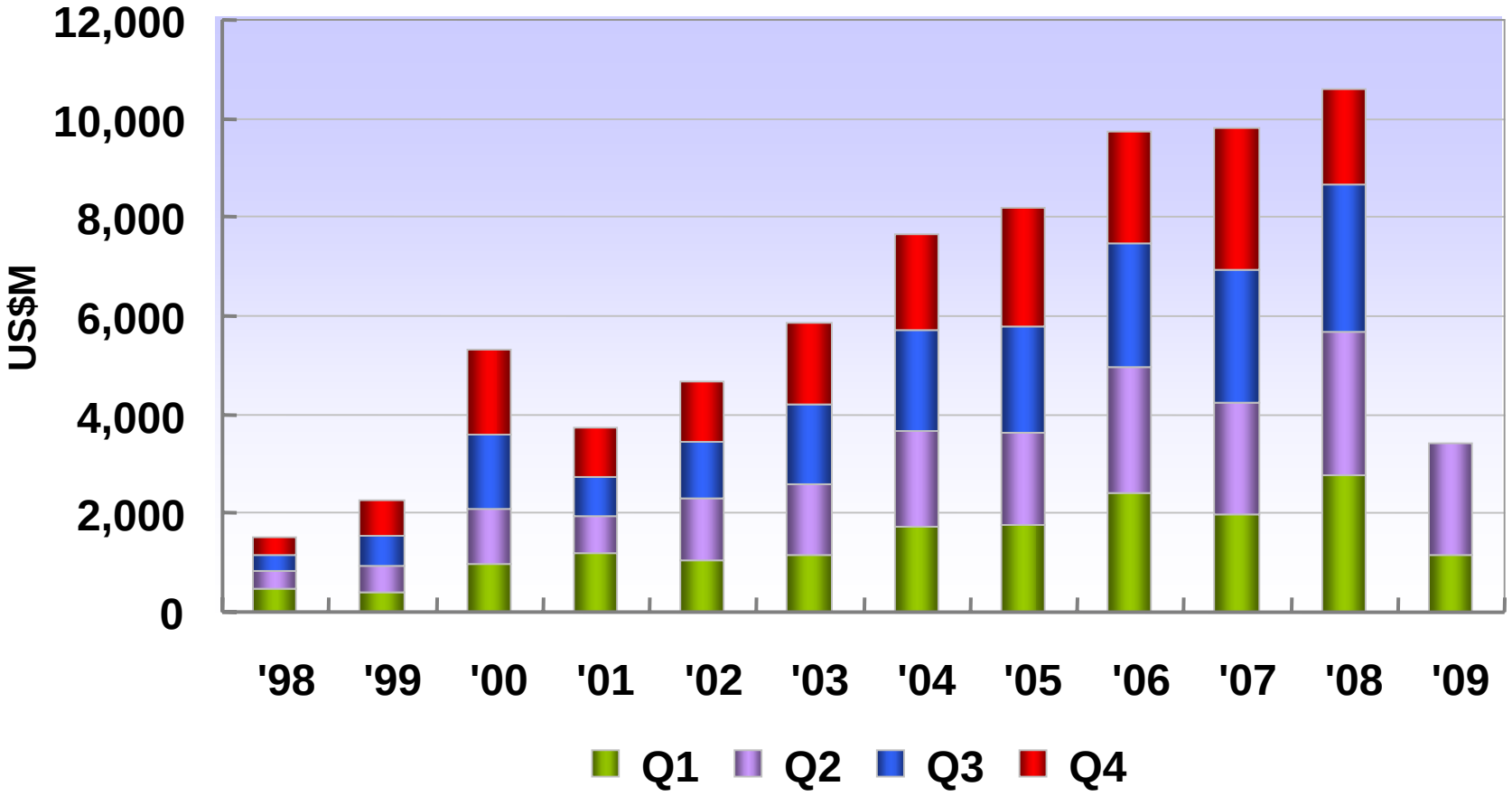
** JV with NXP*

12“ Fabs in Taiwan

Fab12

Fab14

TSMC Sales Growth



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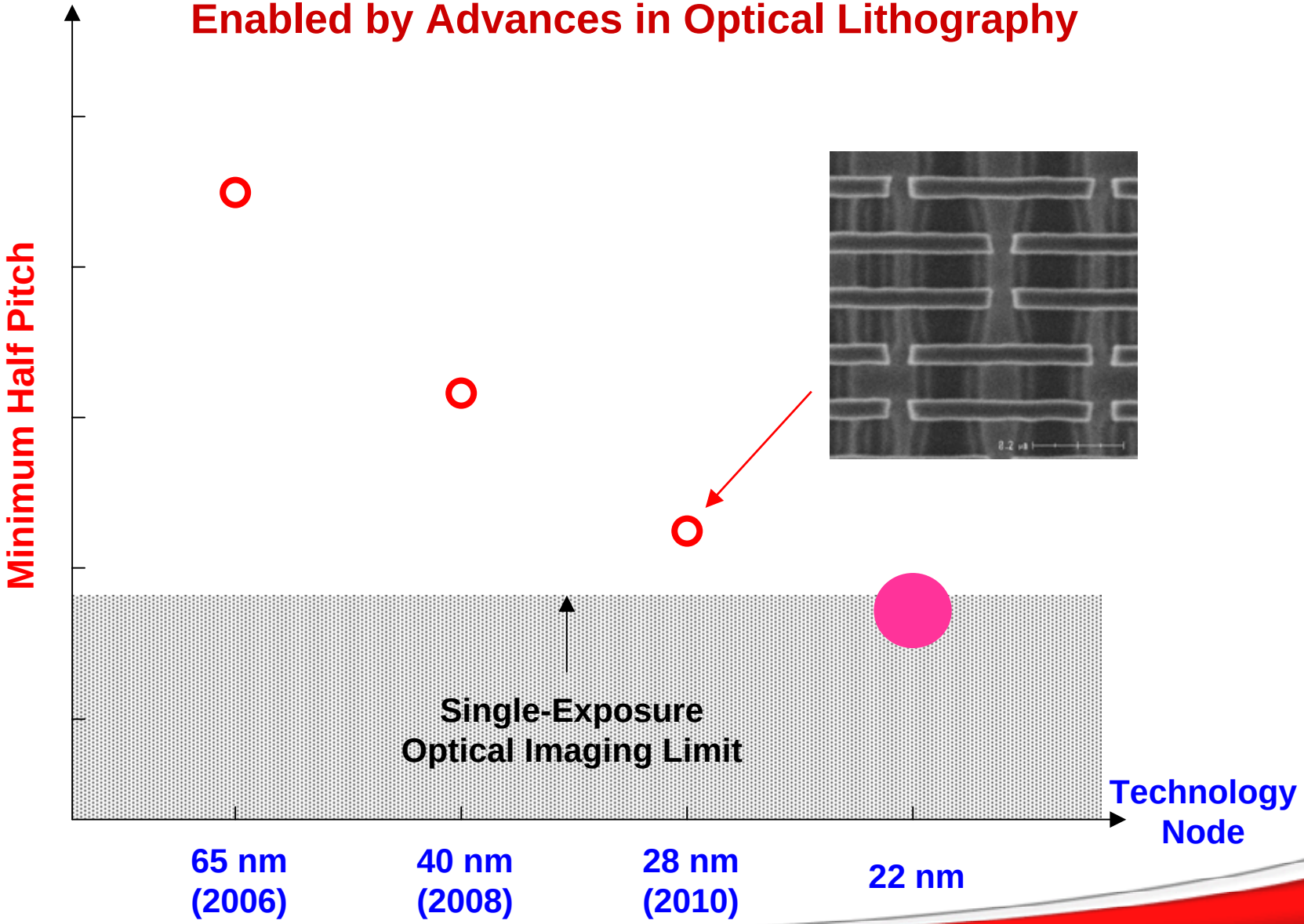
TSMC Technology Roadmap

Enabled by Advances in Optical Lithography



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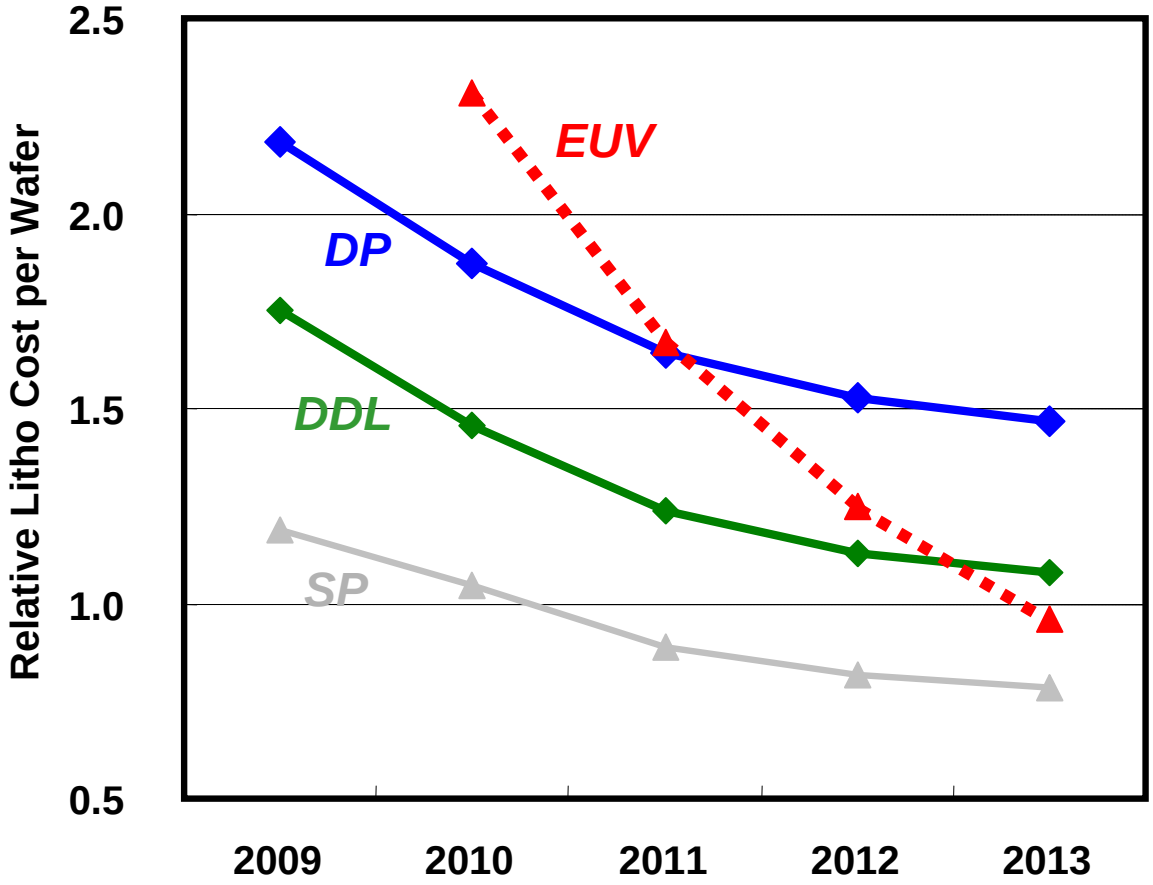
EUVL Will Have a Cost Advantage

if suppliers execute to their throughput roadmaps



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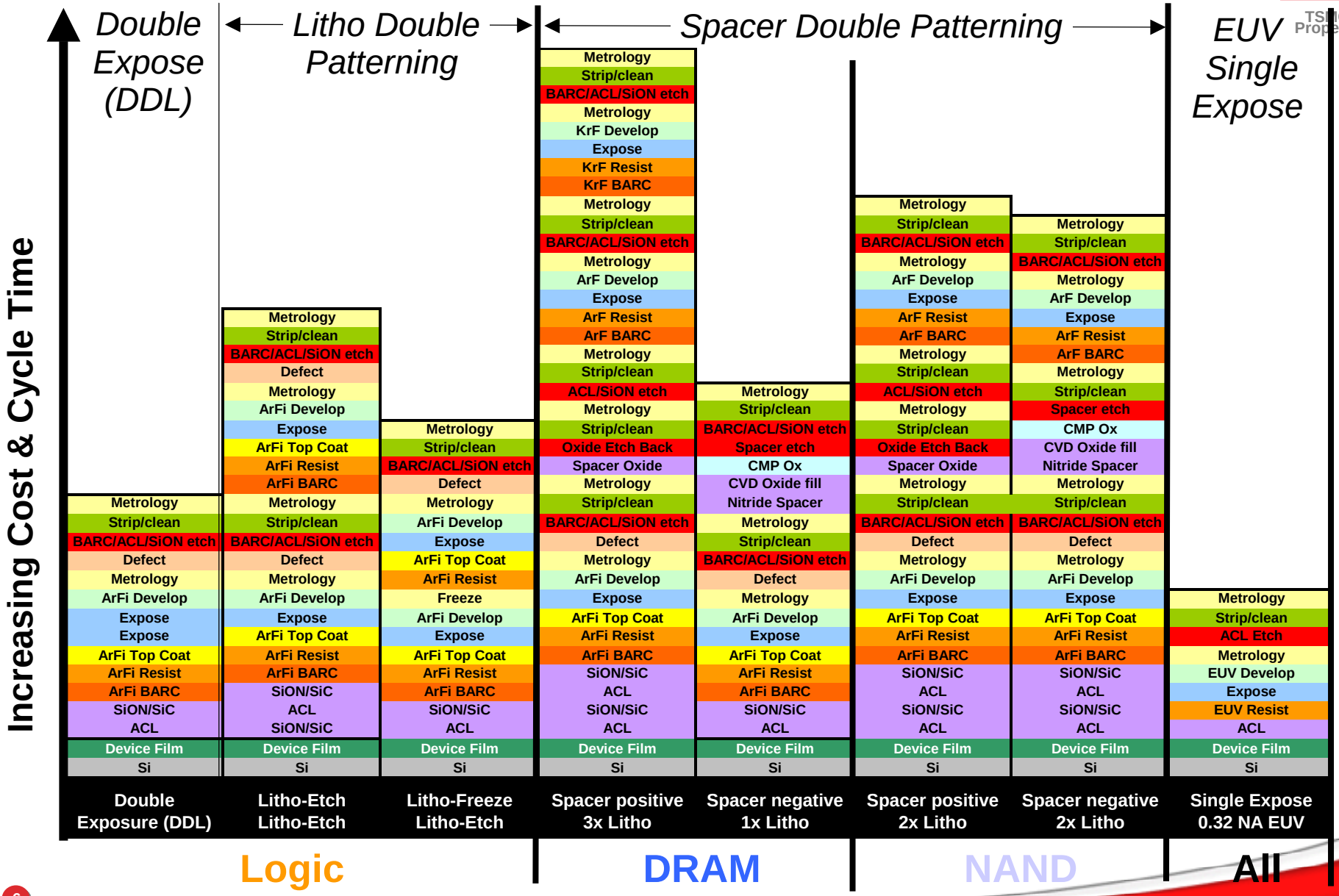
Processing Steps for 22-nm Patterning Alternatives



Source: ASML

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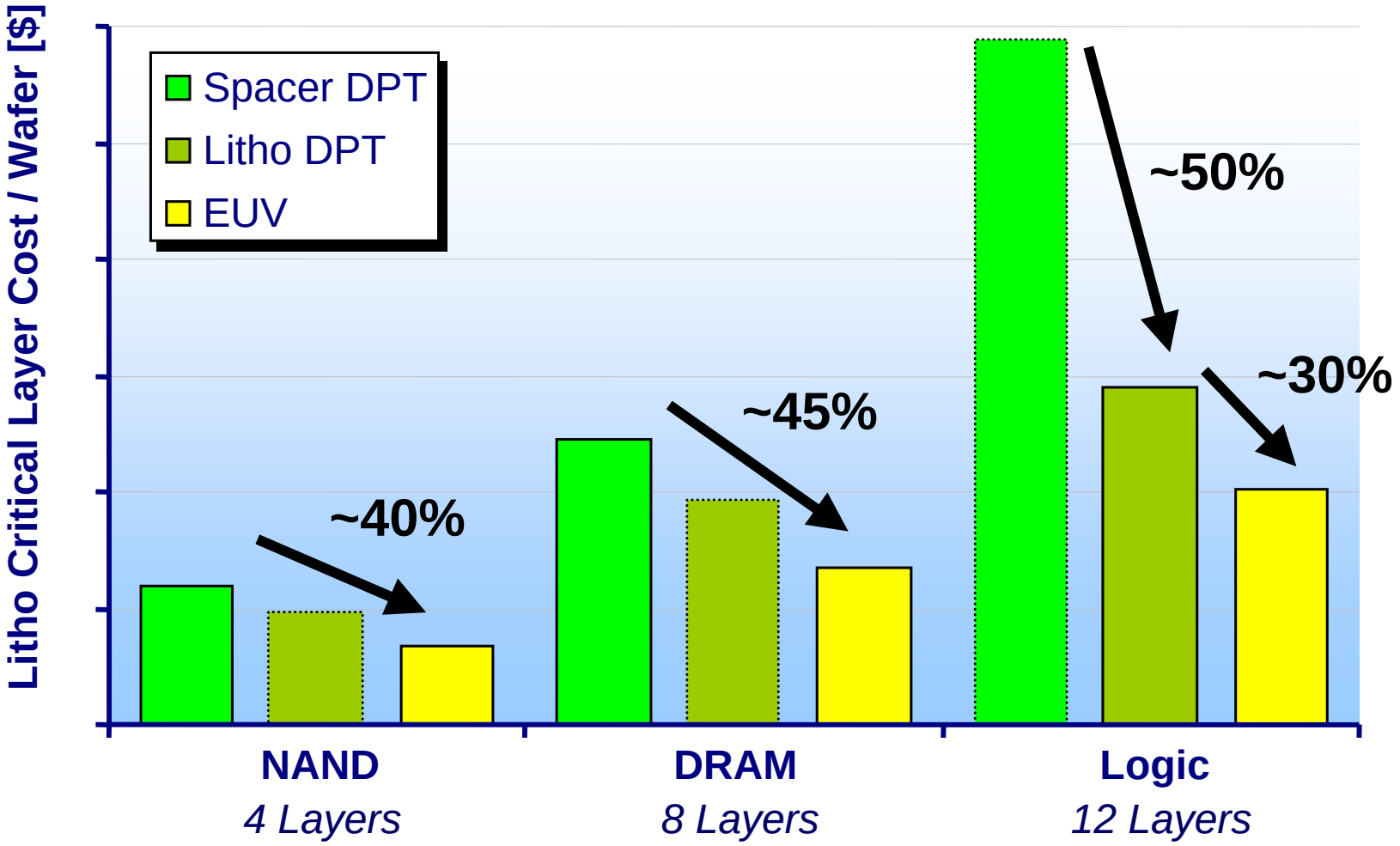
22-nm Node Critical Layer Patterning Cost



Source: ASML

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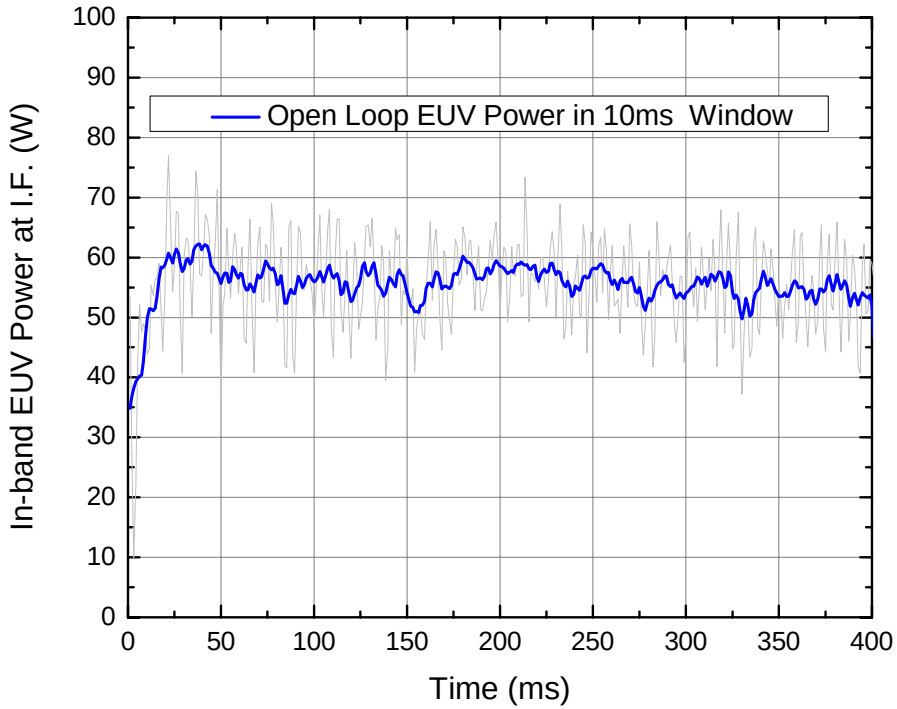
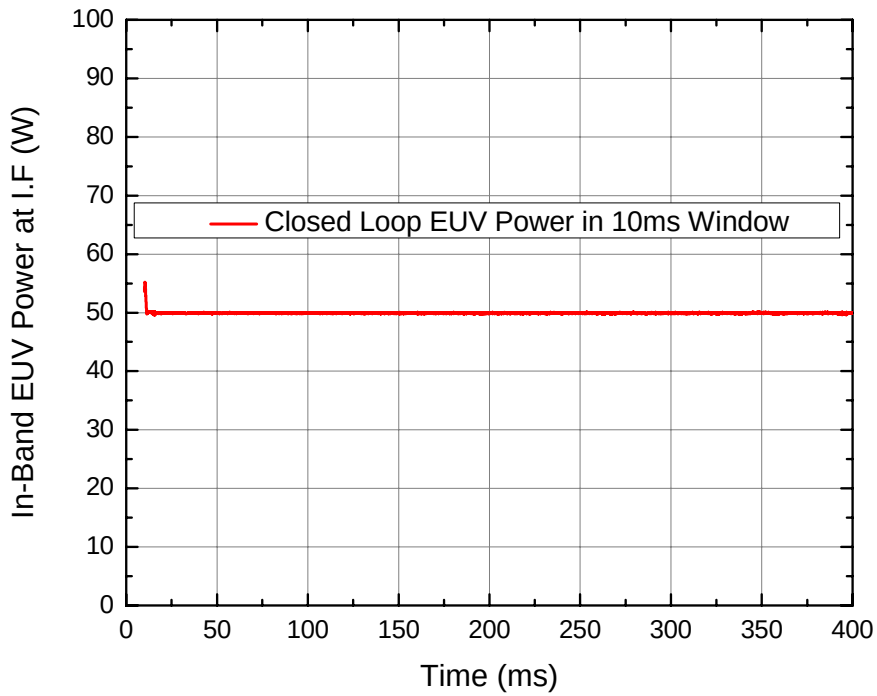
Closed Loop Dose Stability of <±0.35% meets Device Production Requirements





- Open loop dose performance is <+/-11% (10ms window)

Source: Cymer

- **Closed loop dose performance is <+/-0.35%**
- EUV power level set point for closed loop control was 50W

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In-House Fabrication of EUV Masks

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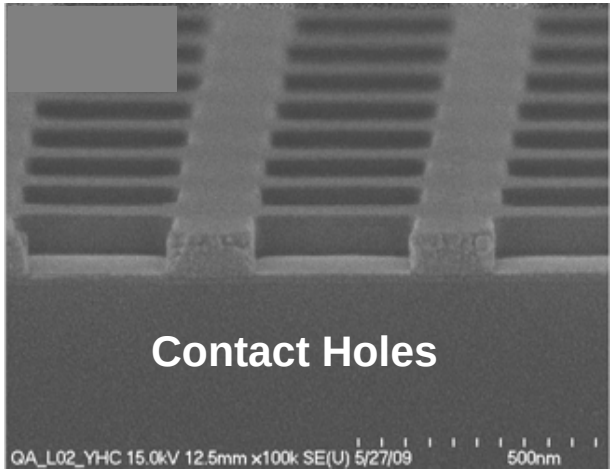

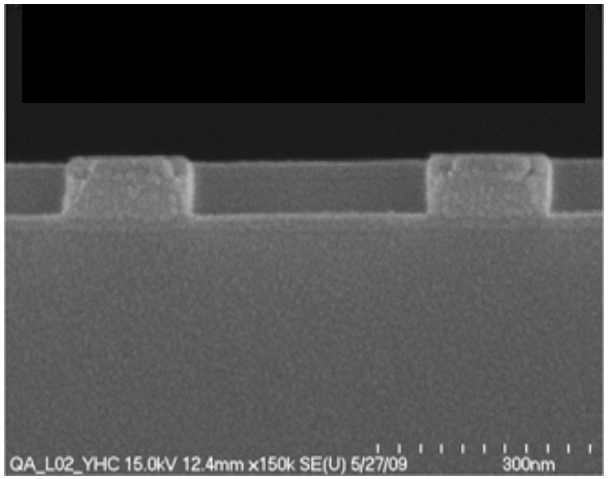

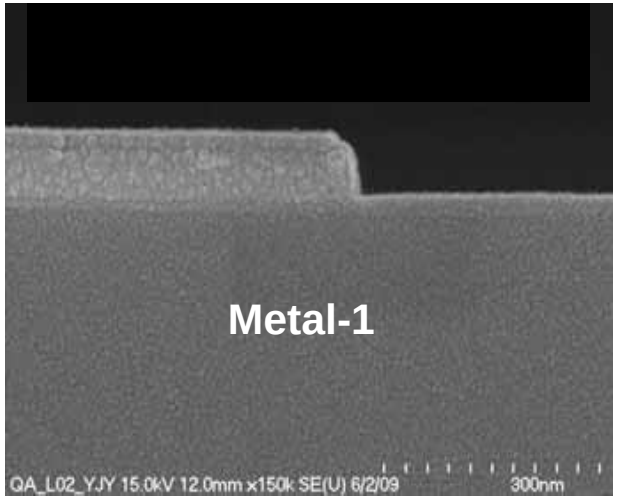

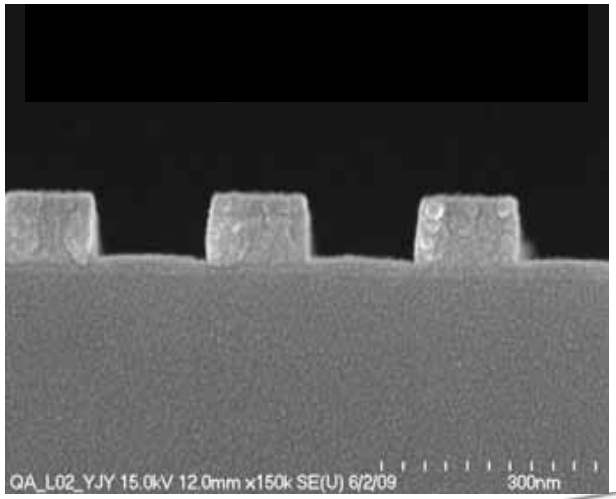

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Absorber Defect Inspection Using 193-nm Tool

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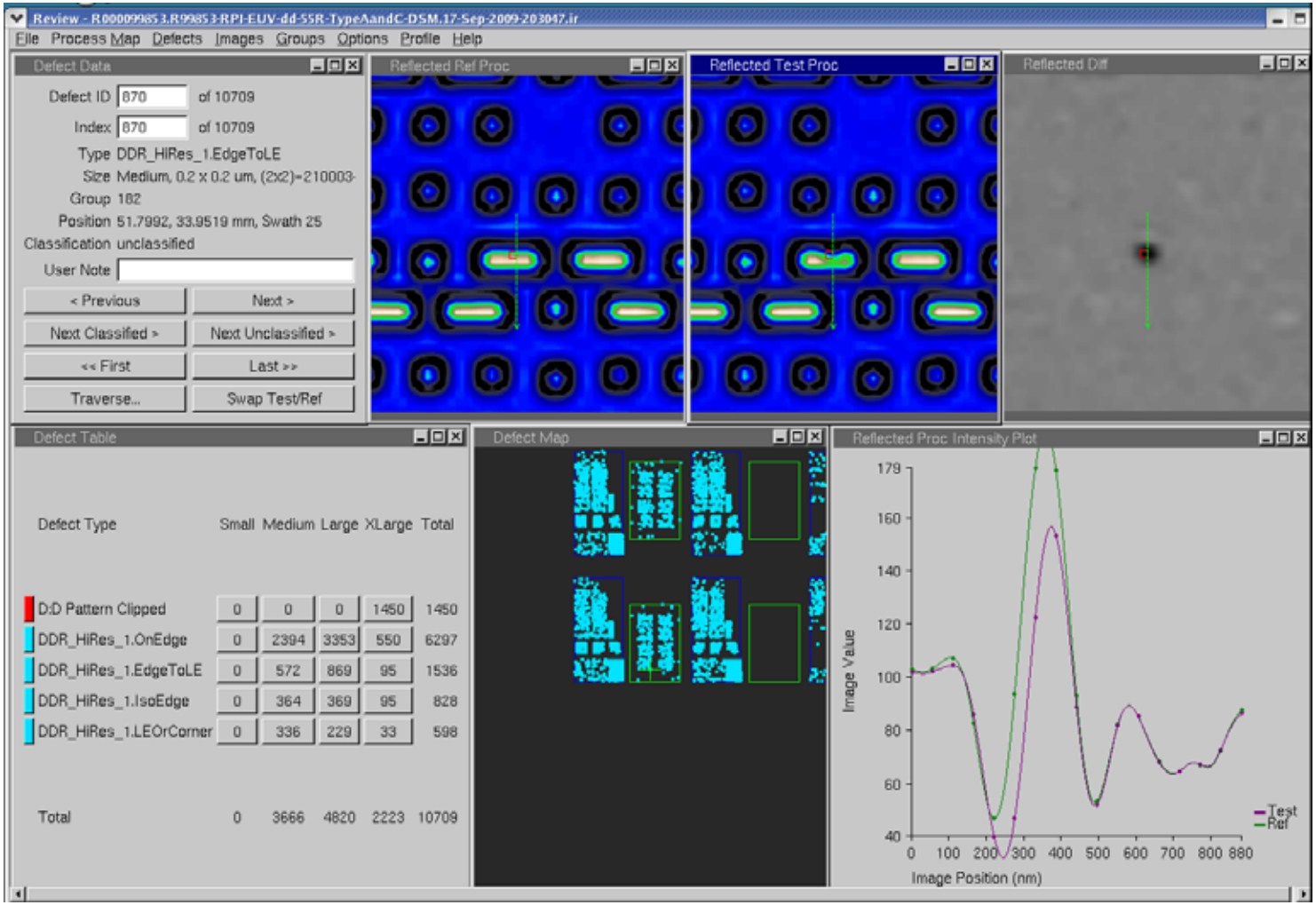

- KT610 can execute inspection on the 22-nm Hole layer

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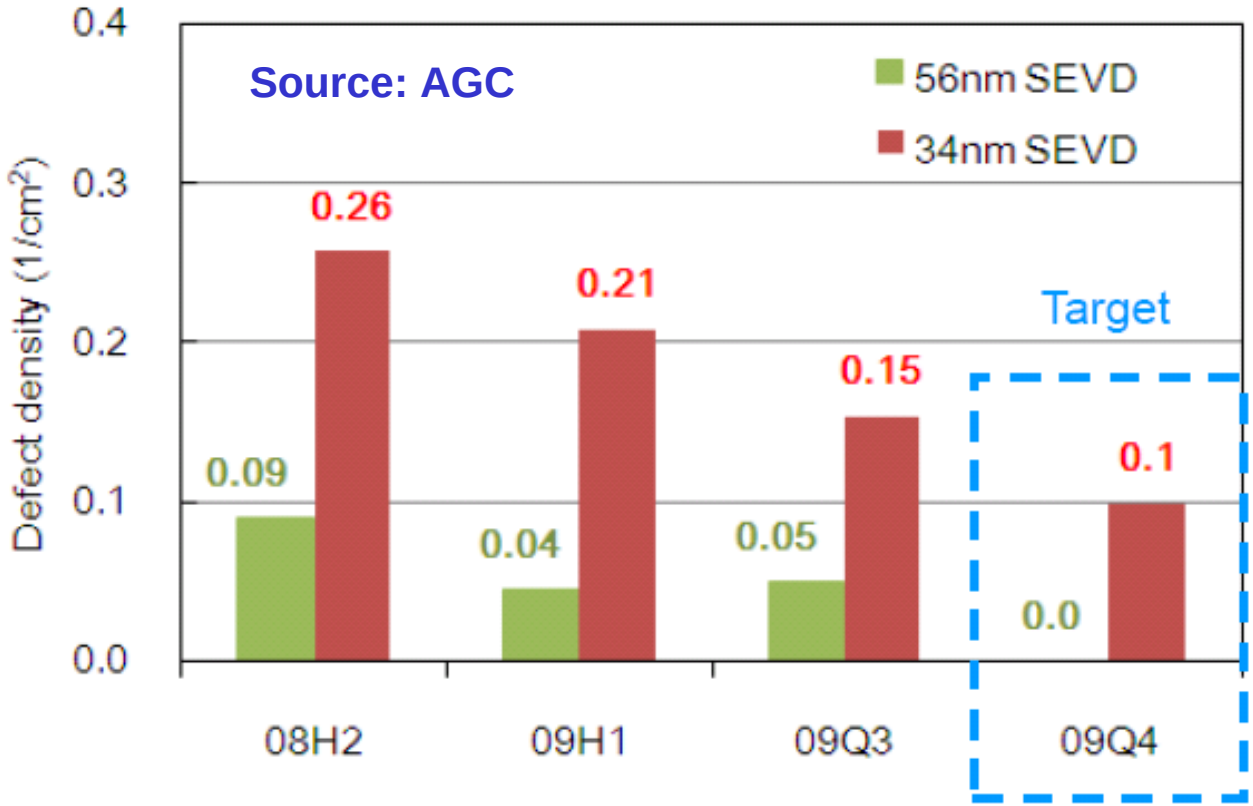
LTEM-ML Blank Defect Trend



- **Goal: 0.01/cm² @ 18 nm**

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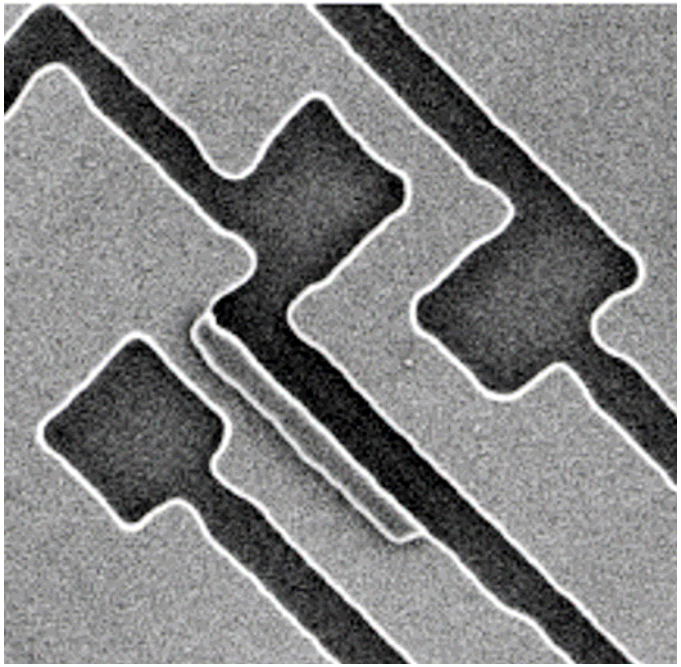
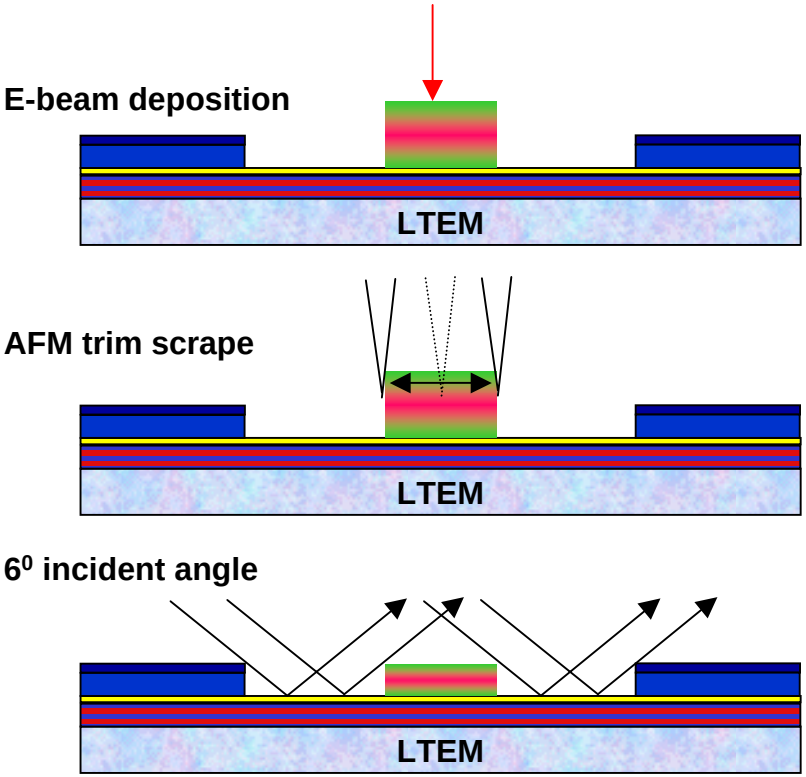
Challenges in EUV Mask Repair - Deposition





- Need accurate 3-D profile control of deposited area
- Need image verification by actinic AIMS tool

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Actinic Mask Metrology Tools Required for HVM

User funding of NRE is necessary

- Actinic BI, AIMS, and PMI tools are required for HVM of EUV masks
  - Consensus by SEMATECH EUV Mask TWG
- User funding of NRE is required in order to build these tools in time
  - Consensus by SEMATECH EUV Mask BWG
- A scenario

Tool	Blank Inspection Tool			EUV AIMS Tool			Patterned Inspection Tool		
Total NRE	$40M			$70M			$150 - $250M, average $200M		
Year	2010	2011	2012	2010	2011	2012	2011	2012	2013
User funding	10%	20%	20%	10%	30%	30%	10%	20%	20%
User funding in $	$4M	$8M	$8M	$7M	$21M	$21M	$20M	$40M	$40M

- Each user's share, assuming six contributing parties

Year	2010	2011	2012	2013	Total
Cash Out	$2M	$8M	$12M	$7M	$29M

- NRE funding recouped through future tool sales

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EUV Lithography Processing Development

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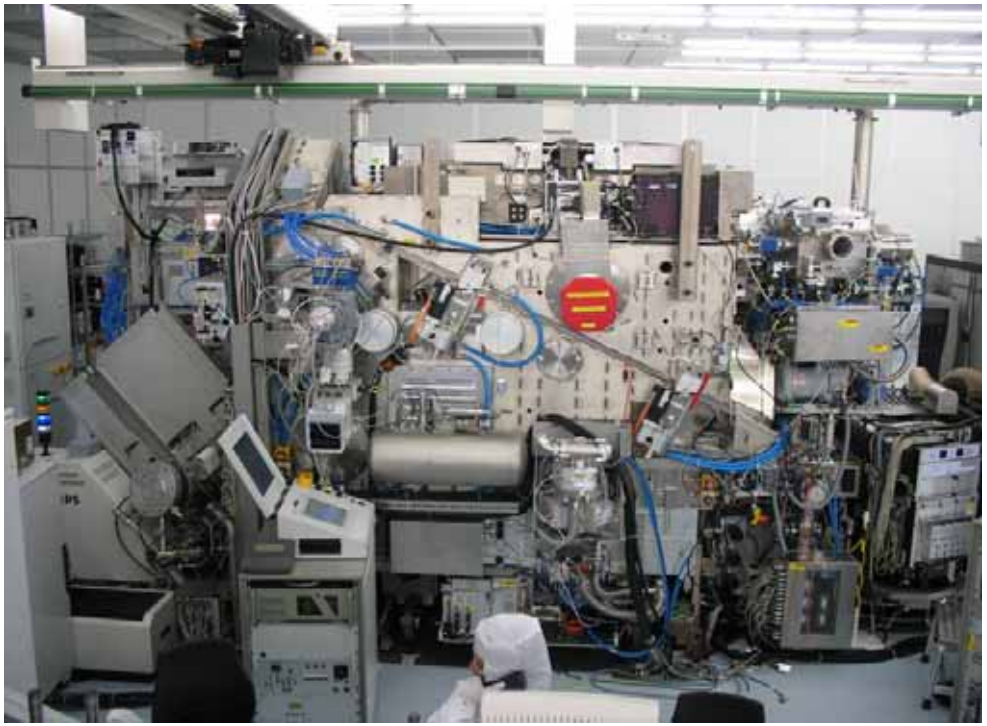
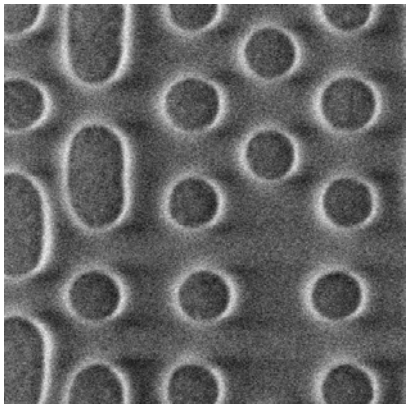
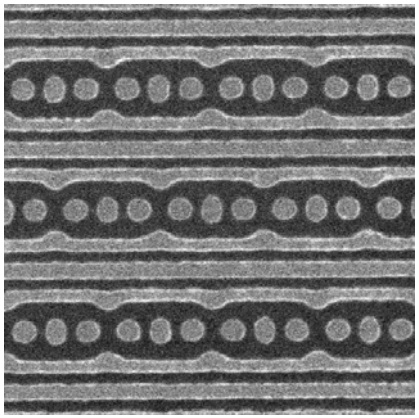
Alpha Demo Tool (ADT) at IMEC



Contact Layer of 32-nm Logic



Metal-1 Layer of 20-nm Logic



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EUV Processing Window for 28-nm Logic

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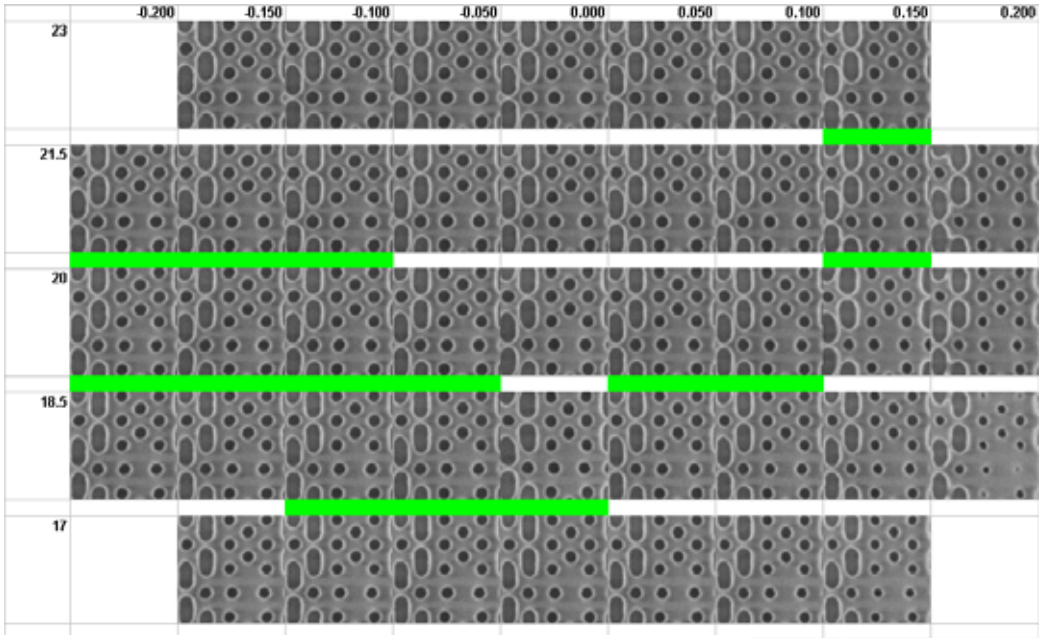

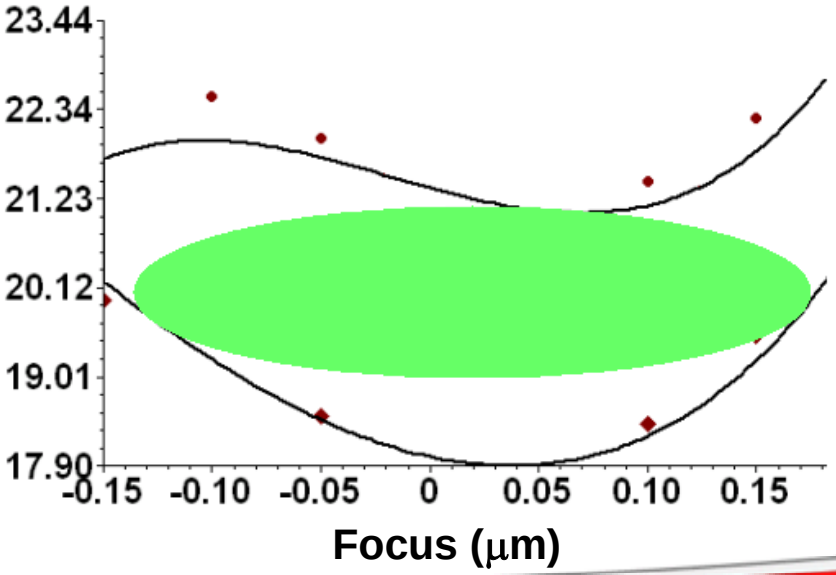

- **DOF: > 0.3 μm**

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EUV Processing Window for 22-nm Logic

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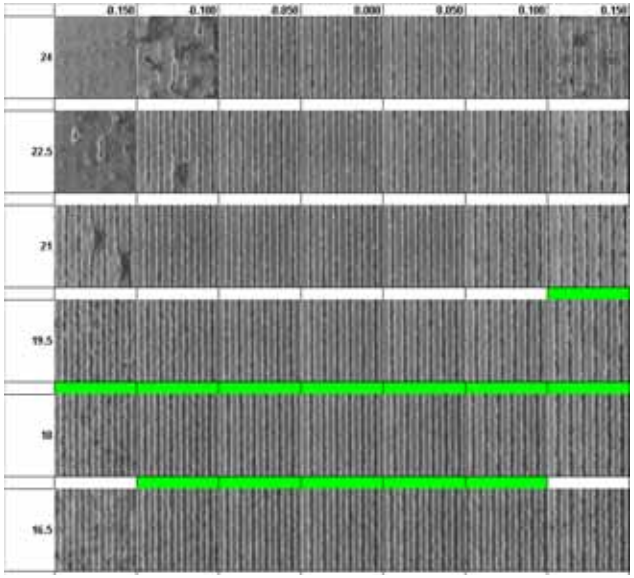

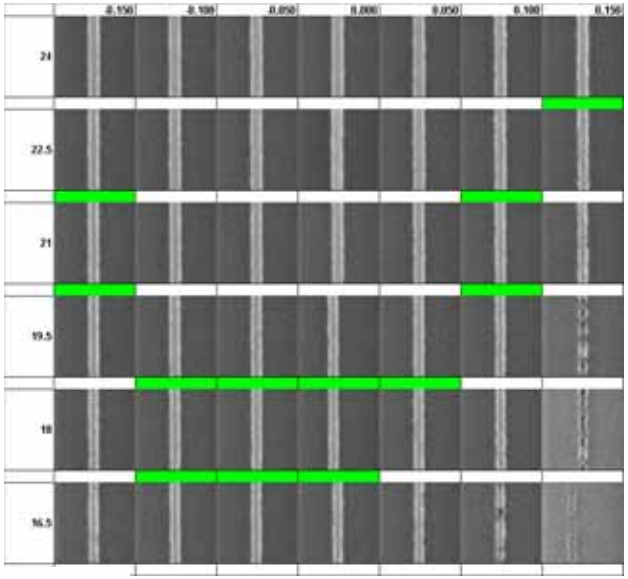

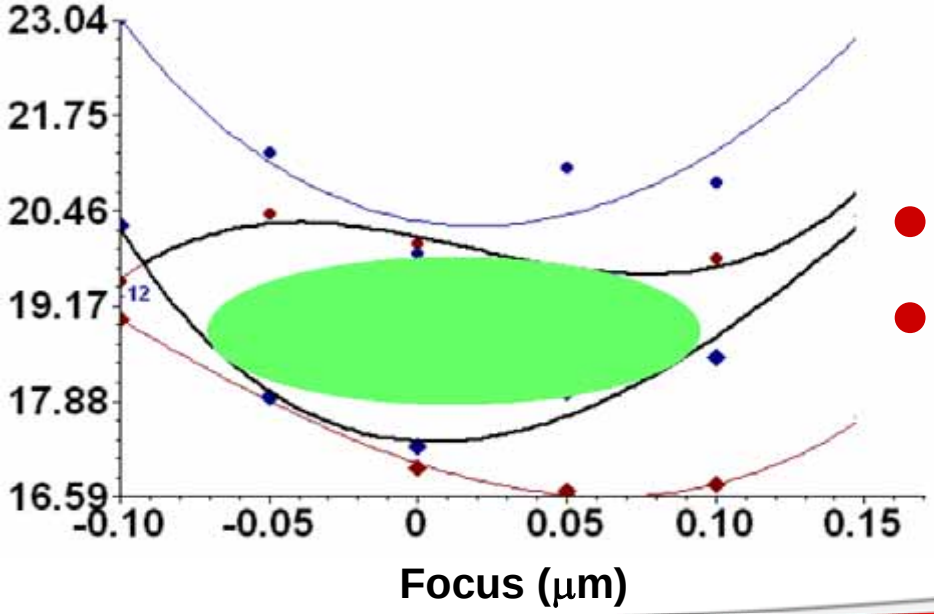

- **Common DOF: > 150 nm**
- **Common EL: ~10%**

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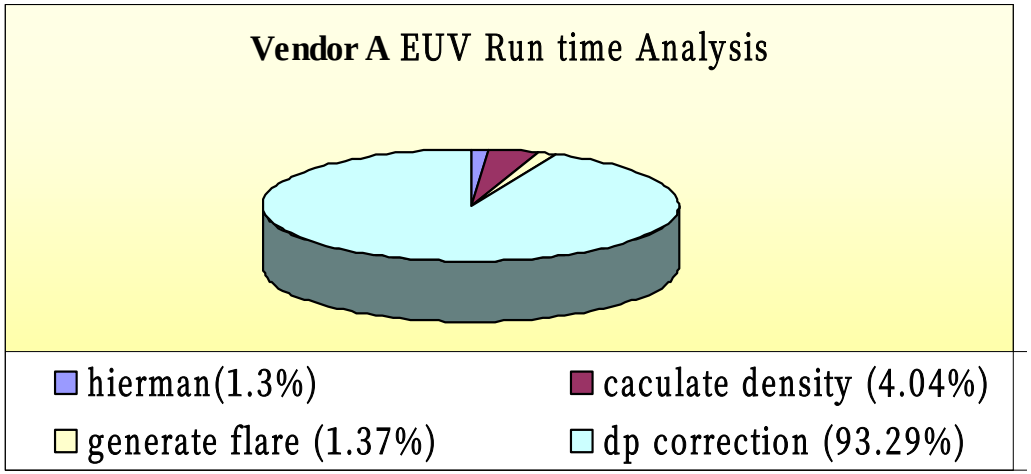
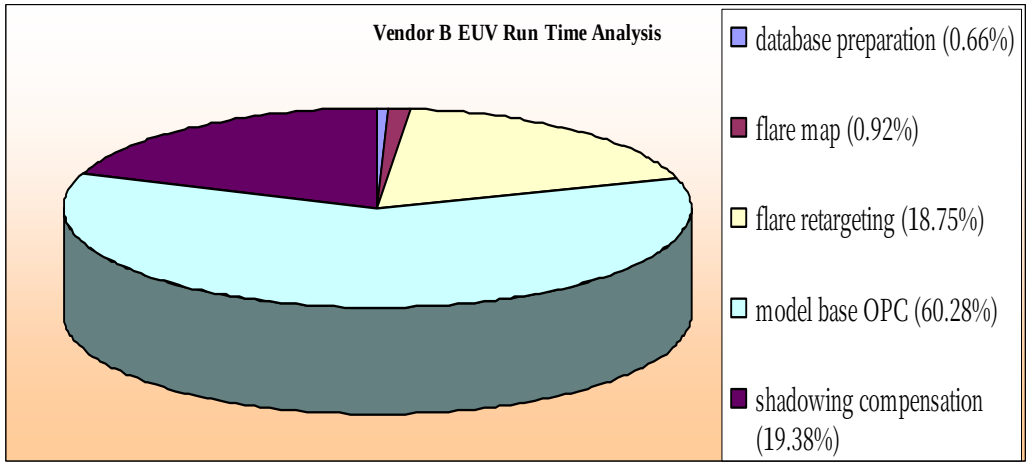
EUV OPC Run Time Test Results





	Run time	Run time in sec (120cpus)	Run time in hrs (120cpus)
Vendor A	154169(40cpus)	51389	14.27
Vendor B	208319 (28cpus)	48607	13.50

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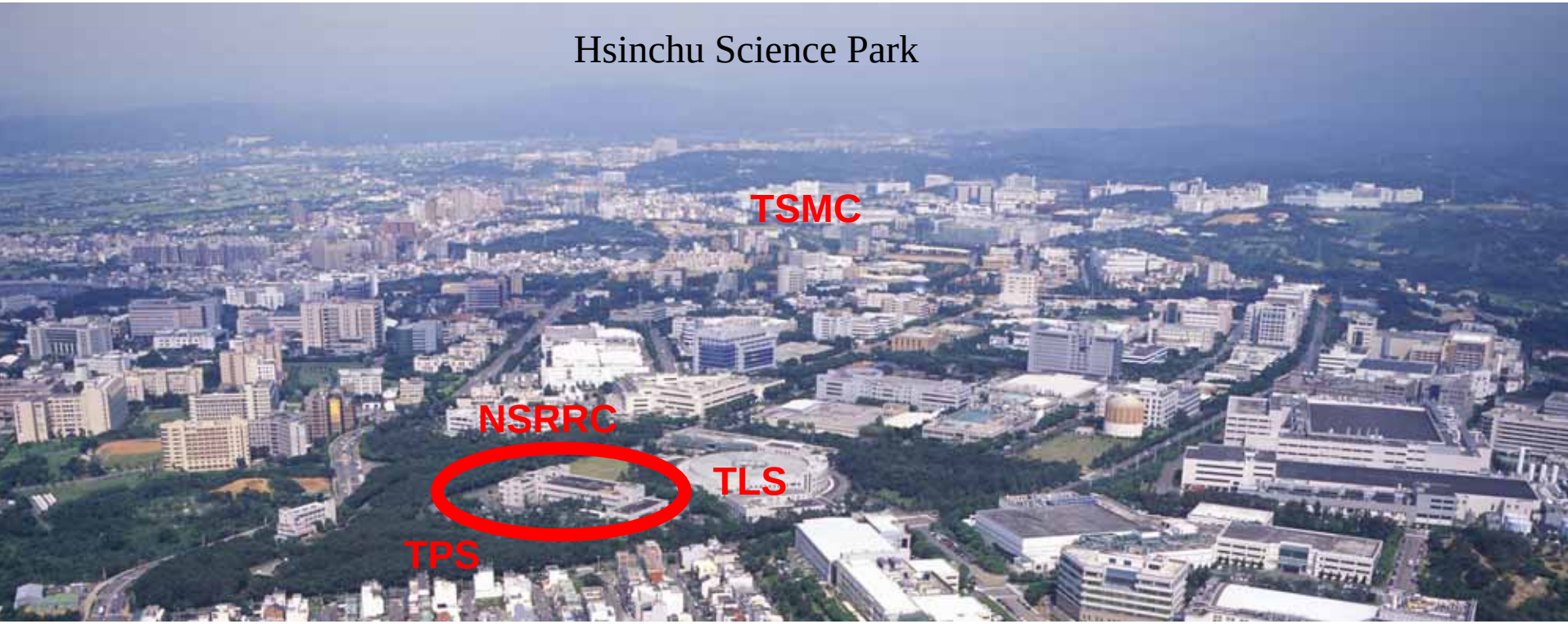
EUV Resist-Related JDPs Planned



NSRRC: National Synchrotron Radiation Research Center
TLS: Taiwan Light Source (open to users in 1993)
TPS: Taiwan Photon Source (will be open to users in 2013)

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EUV Research Activities in Taiwan

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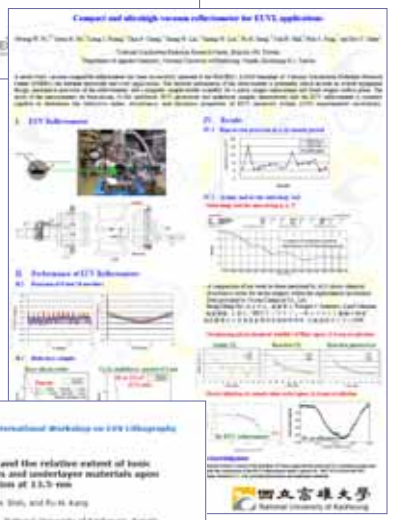

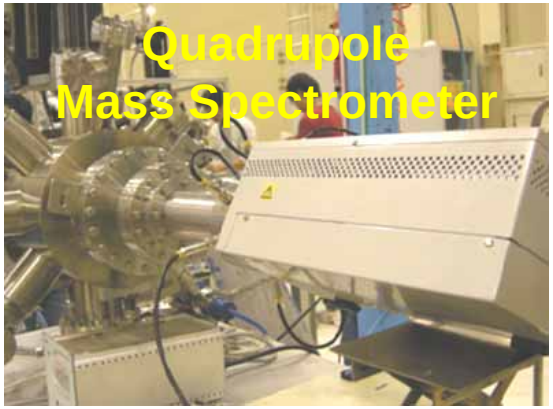

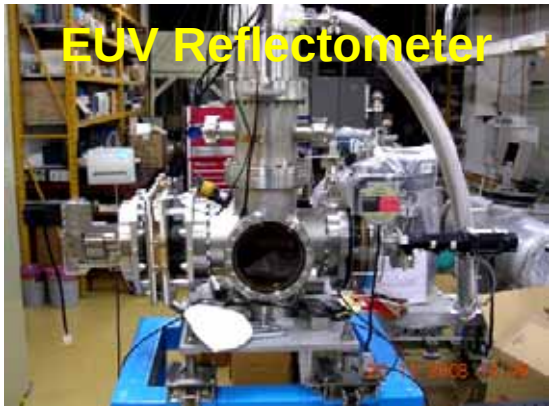

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Acknowledgement

- TSMC Nano Patterning Technology Division
  - Burn Lin, Y.C. Ku, T.S. Gau, R.G. Liu, Angus Chin, Vincent Lee, Alex Chen, Luke Hsu, James Chu, T.C. Lien, Y.T. Tsai, Boren Lo, C.H. Chang, Jimmy Hu
- TSMC Manufacturing Technology Center
  - John Lin, H.J. Lee, R.C. Peng, Tony Wu
- IMEC/ASML
  - Kurt Ronse, Hans Meiling, Jan Hermans, Andre van Dijk

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“Once more unto the breach, dear friends, once more.”

– Wm. Shakespeare, in Henry V, quoted by Dr. Morris Chang in TSMC Q2 2009 Analyst Meeting