Progress in full field EUV lithography program at IMEC

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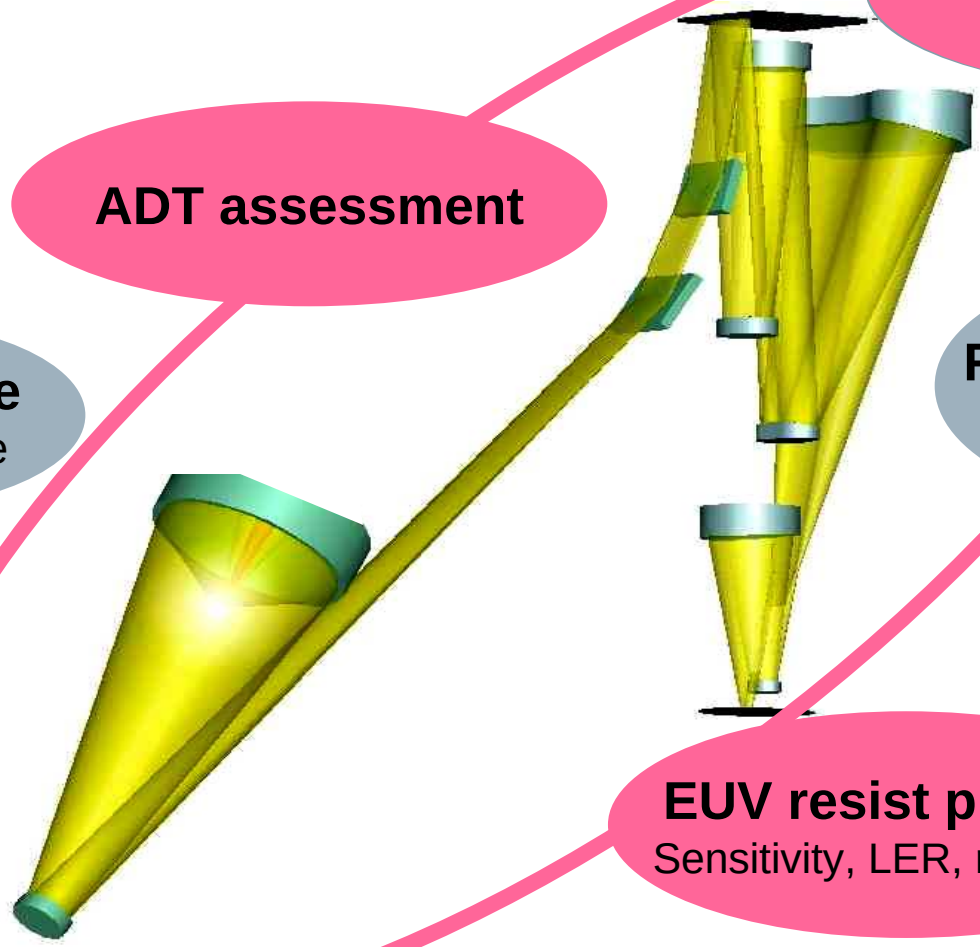
[4]On assignment from Micron
[5]On assignment from Qimonda

International EUVL Symposium, 28-31 October 2007, Sapporo

EUVL program contents vs EUV critical issues
3 projects



EUV masks
Handling in fab

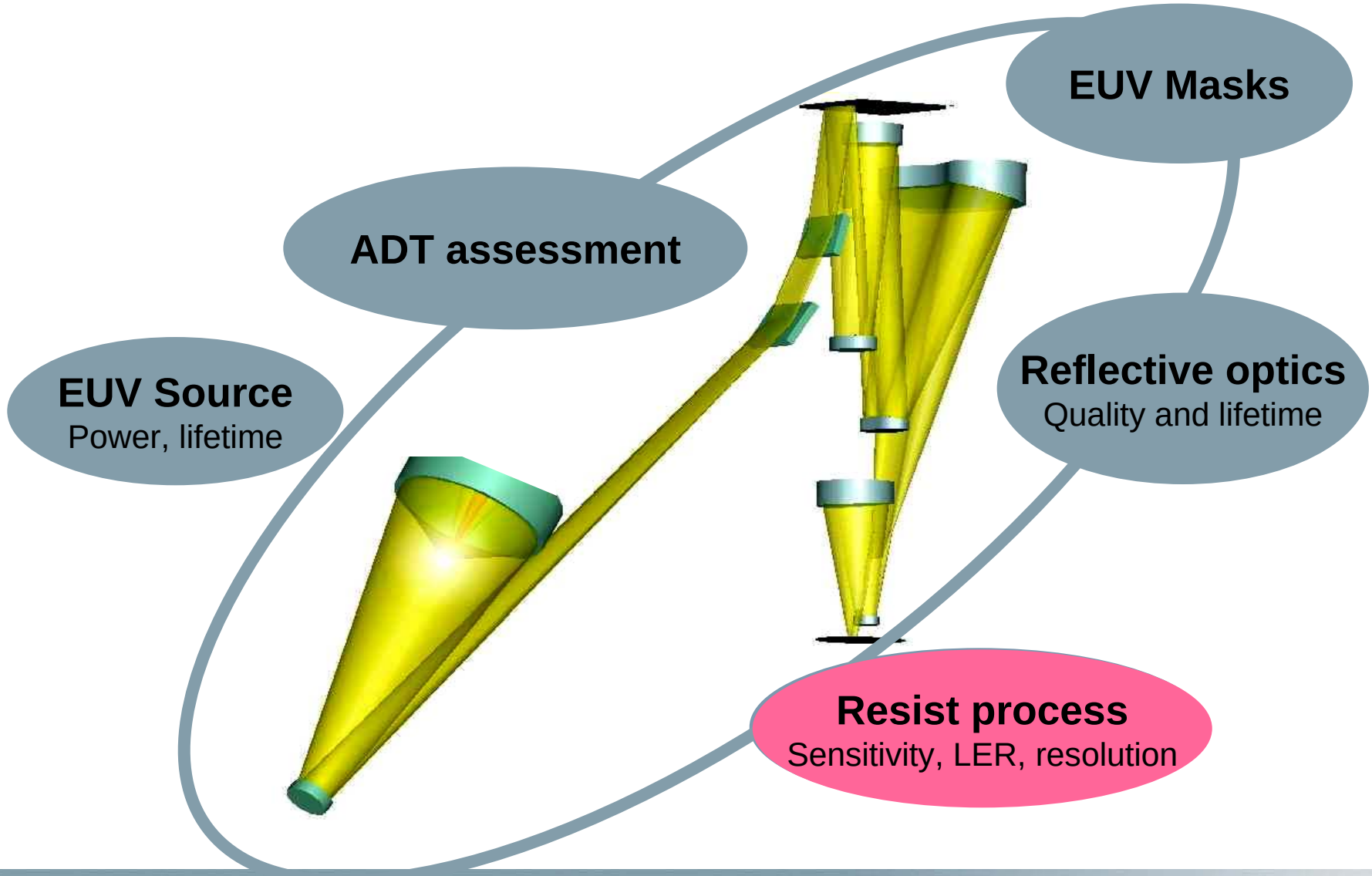
ADT assessment

EUV Source
Power, lifetime

Reflective optics
Quality and lifetime

EUV resist process
Sensitivity, LER, resolution

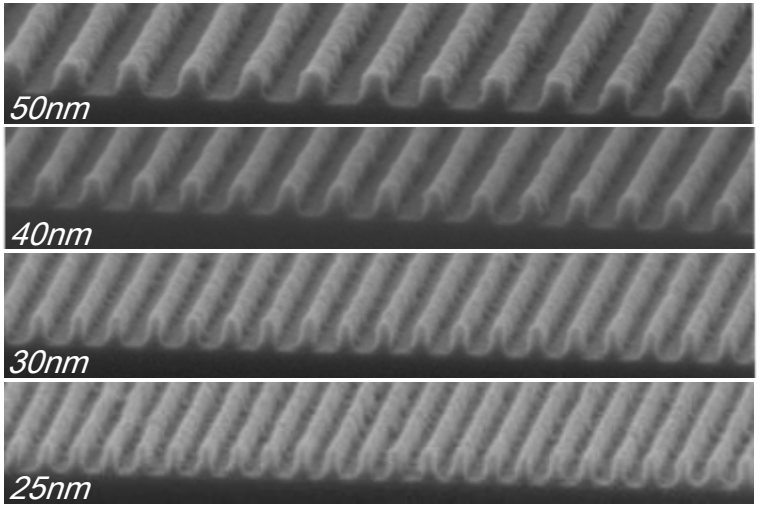
EUVL program contents
EUV resists



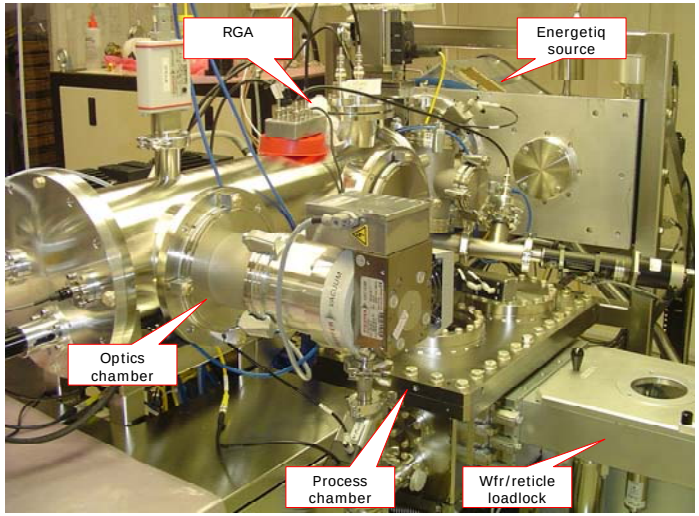
EUV resist project
Key objectives

- EUV resists
  - Benchmark EUV resist performance versus requirements
  - Drive EUV resist suppliers
  - Demonstrate EUVL ability for small electrically working circuits
  - Build fundamental understanding for EUV resist out-gassing requirements for EUVL high volume manufacturing

in close collaboration with all major resist suppliers worldwide



Resist Screening at PSI

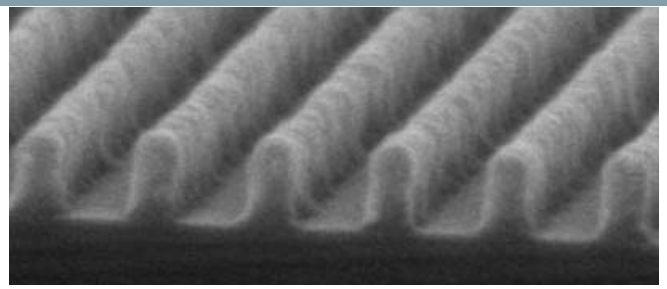


EUV Technology Outgassing Tool

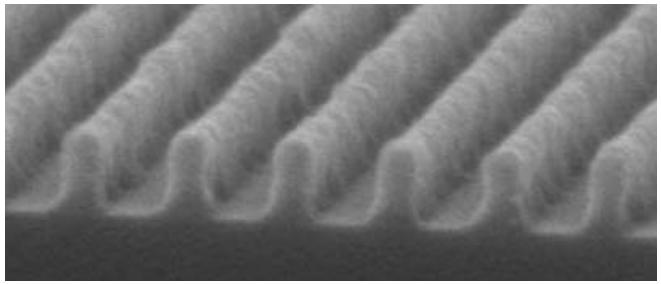
Reference resist (Interference litho)

MET-2D, 80nm resist thickness

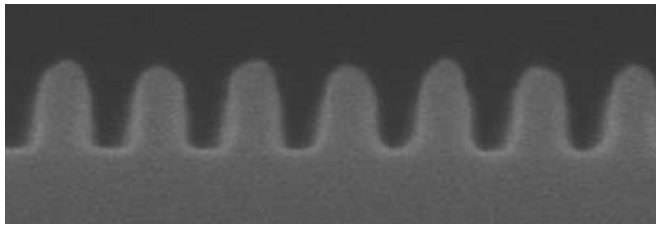
50 nm
(80nm thick)



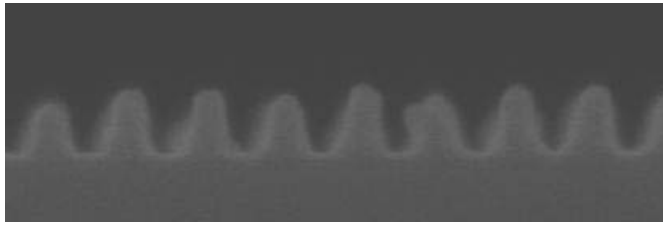
45 nm



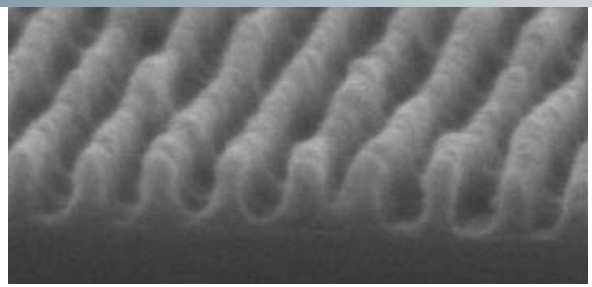
40 nm



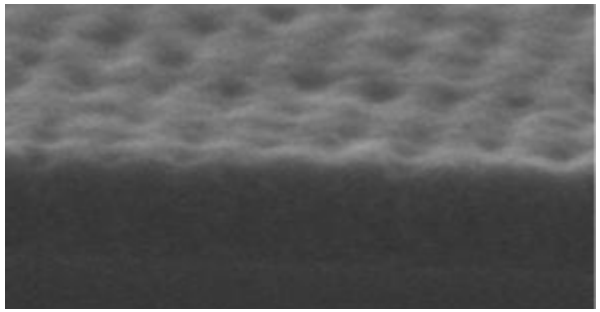
32.5 nm



30nm

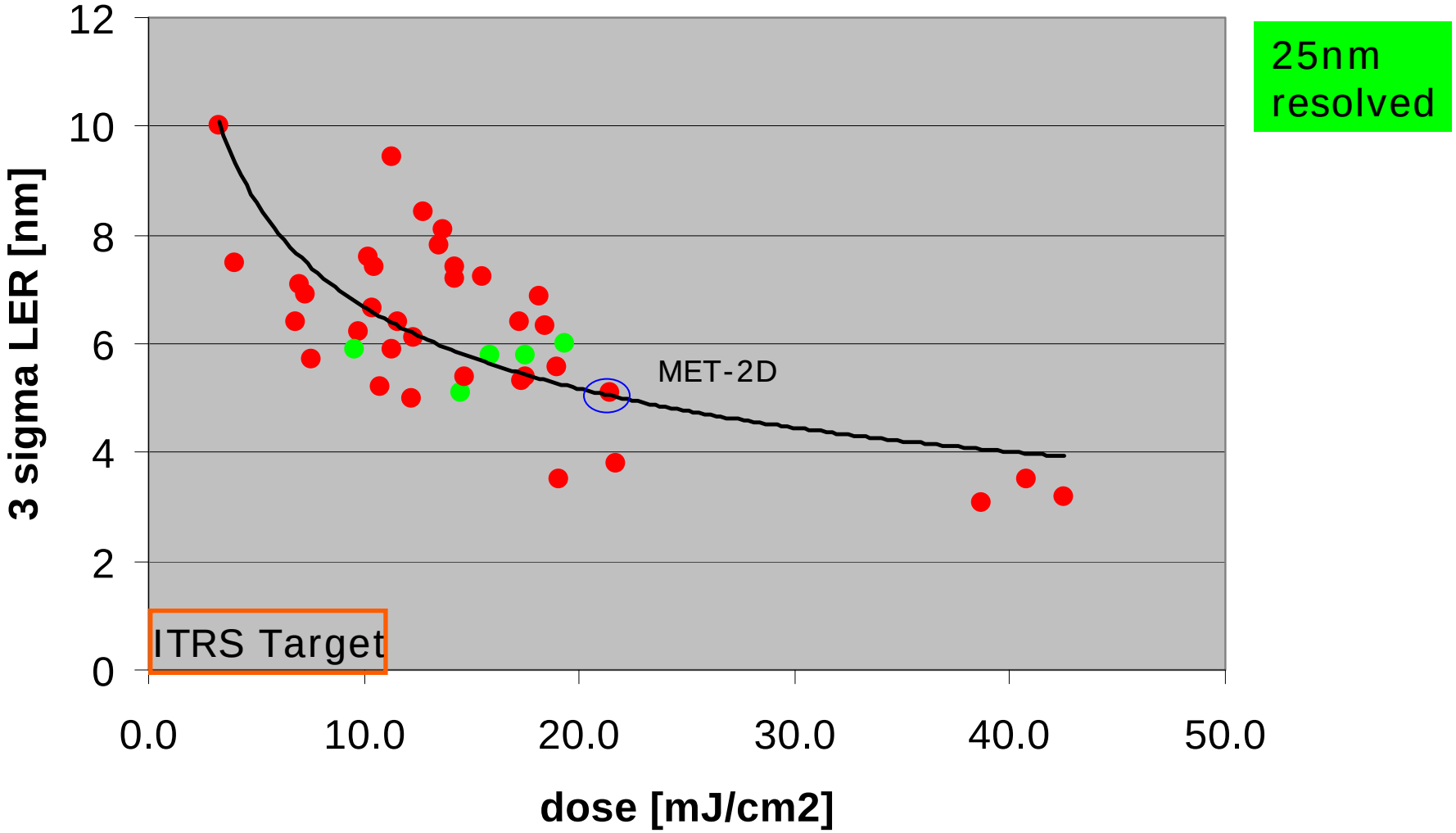


25nm



$Energy_{size}$	**21.4 mJ/cm²**
Exp. Lat. (50nm)	13%
LER (3σ) (50nm)	**5.1nm**
Resolution	**32.5 nm**

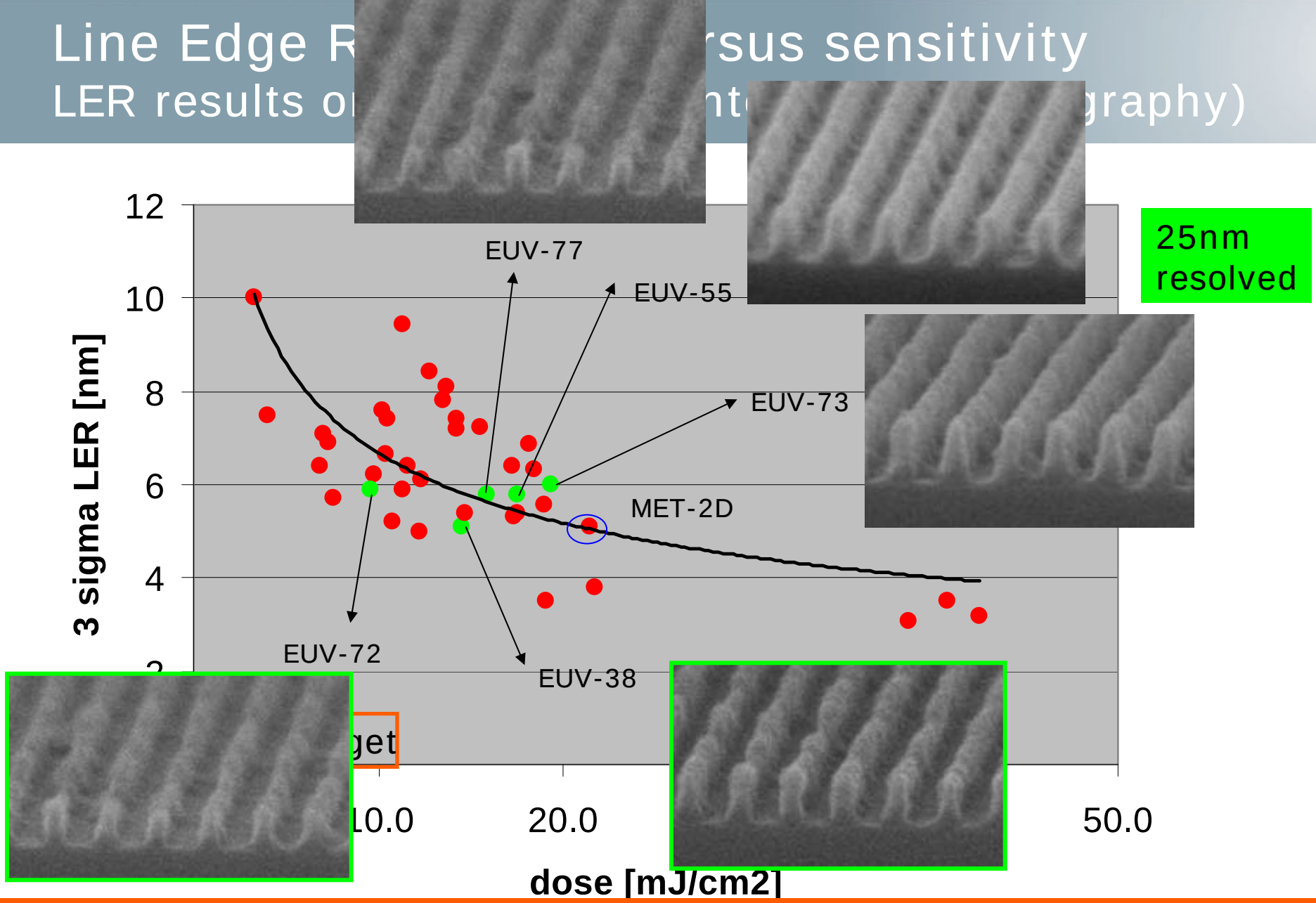
Line Edge Roughness versus sensitivity
LER results on 50nm lines (Interference lithography)



Poster RE-P10 "EUV resist process development for full field imaging", A. Niroomand et al

Line Edge R rsus sensitivity

LER results o nt graphy)

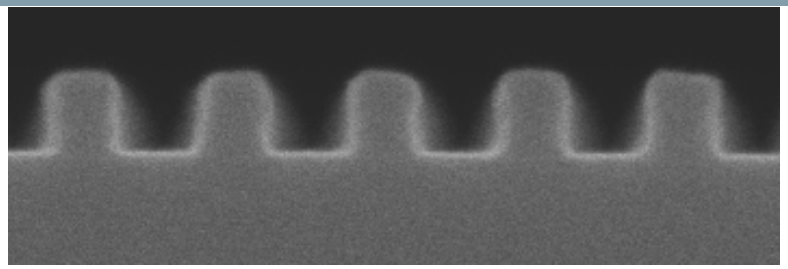


Best overall performing resist is EUV-72 (high sensitivity with ~25nm resolution).

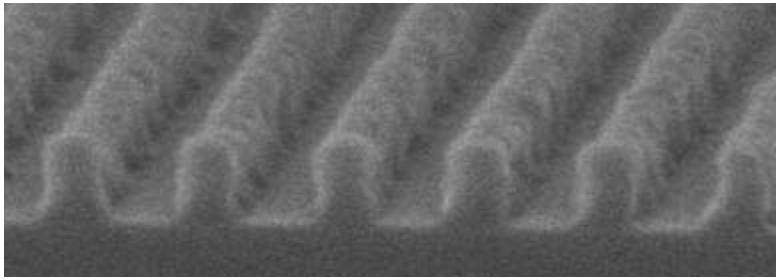
State of the art resist Q3 2006

EUV-38 resist

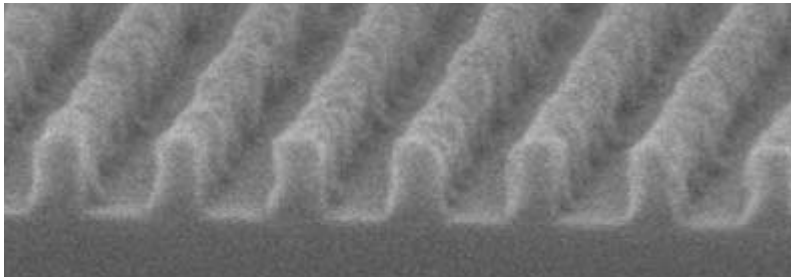
50 nm



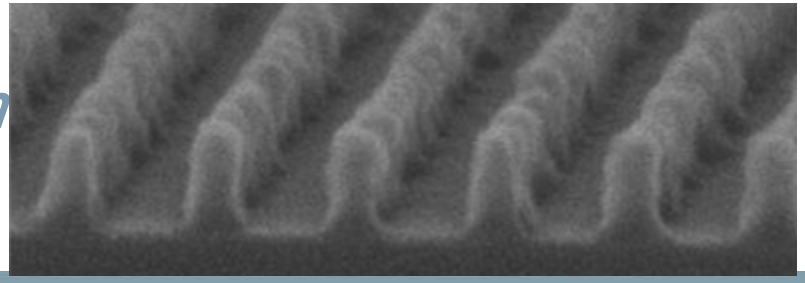
45 nm



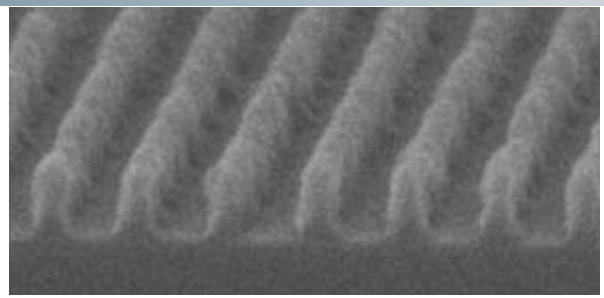
40 nm



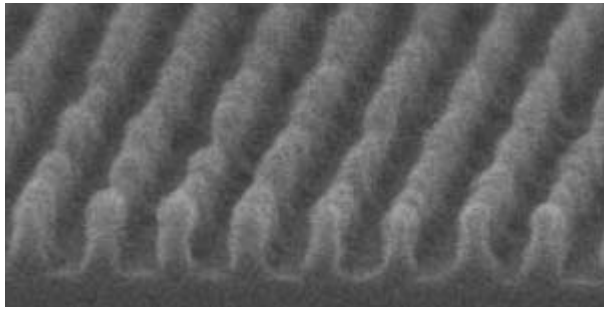
32.5 nm



30nm



25nm

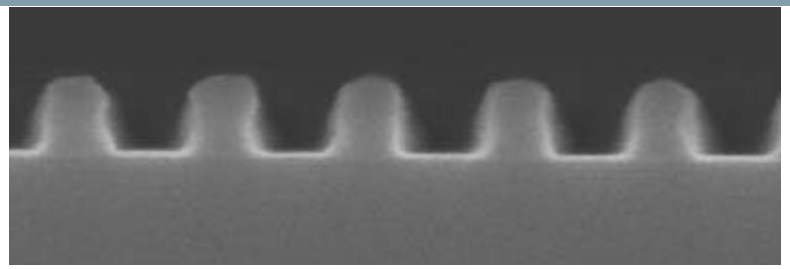


$Energy_{size}$	**14.8 mJ/cm²**
Exp. Lat. (50nm)	26%
LER (3σ) (50nm)	**5.2nm**
Resolution	**25nm**

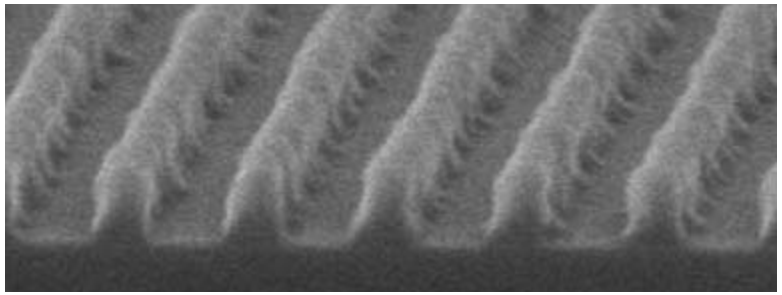
Overall best resist Q3 2007

EUV-72 resist

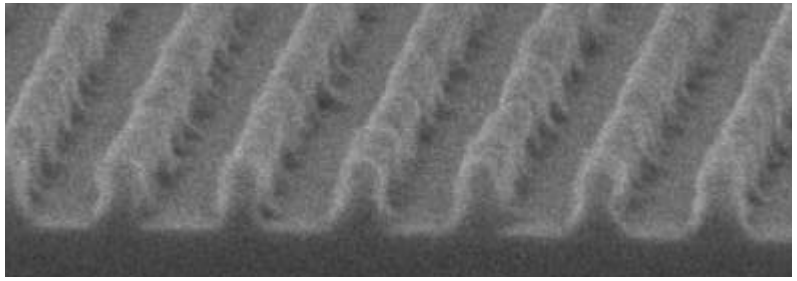
50 nm



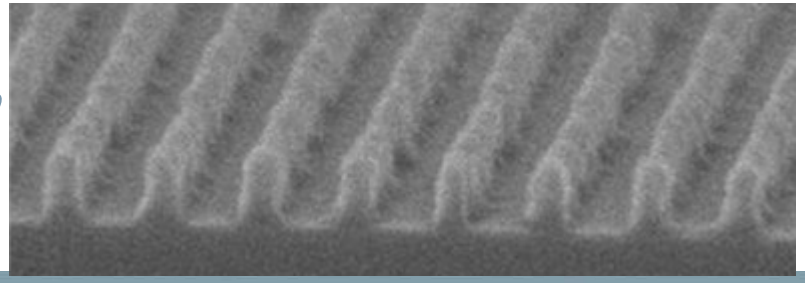
45 nm



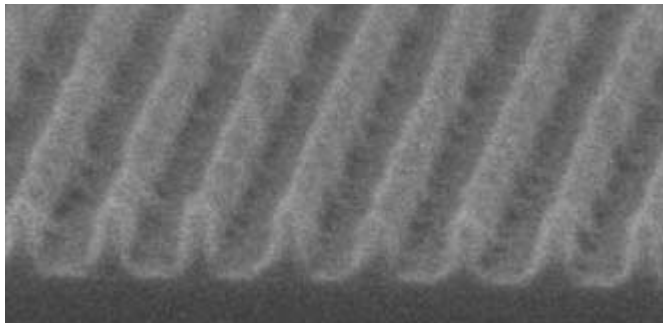
40 nm



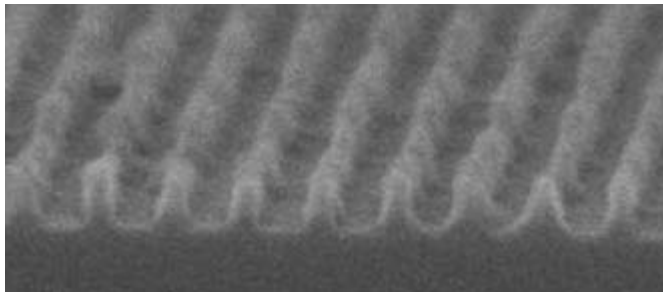
32.5 nm



30nm

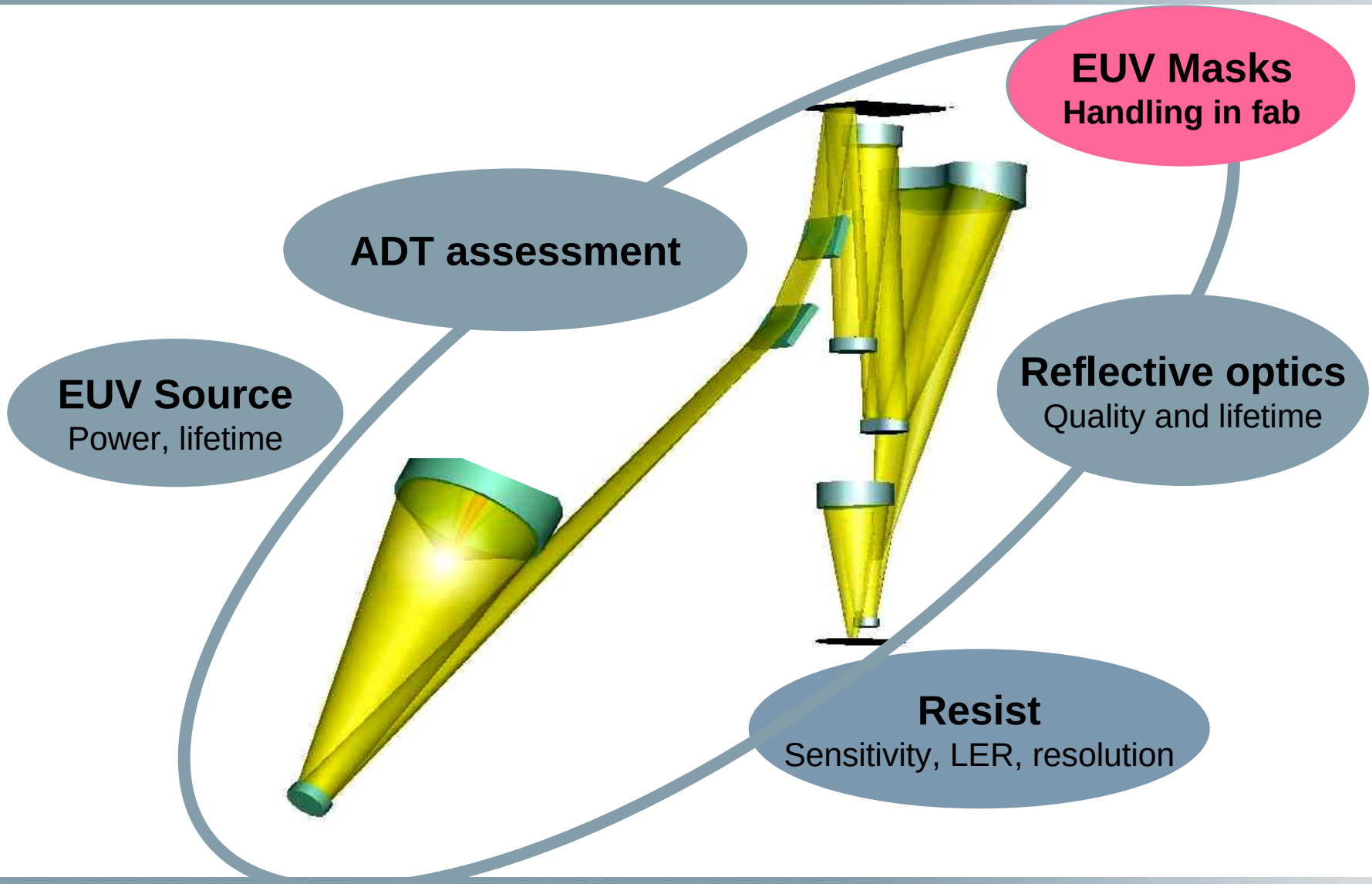


25nm



$Energy_{size}$	**9.6 mJ/cm²**
Exp. Lat. (50nm)	27%
LER (3σ) (50nm)	**5.9nm**
Resolution	**~25 nm**

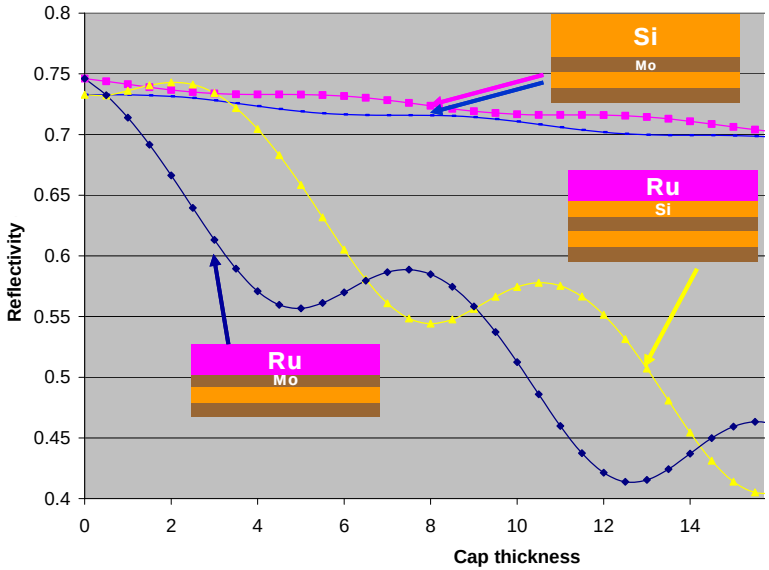
EUVL program contents
EUV reticles Project



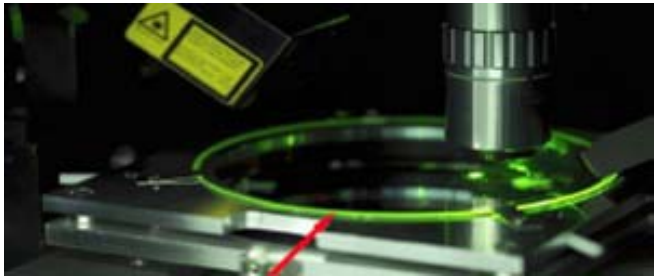
EUV reticle project
Key objectives

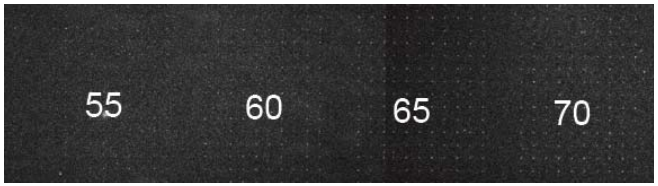
- 2. EUV masks
  - Benchmark EUV reticle performance versus requirements and blank architecture
  - Build understanding on handling requirements for EUV mask lifetime in fab environment
  - Build understanding on EUV mask defect specs requirements for defect free lithography

in close collaboration with all major EUV mask (and blank) suppliers worldwide (including captive mask shops core partners)



Blank reflectivity simulation

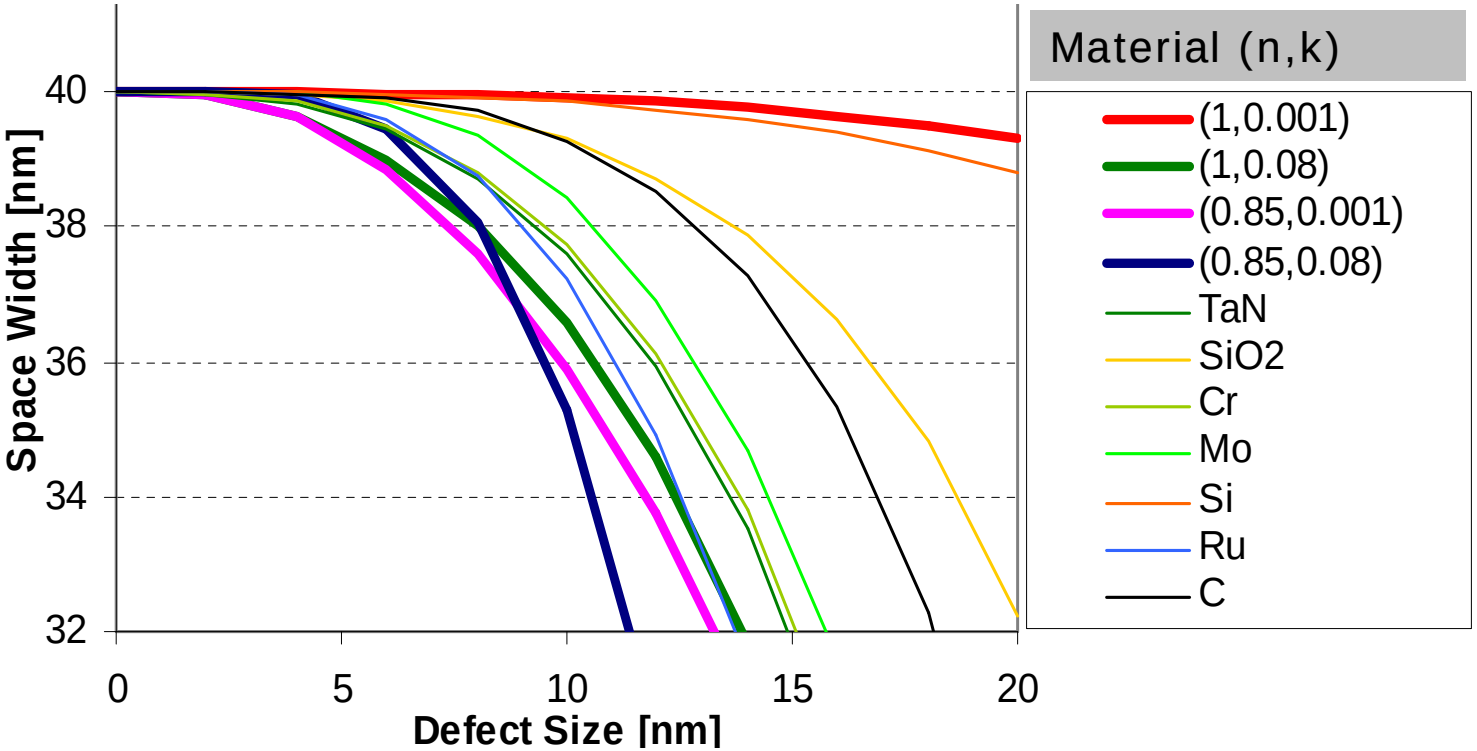




TNO Particle Scanner

DNP TOPPAN HOYA AGC

Particle defect: variation of n&k



The particle material determines its printability.

oral DI-01 "Mask defect printability in full field EUV lithography", R. Jonckheere

Printability study of 4 types of mask defects by simulation

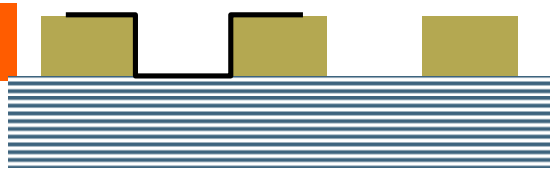
Particle

eg Carbon or opaque materials defect
Critical particle size is ~14nm for C
Printability depends on (n,k)

Absorber defect

Opaque & clear type
Critical opaque defect size: is ~8nm
Critical distance is typically 2-3X smaller than in ArF

Local R%-loss



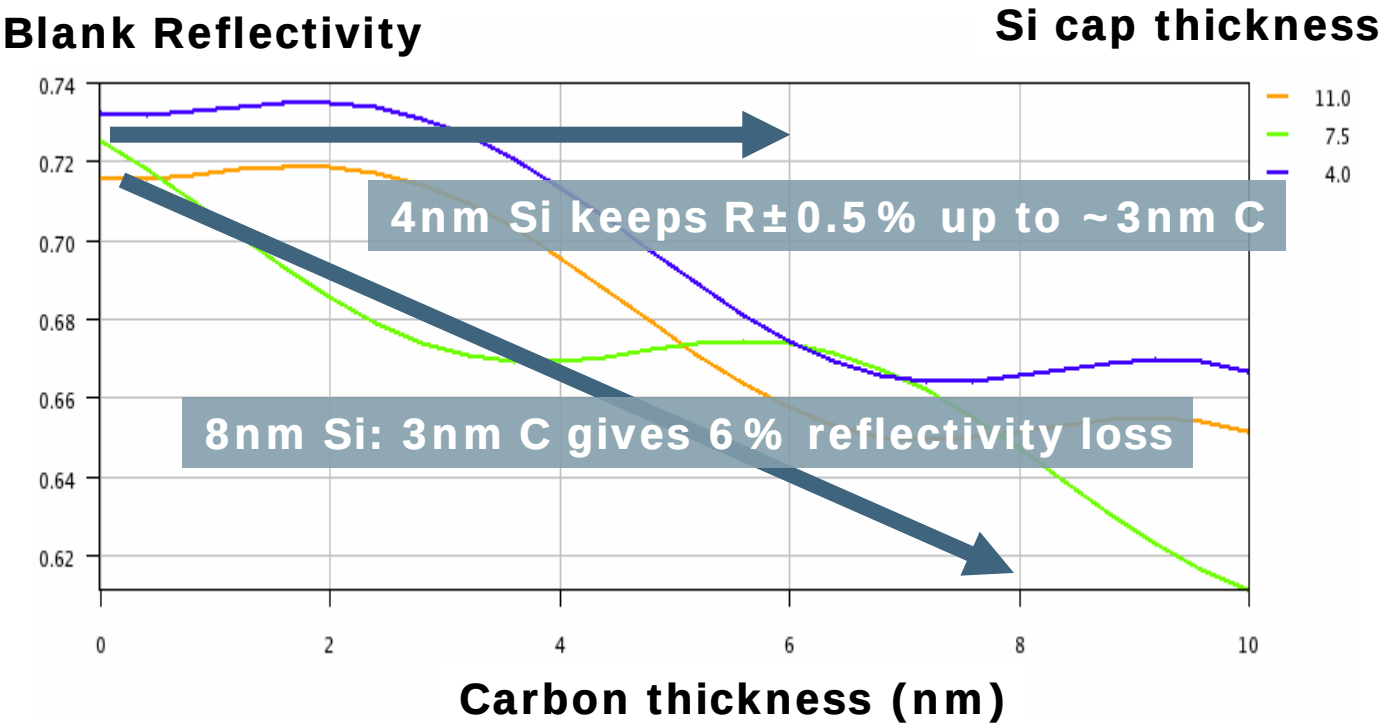
Local carbon deposition
If conformal it prints very quickly (from 2nm thickness onwards)

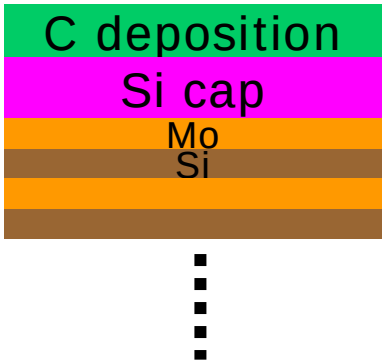
ML defect

Major effect from multilayer distortion near top (phase defects ~2-3nm).
Material dependence only when the defect is located near the surface.

Oral DI-01 "Mask defect printability in full field EUV lithography", R. Jonckheere

EUV reticle long term reflectivity (degradation)

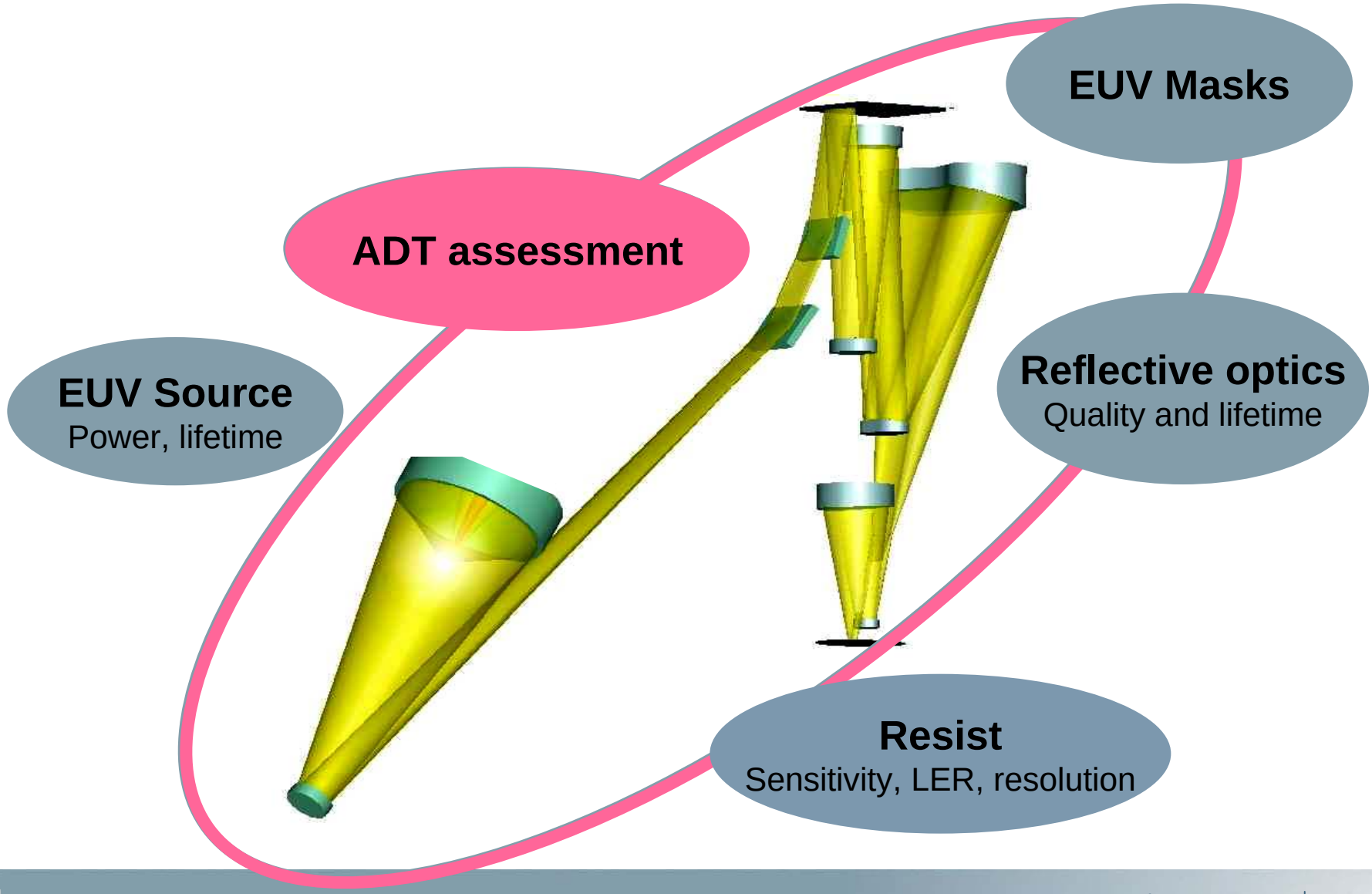




Protective mask capping layer (Si or Ru) and thickness can be optimized to minimize/maximize the sensitivity carbon deposition.

Poster MC-P03 "Study of capping layer impact on reflectivity loss by carbon deposition", Rik Jonckheere et al

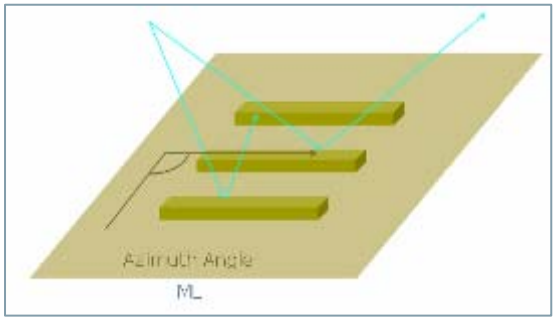
EUVL program contents
EUV ADT assessment project



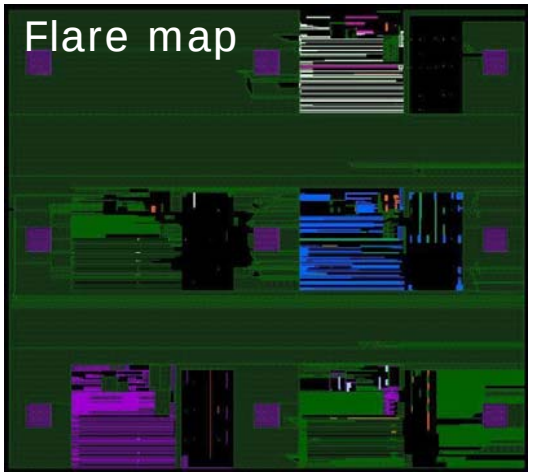
EUV ADT assessment project
Key objectives

- EUV alpha tool assessment
  - Detailed characterization of EUV ADT fingerprint in terms of
    - Imaging
    - Overlay (single machine and matched machine)
  - Detailed stability monitoring of EUV ADT
    - In terms of optics contamination (image degradation)
    - In terms of reliability and up-time (CoO)
  - Develop and demonstrate correction techniques to compensate for EUV shadowing and flare

in close collaboration with ASML

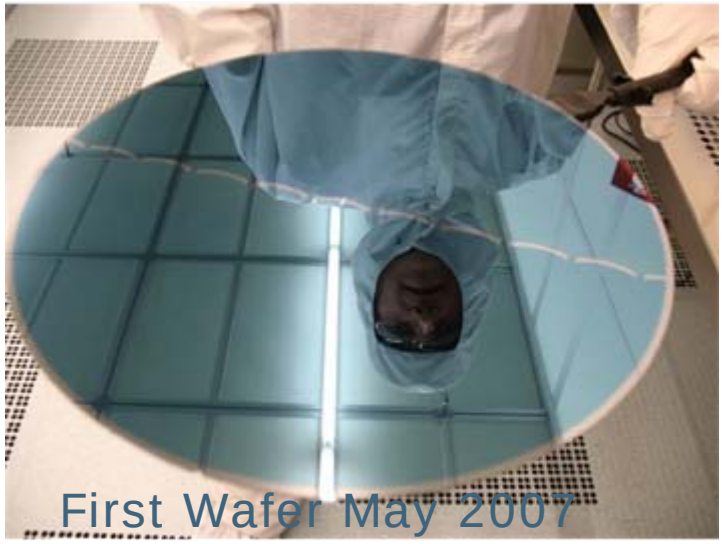


Shadowing Compensation



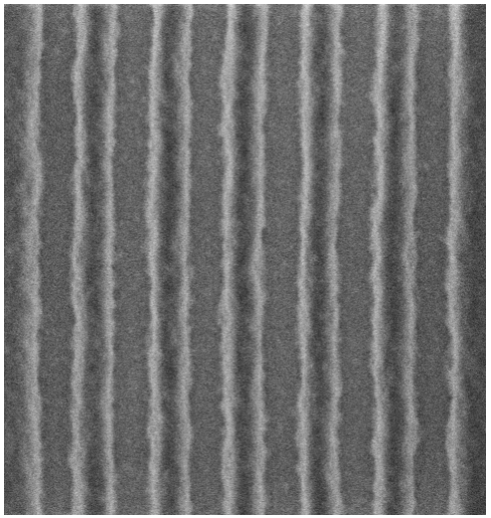
Flare map

ASML EUV Alpha Demo Tool (ADT) at IMEC



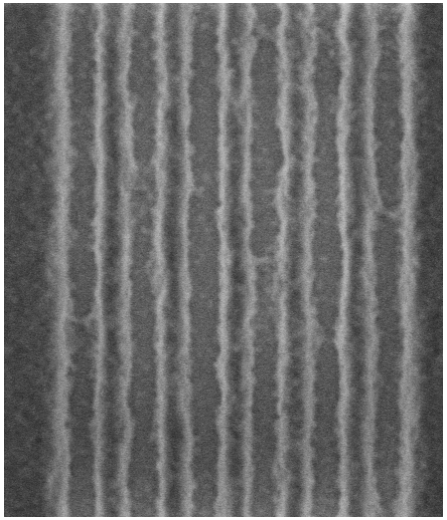
ASML EUV Alpha Demo Tool
First imaging with Sn source

50nm 1:1

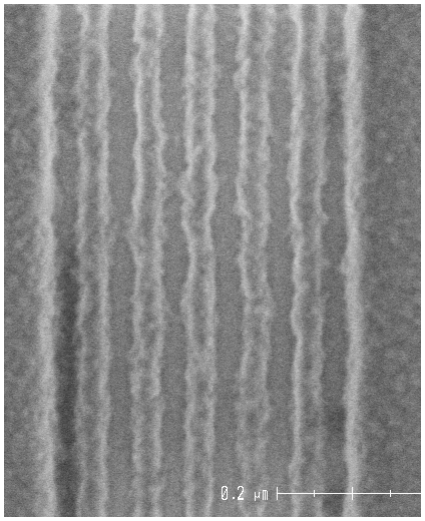


CD=47.3nm

40nm 1:1



35nm 1:1



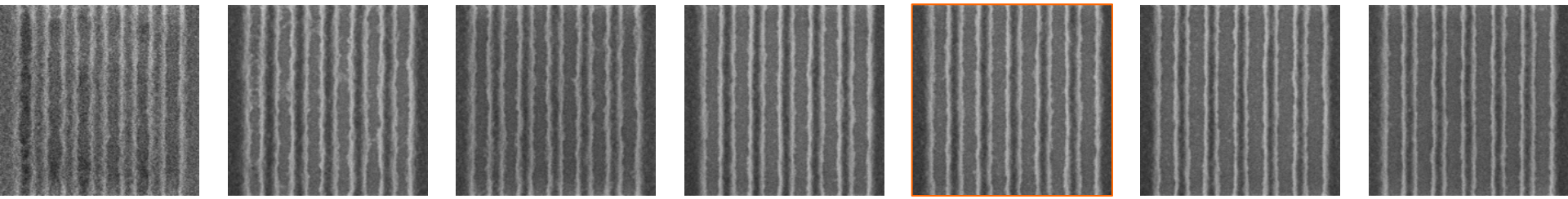
CD=34nm

Resist: Rohm Haas MET-2D
Thickness 100nm
NA=0.25, σ=0.5
Lens aberration reduction not finalized yet

ADT imaging
50nm V and H lines through **dose**

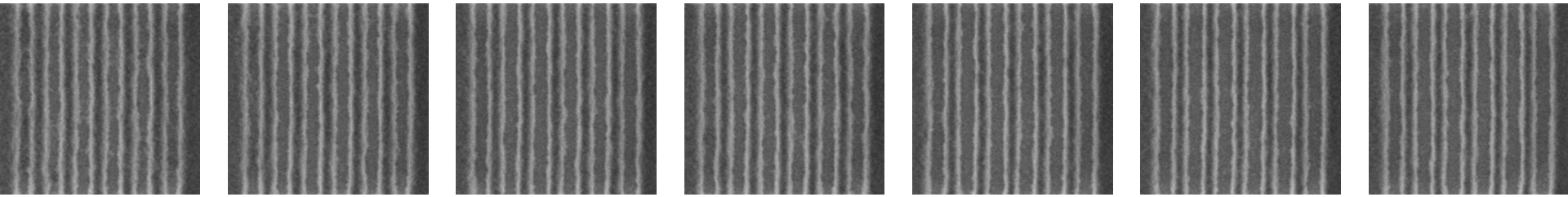
17.05 mJ	17.3 mJ	17.55 mJ	17.8mJ	18.05mJ	18.3mJ	18.55mJ

Vertical lines



57.3nm	59.6nm	52.6nm	52.7nm	51.2nm	45.6nm	46.1nm

Horizontal lines



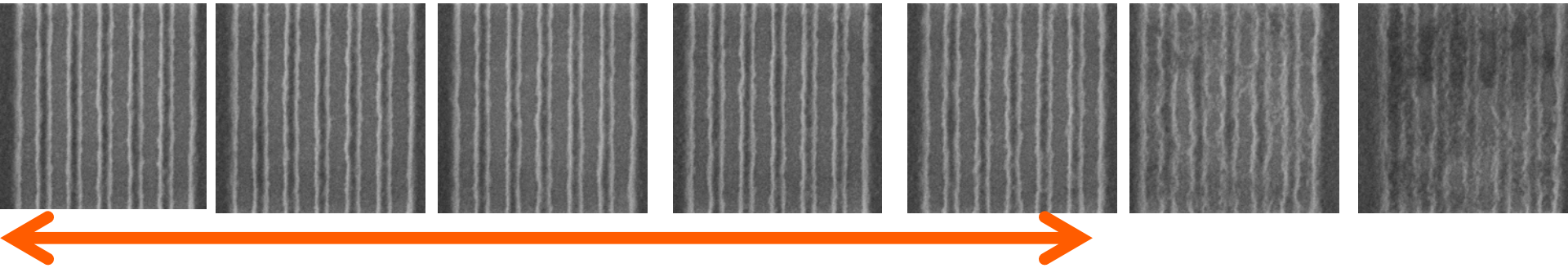
61.9nm	58.3nm	55.8nm	56.4nm	53.8nm	51.6nm	52.4nm

Resist: Rohm Haas MET-2D
Thickness 100nm
NA=0.25, σ=0.5
Lens aberration reduction not finalized yet

ASML

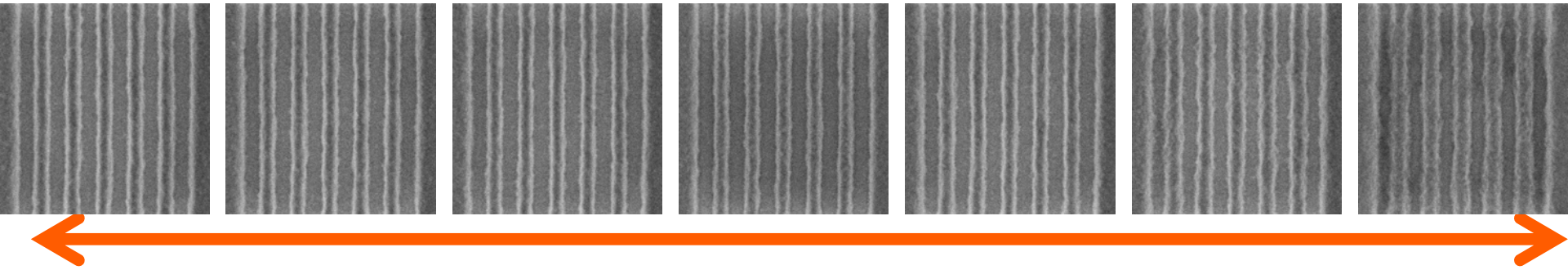
ADT imaging
50nm V and H lines through **focus**

Vertical L/S



>160nm DOF

Horizontal L/S



>240nm DOF

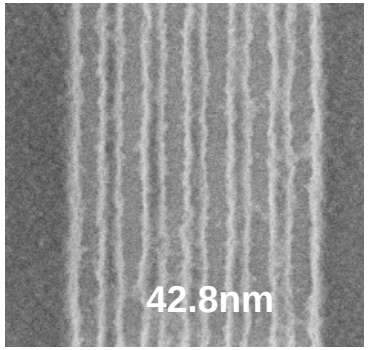
Resist: Rohm Haas MET-2D
Thickness 100nm
NA=0.25, σ=0.5
Lens aberration reduction not finalized yet

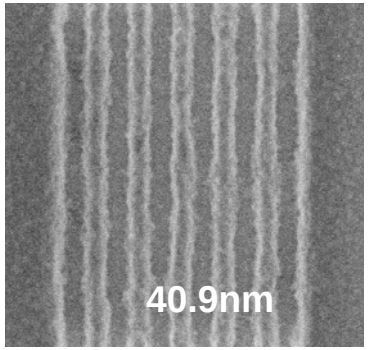
ASML

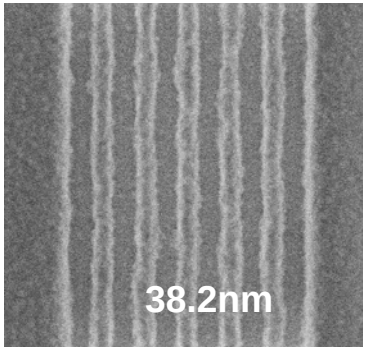
ADT imaging
40nm V and H lines through dose

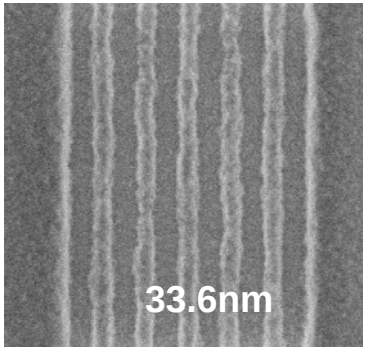
17.55 mJ	17.8mJ	18.05mJ	18.3mJ	18.55mJ

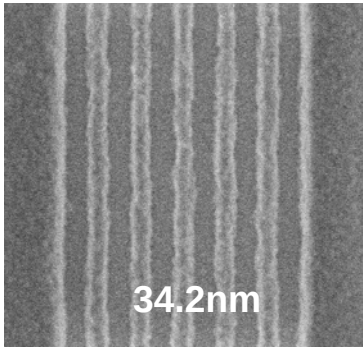
Vertical lines



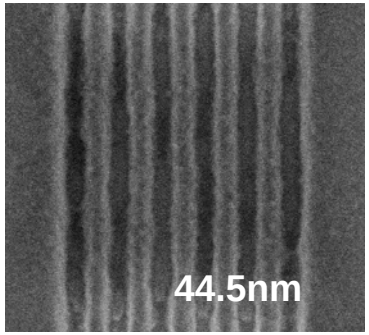


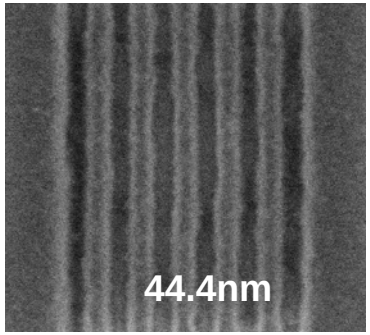


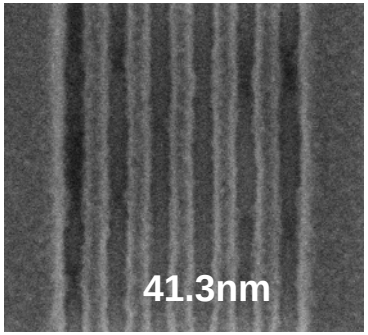


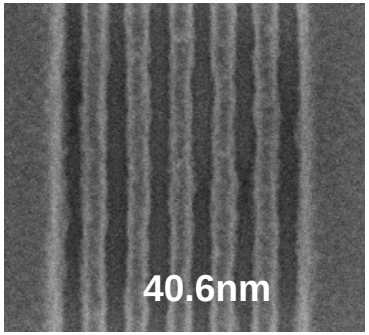


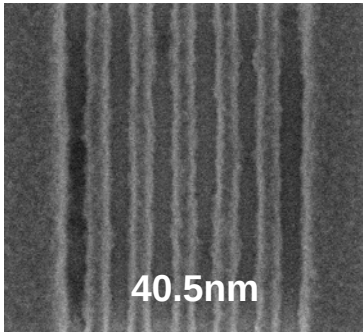
Horizontal lines











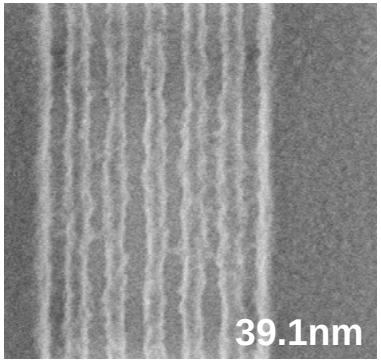
Resist: Rohm Haas MET-2D
Thickness 100nm
NA=0.25, σ=0.5
Lens aberration reduction not finalized yet

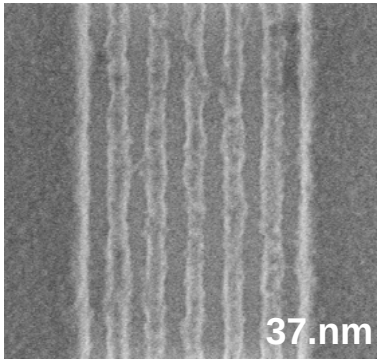
ASML

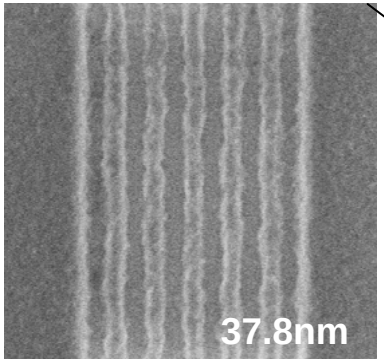
ADT imaging
35nm V and H lines through dose

18.05mJ/cm^2 18.3mJ/cm^2 18.55mJ/cm^2

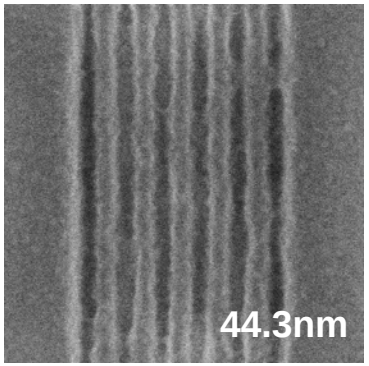
Vertical lines

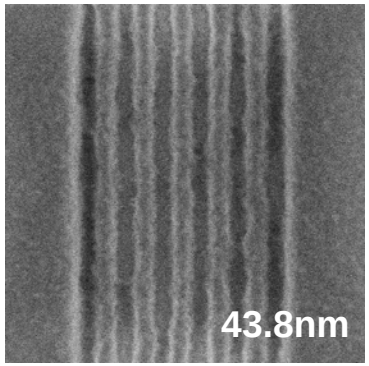


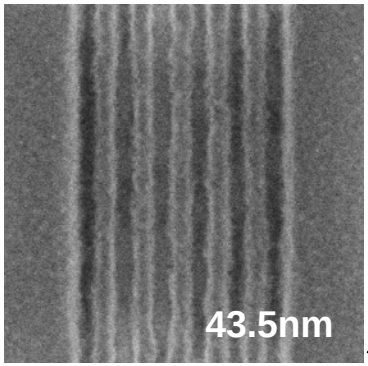


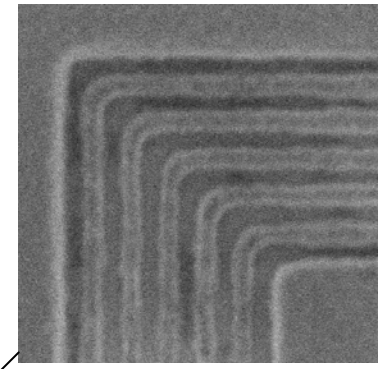


Horizontal lines







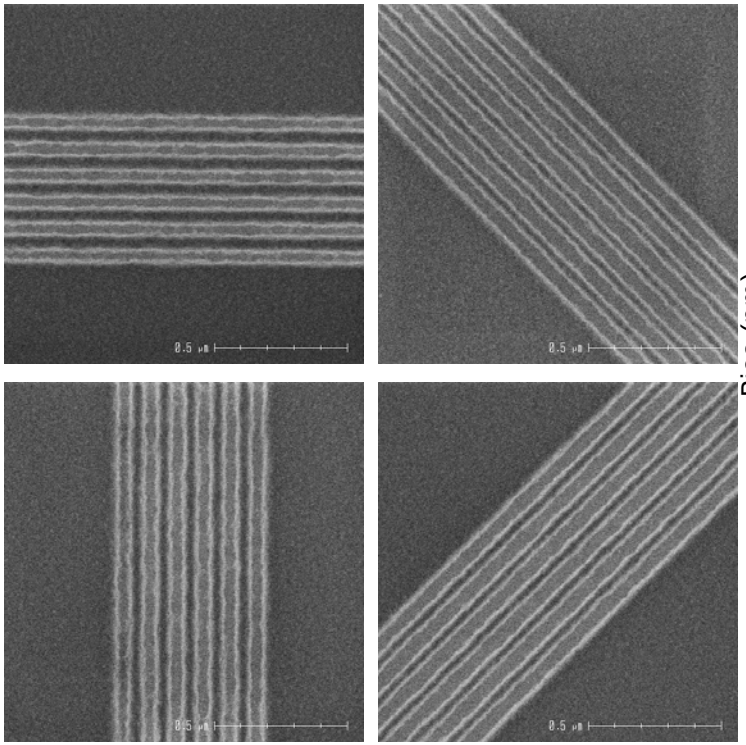


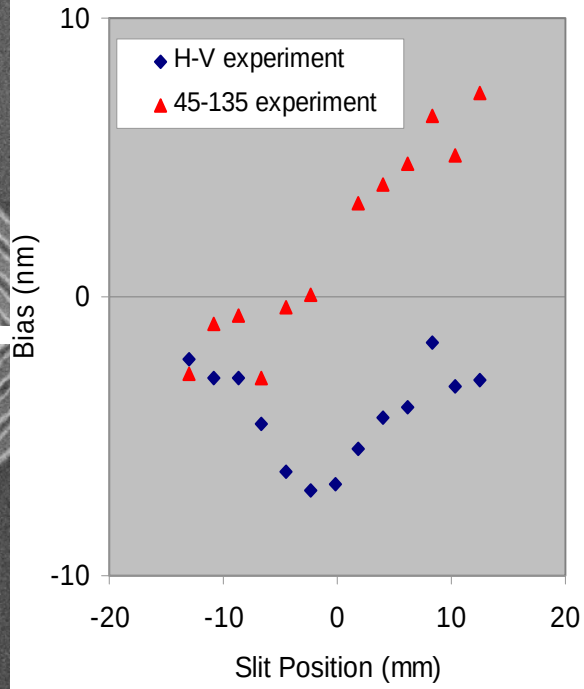
Resist: Rohm Haas MET-2D
Thickness 100nm
NA=0.25, σ=0.5
Lens aberration reduction not finalized yet

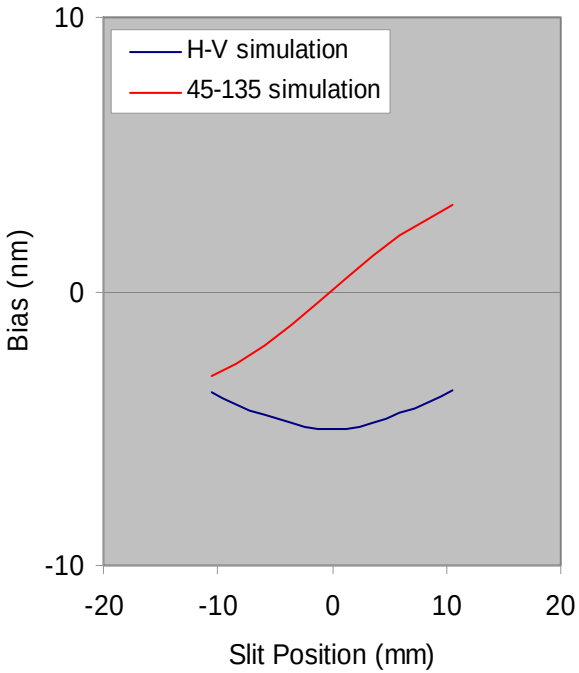
ASML

Shadowing on ASML EUV ADT with Sn Source

Experimental validation







Measurement of 50nm 1:1 L/S at 0^0, 90^0, 45^0, 135^0

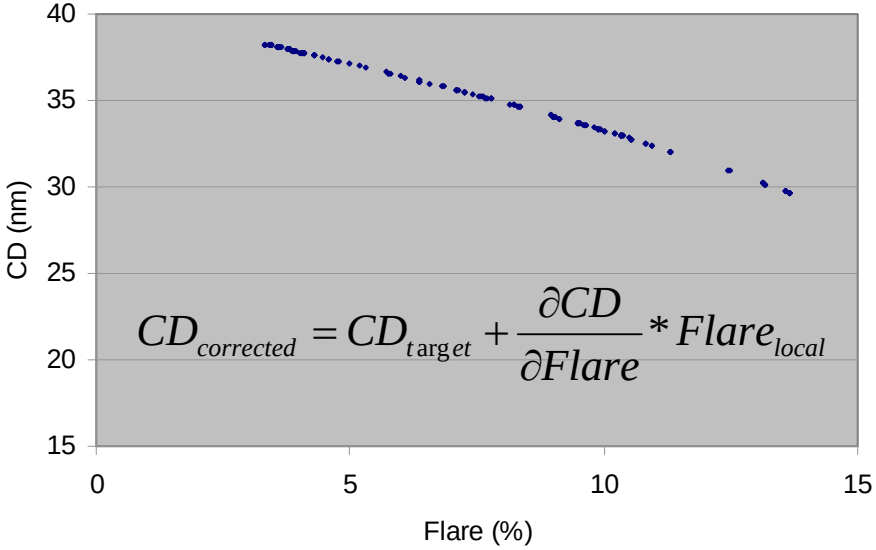
Comparison of simulation and experiment for HV bias and 45^0 -135^0 bias through slit

The experimental measurement of shadowing is in agreement with simulation prediction.

Poster MA-P08 "Shadowing effect compensation", G.F. Lorusso et al

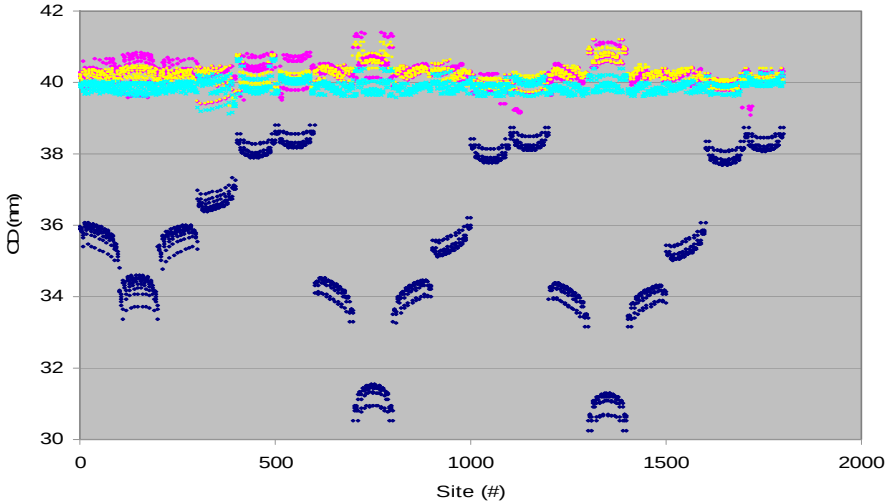
Flare mitigation strategy
Quantifying the quality of rule-based flare correction

Linear dependence of CD on flare



$$CD_{corrected} = CD_{target} + \frac{\partial CD}{\partial Flare} * Flare_{local}$$

CD variation across die

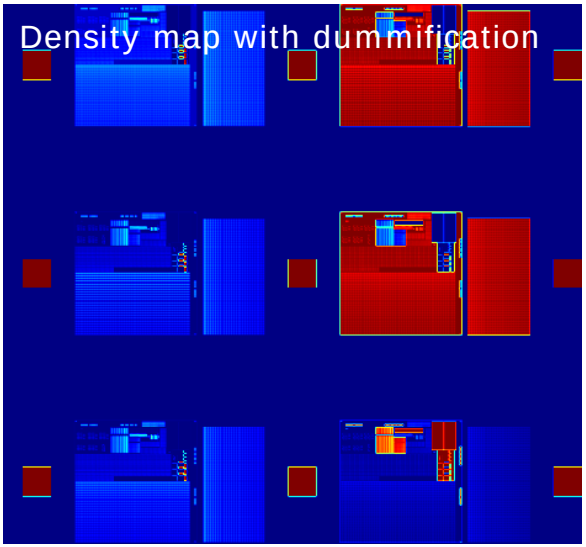


- CD Uncorrected
- CD Flare-corrected - not fractured
- CD Flare-corrected – Fractured
- CD Flare-corrected – Fractured – Iterated on Flare

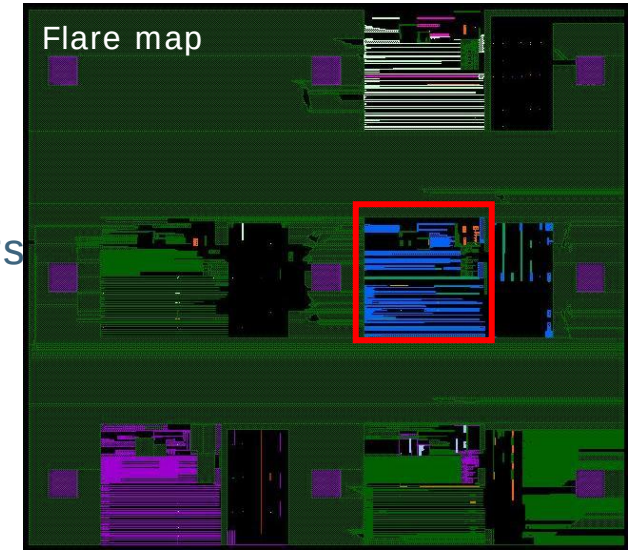
Rule based correction re-sizes the CD at mask level to remove flare artifacts and seems very effective
High-quality Full-Chip Flare map critical to implement rule-based

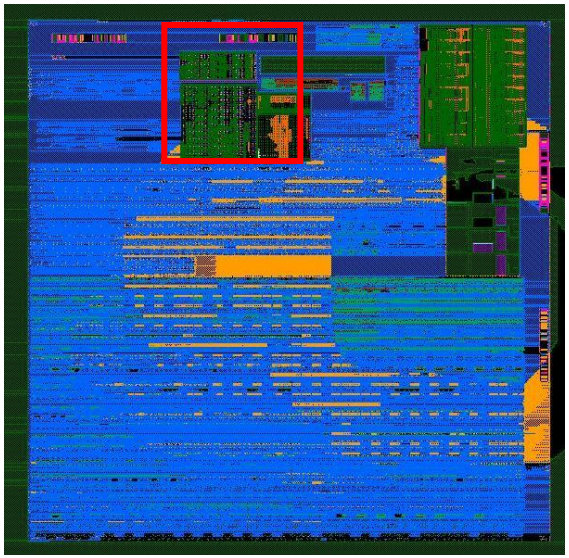
Simulation SOLID-EUV

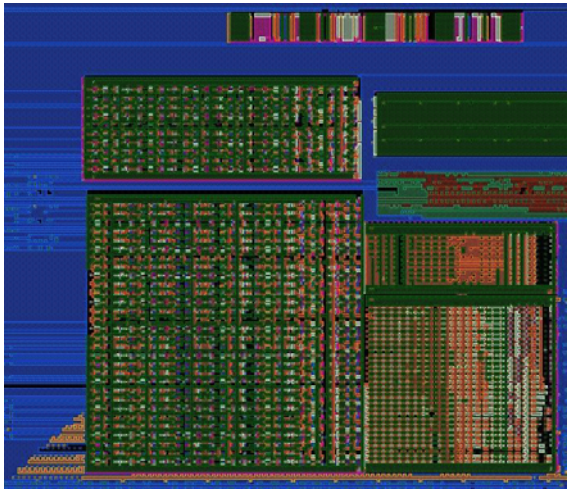
Full Chip Flare Map



68 hrs →



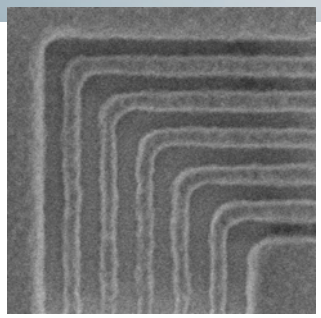




High resolution full chip flare map can be calculated in reasonable time with standard EDA SW.

oral OP-03 "Flare mitigation strategies for EUV", A. Myers

Summary and outlook



- 1st high resolution images demonstrated with ASML ADT equipped with a Sn source
- EUV resists are making steady progress
  - Resolution of 25nm HP demonstrated with interference litho for several materials and sensitivities are reaching the 10mJ/cm^2 target
  - LER is remaining the major challenge
- EUV reticles
  - Extensive simulation study of defect printability and mask reflectivity
  - Experimental phase in preparation with wide mask shop involvement
- Feasible Flare and Shadowing compensation strategies have been developed based on simulation.
- EUV ADT @ IMEC is getting ready for experimental verification

Full field EUV Lithography is becoming reality

Acknowledgements

Many thanks to:

- ASML
  - Noreen Harned, Hans Meiling, John Zimmerman, Bas Hultermans
  - ASML EUV team at IMEC
  - Age Bakker, Leon Romijn, Charles Schaap, Andre Van Dijk
  - Sjoerd Lok, Joop Van Dijck
- Sigma-C (Synopsys)
  - Brian Ward
- IMEC
  - Tom Vandeweyer , Geert Vandenberghe
- PSI
  - Harun Solak, Anja Weber
- Resist and BARC suppliers
- Mask shops
- IMEC IIAP partners

aspire invent achieve

imec

qimonda infineon intel Micron NXP founded by Philips Panasonic ideas for life SAMSUNG ST Texas Instruments tsmc ELPIDA hynix Semiconductor