

The 2007 International EUVL Symposium
Oct. 29th 2007 Sapporo Japan

EUV Lithography Cost of Ownership Considerations

Phil Seidel

Senior Member Technical Staff
Project Manager/EUV Strategy

(512) 356-3732 phil.seidel@SEMATECH.org



Accelerating the next technology revolution.

Advanced Materials Research Center, AMRC, International SEMATECH Manufacturing Initiative, and ISMI are servicemarks of SEMATECH, Inc. SEMATECH, the SEMATECH logo, Advanced Technology Development Facility, ATDF, and the ATDF logo are registered servicemarks of SEMATECH, Inc. All other servicemarks and trademarks are the property of their respective owners.

AGENDA

- CoO overview and Lithography CoO comparisons
- EUV mask CoO analysis w/ 193nm comparisons
- EUV litho patterning CoO analysis w/ 193nm comparisons
- EUV technology requirements vs. potential actual performance: Impacts/opportunity
 - ❑ Blank cost vs. write time impact to EUV mask costs
 - ❑ Exposure throughput vs. Source Power and Resist Speed
 - ❑ Source operation / SoCoMo performance
 - ❑ Overall Reliability
 - ❑ Yield performance
- Summary

SEMATECH's Lithography CoO Exposure Tool Cell Model

$$C_{pwle} = \frac{(C_e + C_l + C_f + C_c + C_r Q_{rw} N_c)}{(T U Y_p)} + \frac{C_m}{N_{wm}} + C_{other}$$

C_{pwle} = cost per wafer level exposure

C_e = yearly cost of exposure, coating, and pattern transfer equipment (including depreciation, maintenance, and installation using 5 yr. depr.)

C_l = yearly cost of labor

C_f = yearly cost of cleanroom space

C_c = cost of other consumables (condenser, laser diodes)

C_r = cost of resist

Q_{rw} = quantity of resist used per wafer

N_c = number of wafers coated

T = throughput = raw throughput

U = tool utilization

Y_p = yield of lithography step

C_m = cost of mask

N_{wm} = number of wafers exposed per mask

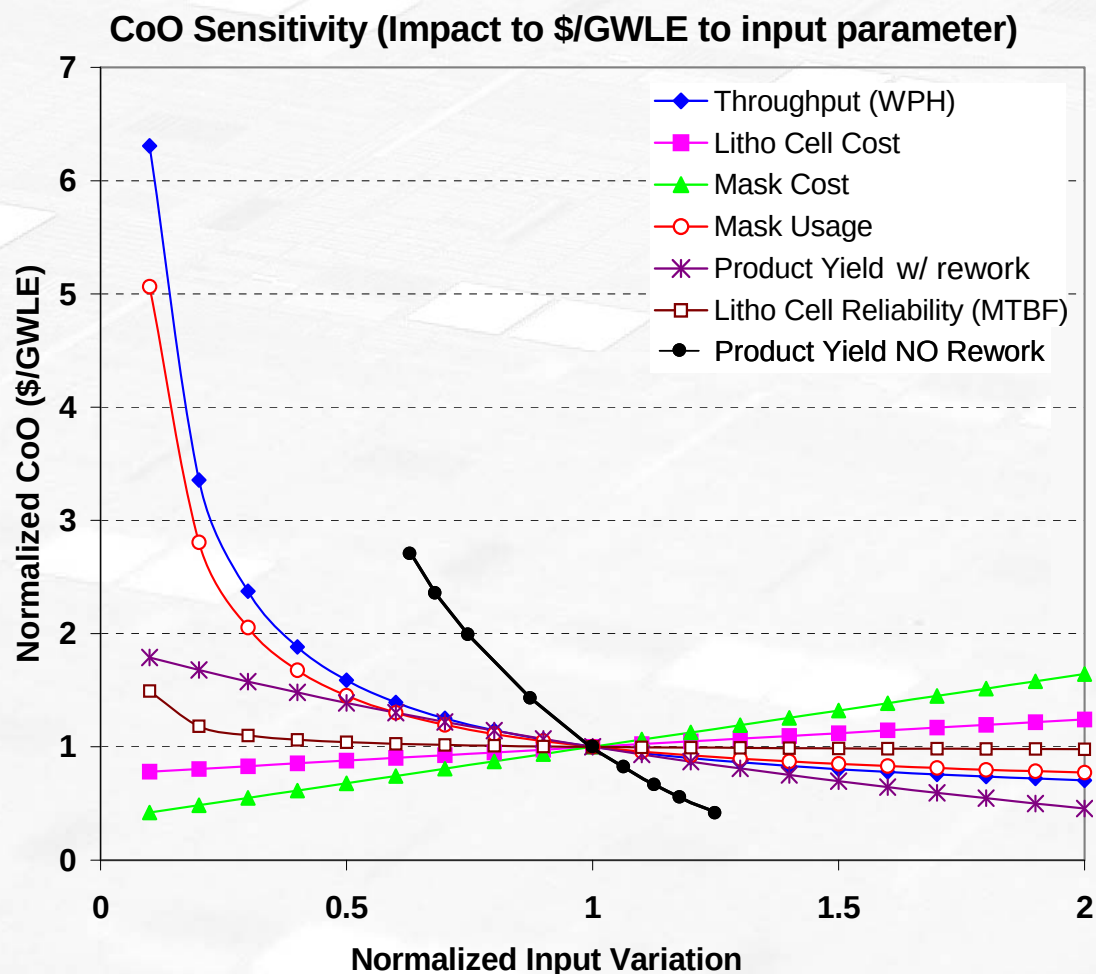
C_{other} = other litho-related costs (etch, cleans, etc.)



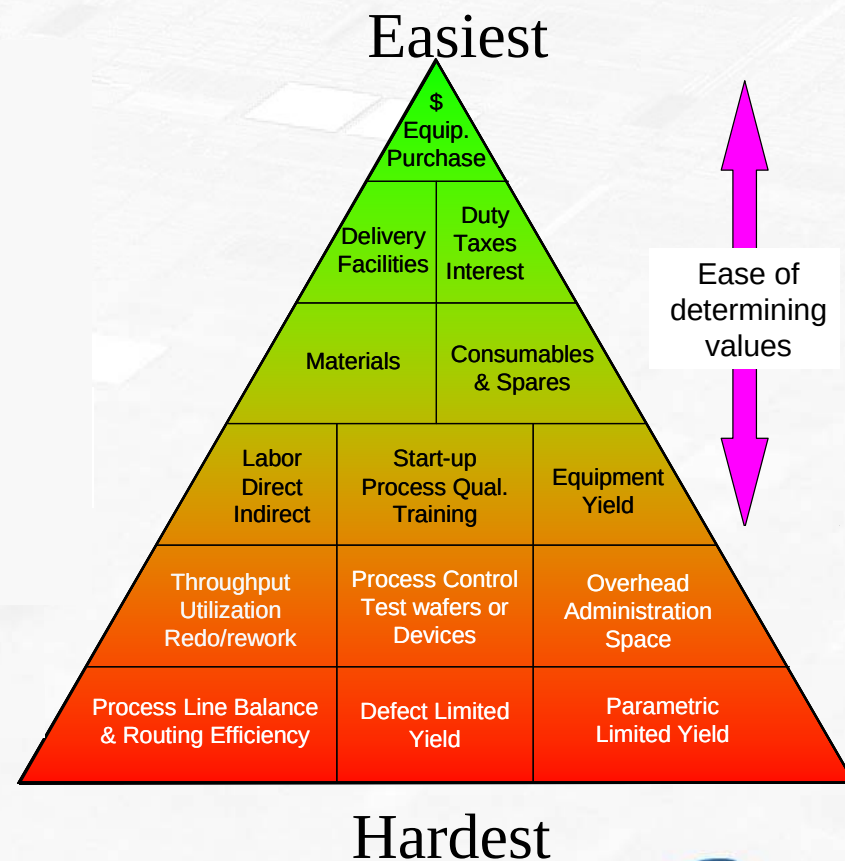
Lithography CoO: Overview

CoO very dependent on key assumptions of input parameter

- Some have significant impacts on CoO outputs (low yield, TPT, mask usage)
- Mfg. operations in fab can influence CoO (e.g., handling of SAHD, yield decisions, etc.)



Graph as referenced in 2005 ITRS Litho chapter

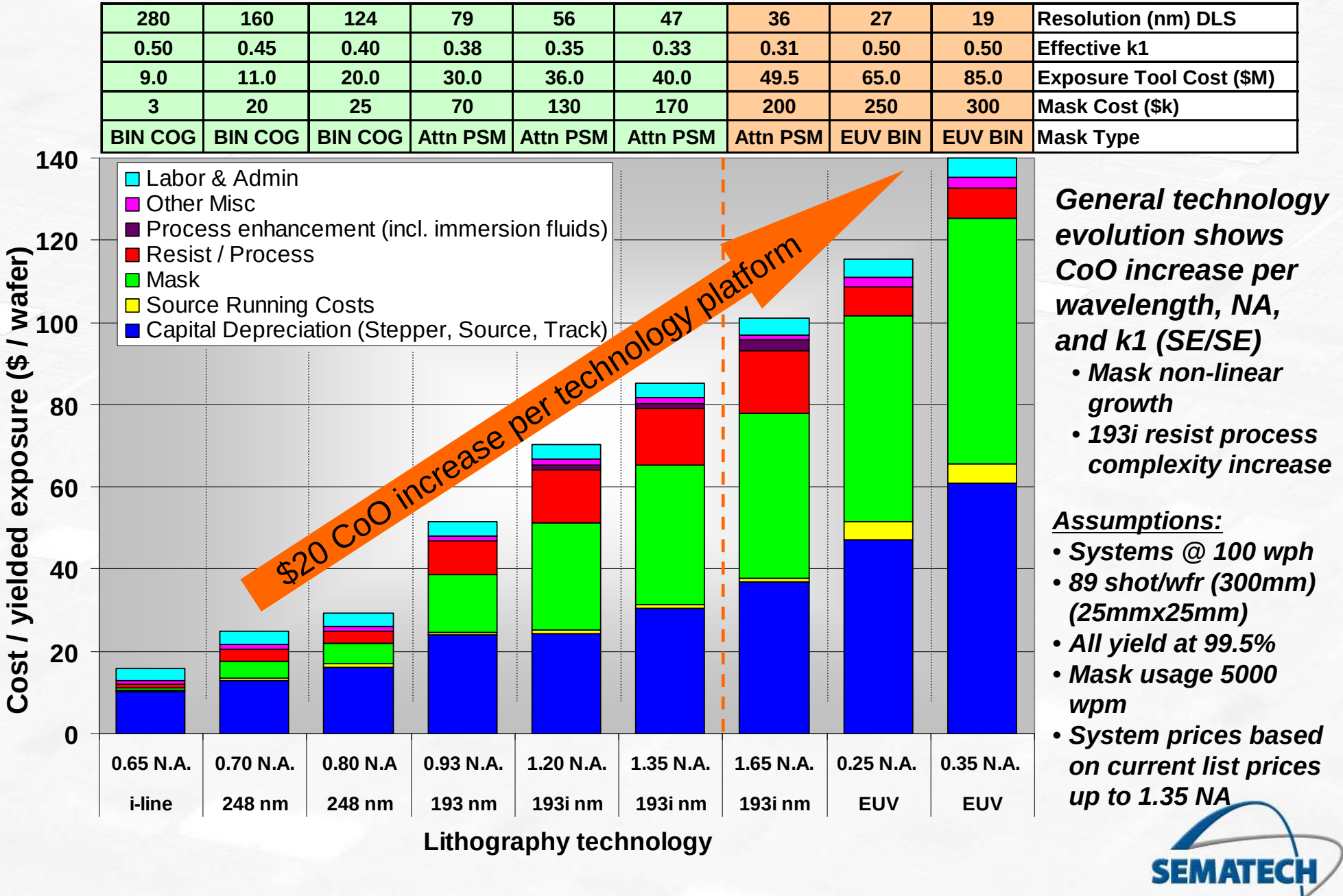


EUV Production Requirements for 32nm HP

- All major subcomponents of the technology have key performance requirements that have significant development programs
- All requirements have either a technology enabling and / or CoO impact
- Cost Effective Source:
 - ❑ Hi power at intermediate focus (> 200 Watts EUV @ IF)
 - ❑ Effective SoCoMo performance (80B pulse lifetime, costs, reliability)
 - ❑ Source maintainability (entry cost, running costs, input power)
- Cost Effective Mask:
 - ❑ High quality defect free EUV blanks (LTEM, 0.003 def/cm² w/ or w/out repair)
 - ❑ Mask patterning yields and costs (mask making toolsets cost vs. performance)
 - ❑ Defect free mask handling requirements (non traditional pellicle)
- Cost Effective Exposure System / Optics:
 - ❑ Efficient vacuum system material handling (mask stages)
 - ❑ P.O. performance at high reflectivity with uniformity (WFE ≤ 0.27 nm rms)
 - ❑ P.O. contamination lifetimes and mitigation
- Cost Effective Resist:
 - ❑ CD and LER performance (≤ 25 nm resolution, ≤ 1.7 nm LER)
 - ❑ Photospeed (≤ 10.0 mJ/cm²)



CoO Comparison for Lithography Technologies at Specific Imaging Resolutions SE/SE (resist, exposure, develop)



SEMATECH Mask CoO Input Assumptions

MODEL NAME: 45nm HP E Attenuated PSM

DATE: 10/5/2007

YOUR NAME: P. Seidel

TECHNOLOGY: 193 dry & 193nm i

SUPPLIER: (n/a)

OTHER INFO:

45nm HP Emb. Attenuated PSM - 193 dry & 193

Process Flow #	Name	1 Equipment Description	2 Equipment Cost	3
0 Customer data				
1 Workstation		HP9000	\$ 50,000	
	Clerical	CATS Software	\$ 100,000	
	Die-Data prep	KLA/Orbot s/w	\$ 110,000	
	OPC Proc	none	\$ 250,000	
1.5 Blank Defect Insp.		Inspection	\$ 4,000,000	
2 Coat/Bake		track elements	\$ 2,000,000	
3 Write		e-beam tool	\$ 30,000,000	
4 Develop		track elements	\$ 1	
5 Dry Etch		Multi etch module sys	\$ 5,250,000	
6 Measure CD		CD SEM	\$ 4,500,000	

MODEL NAME: 32nm - 22nm HP BIN OPC

DATE: 10/5/2007

YOUR NAME: P. Seidel

TECHNOLOGY: EUV mask 32nm HP

SUPPLIER: (n/a)

OTHER INFO:

EUV Mask - mild OPC 45nm HP Logic

Process Flow #	Name	1 Equipment Description	2 Equipment Cost	3 Process Hours	3 Process Yields	9 Consum. Use Cost (\$/mask)	4
0 Customer data							
1 Workstation		HP9000	\$ 55,125	11	100.0%	\$ -	
	Clerical	CATS Software	\$ 110,250	2	100.0%	\$ -	
	Die-Data prep	KLA/Orbot s/w	\$ 121,275	7	100.0%	\$ -	
	OPC Proc	none	\$ 275,625	2	100.0%	\$ -	
1.5 Blank Defect Insp.		Inspection	\$ 4,410,000	1	100.0%	\$ -	
2 Coat/Bake		track elements	\$ 2,205,000	0.17	100.0%	\$ -	
3 Write		e-beam tool	\$ 35,000,000	9.6	100.0%	\$ -	
4 Develop		track elements	\$ 1	0.17	100.0%	\$ -	
5 Dry Etch Absorber only		Multi etch module sys	\$ 5,512,500	0.5	100.0%	\$ -	
6 Measure CD		CD SEM	\$ 5,000,000	0.5	72.1%	\$ -	

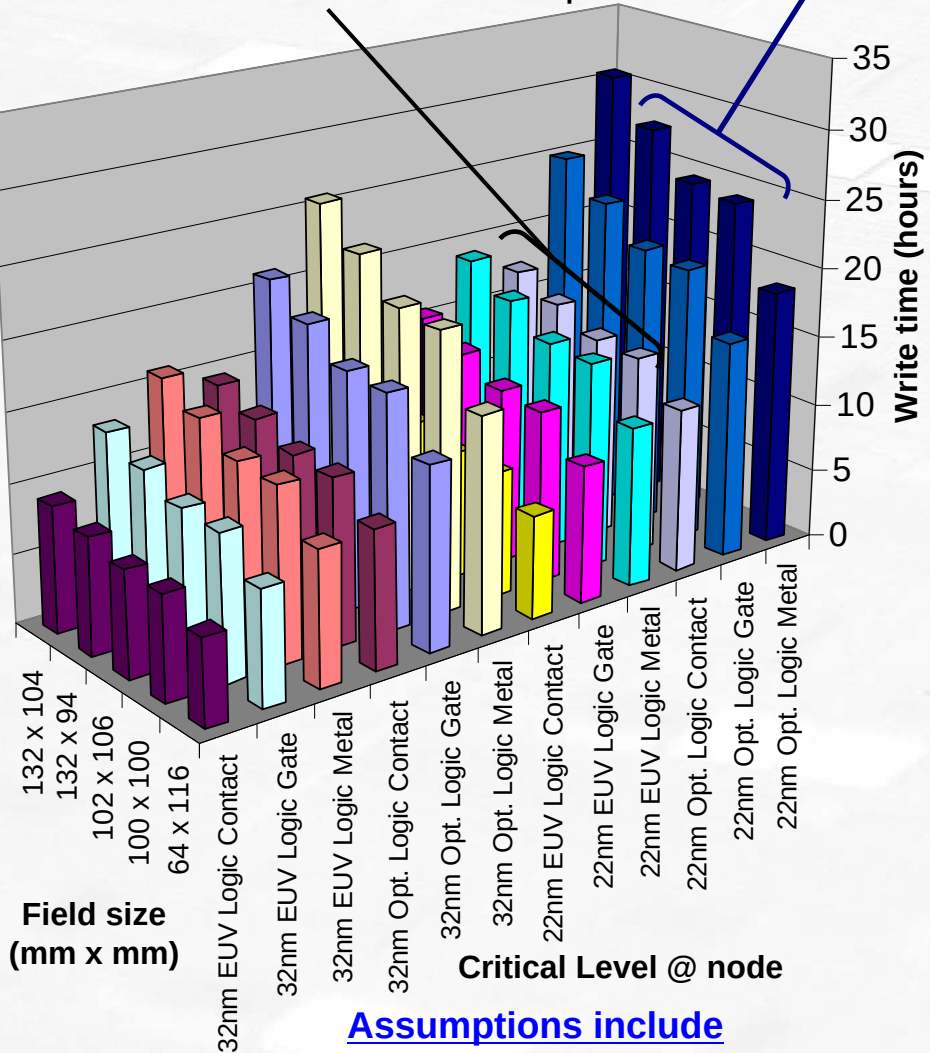
- SEMATECH mask CoO model suites were used with updated assumptions
- Write time calculations were based on e-beam writer “shot count” growth models using 90nm HP baseline (looked at 2.0X and 2.5X growths per node)
- Adjustments to mask shot count requirements are applied based on the feature density for device levels and general k1 requirements.
- EUV shot count assumption 30%–35% less than optical OPC at same node
- First-year mask yields were assumed in the mask CoO models based on previous public presentations (Scott Hector et al., EMLC '06)
- Mask process tooling and mask material assumptions included price increase trend to meet new node requirements at same yield/performances
 - Higher price growth rate included e-beam PG, pattern insp, overlay [~0.2X/node]
 - Moderate growth rates for laser writer, CD, pattern review/repair [~0.1X/node]
 - Other process tools and data fracture cost growth ~5%/node



Mask Write Time and Costs (+ margin) at 32nm - 22nm HP

Writer time estimation using a 2.0X shot count growth from 90 nm HP baseline

- >25 hr for some optical 22 nm HP critical levels.
- >15 hr for some EUV 22nm HP as a result of reduced OPC features vs. optical masks

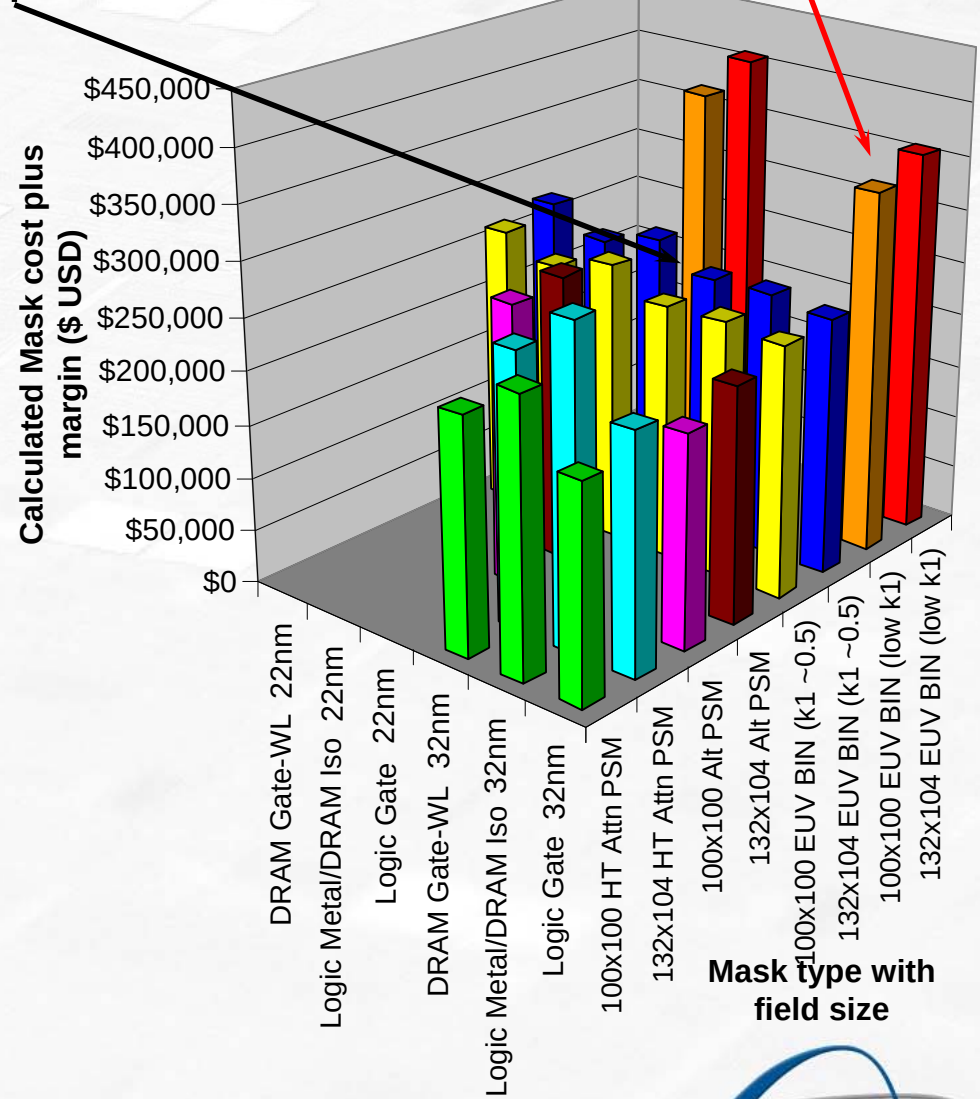


Assumptions include

- New PGs timely introduction to 22nm HP
- Shot count growth increase 2.0X per node
- EUV mask shot count 30-35% less than optical

SEMATECH calculated 32nm and 22nm HP masks using models and assumption

- > k_1 0.50 EUV mask for 32nm HP ~ \$240k
- > A low k_1 EUV mask shot count drives ~ \$350k



Device levels at ITRS technology



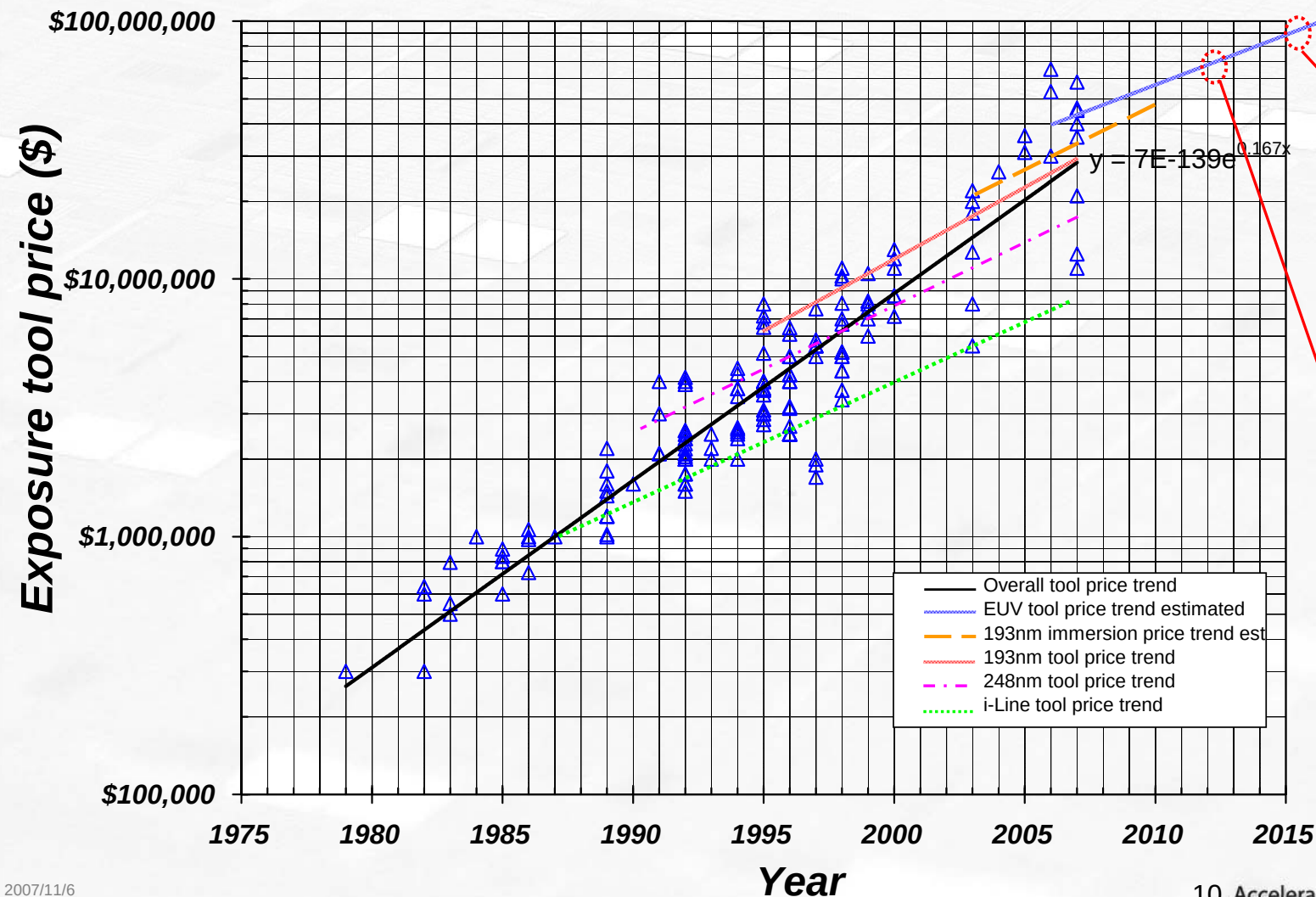
EUV Exposure Tool CoO Assumptions

- SEMATECH exposure tool CoO model suites were used
- Rigorous estimated parameter developments provided assumption set for the input of the CoO parameters for 193 nm dry, 193i, and EUV.
 - Internal SEMATECH project data, expert interviews, public data
- CoO input assumptions generally were scaled based on technology requirements based on trend and internal SEMATECH assessments.
- Exposure tool cells include scanner body, source system, and resist process track. Tracks scaled to meet stepper throughput with ~20% over capacity.
- EUV exposure scanner prices determined using historical price trends with additional evaluations on “technology” jumps (248 nm → 193 nm dry → 193i)
- EUV source powers incrementally increased per technology.
- Photoresist process costs assumed at today’s 65 nm HP baseline and price/performances scaled to assume 45 nm through 22 nm HP needs.
 - EUV resists assumed a SLR process with performance and price increases vs. 193i SLR @ 2 cc/wafer usage
 - EUV developer costs assumed a SLR resist platform aqueous based developer @ same developer consumption rates as 193nm dry
- Total patterning costs include the lithography exposure cell CoO PLUS the “pre” and “post” patterning step costs (i.e., hardmasks, metrology, etching, ashing, etc.)



Exposure Tool Price Assumptions

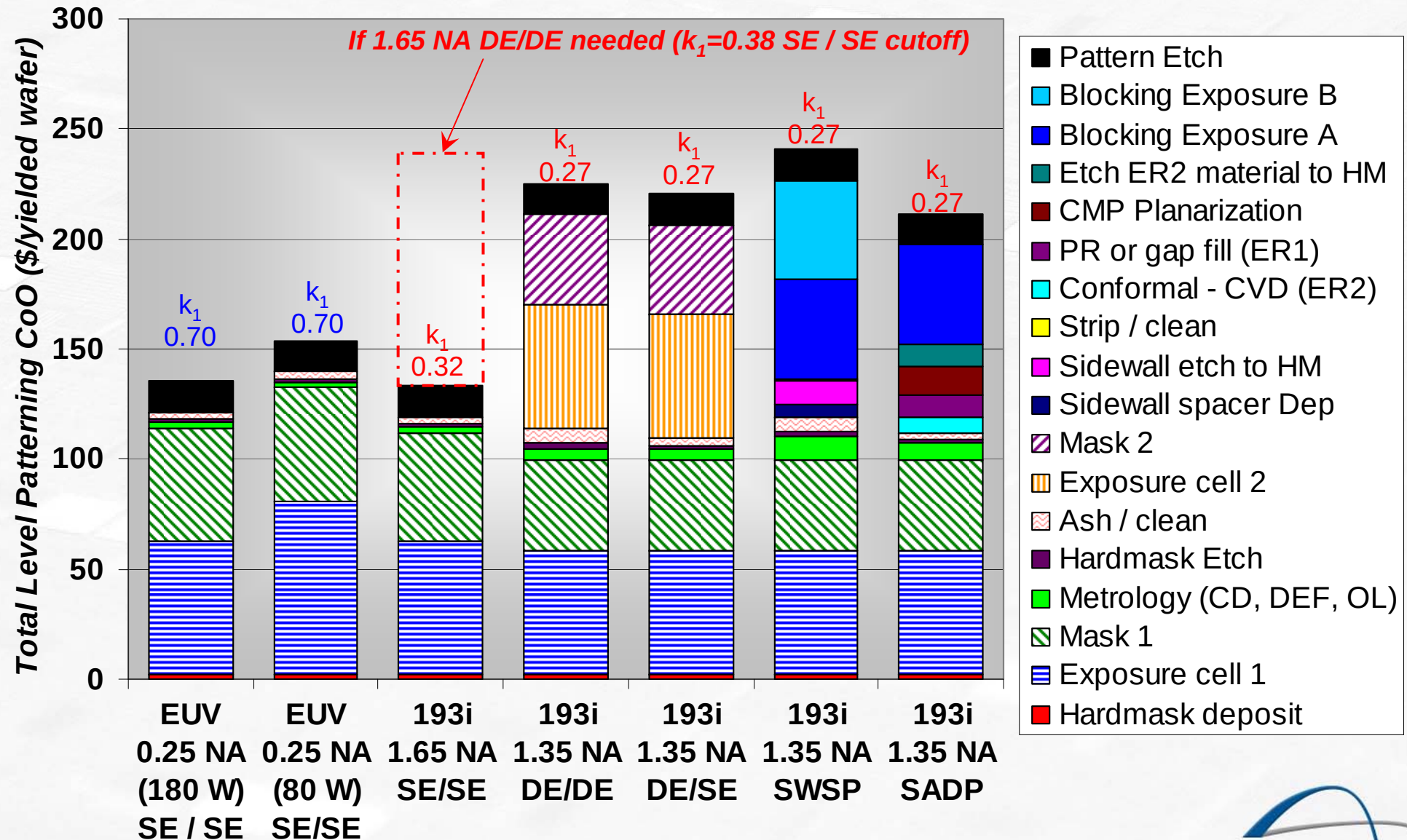
- Production EUV tools prices were estimated based on 193 nm technology growth and with technology jump vs. 193 nm dry.
- The exposure tool price growths are attributed to many factors including exposure wavelengths, numerical apertures, wafer size vs. stage speed improvements, and many other system productivity improvements (e.g. illumination, in situ sensors, etc.)



- 0.35 NA EUV tool estimated \$85M (added projection optics and source power)
- 32 nm HP 0.25 NA EUV tool estimated \$65M (body + source)

Lithography Patterning Solutions for Logic CoO Anal.

Total CoO Comparison for 32nm HP Logic Metal 1 Level for Various Patterning Strategies (all at 99.0% level yield)



Assumptions include 5,000 wafers per mask, 38nm 1:1 DLS resist image for M1



EUV CoO Uncertainty and Potential Opportunities

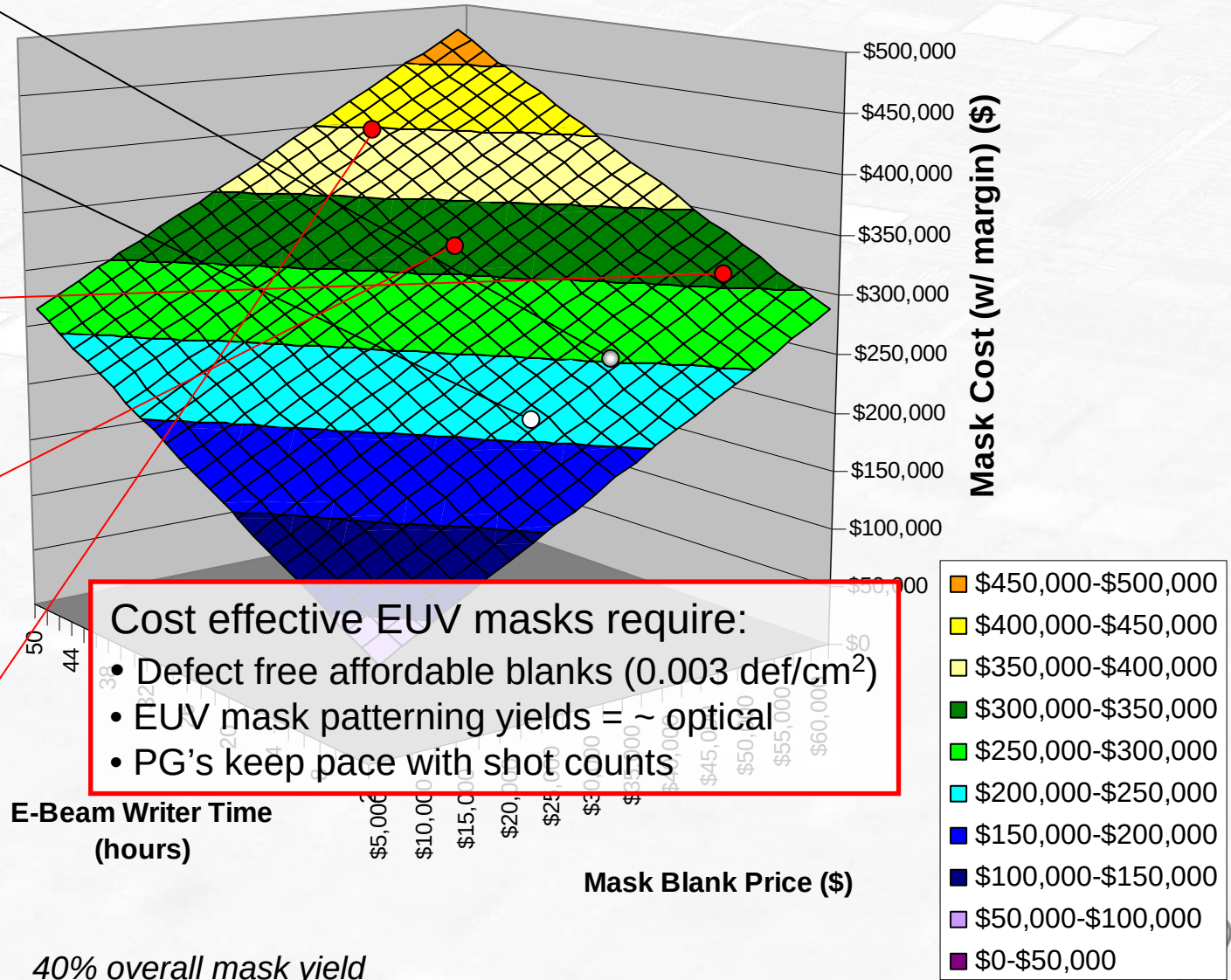
- The EUV CoO assessments presented thus far assume that all EUV performances are attained to development requirements:
 - > 180 Watts IF source power, EUV P.O. mirror reflectivity 67%, 0.25 NA 6 mirrors
 - Imaging k_1 0.50 – 0.60
 - EUV blank defect yield > 60%, EUV mask feature OPC requirements vs. optical
 - Resist photospeed 10 mJ/cm²
 - Exposure tool cell costs conforming to historical trends
 - Many other requirements
- However.... **“WHAT IF”** the major technology requirements do not meet the expected/intended goals
- CoO impacts with
 - Mask blank yield vs. cost, write time, and shot count/mask CoO severity
 - EUV source power vs. resist photospeed
 - EUV source operation, maintainability, and SoCoMo reliability
 - EUV exposure cell availability/operation
 - Increased defectivity/yield hits



EUV Costs Impact Assessment/ Mask Blank vs. Write Time

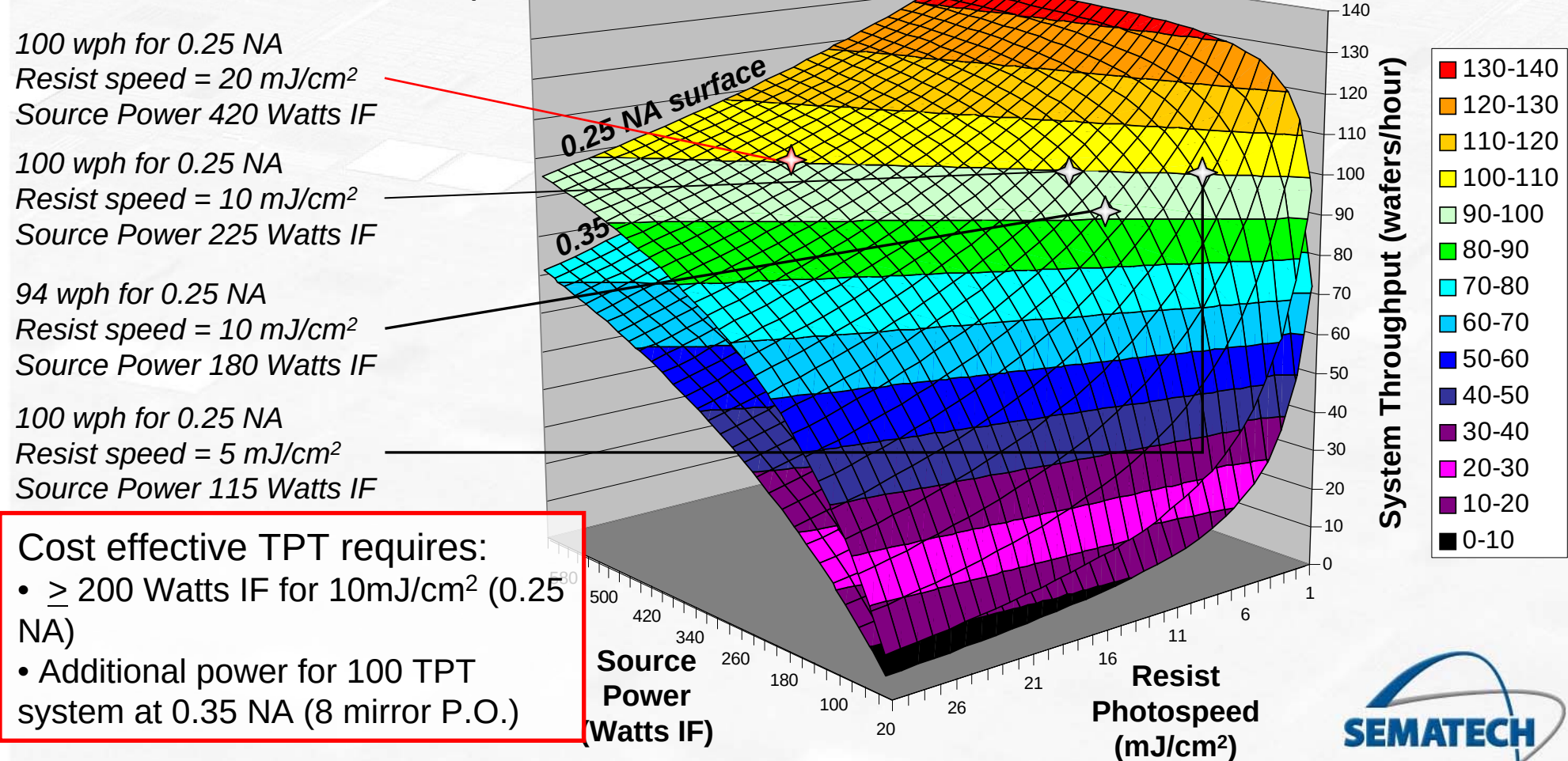
- Assessment to investigate the impact of low blank yield/performance vs. write time if shot count growth mode or sub-0.50 k1 (low k1) masks are needed: A 2.5X growth rate and low k1 mask could drive a \$400k EUV mask
- CoO baseline of 10 hr write, \$40k blank drives a \$250k mask
- EUV blank cost target of \$30k can reduce mask to near \$200k
- If blank defect yield cannot be improved or other mitigation is affected, a \$60k blank drives mask to > \$300k
- If shot count growth rate is at 2.5X vs. 2.0X, then a 30 hrs write drives a \$325k mask
- If a high fidelity EUV mask is needed to image critical logic gate application ($k_1 < 0.4$) and growth rate is 2.5X, then mask write times increase to 40 hrs and results in a \$400k mask

A \$400k mask at 5000 wpm = \$80 CoO adder



EUV System Power Requirements for 100 wph

- 0.35 NA EUV exposure tool requires an 8-mirror P.O. design vs. the 0.25 NA system having 6 mirrors (0.25 NA 100 wph system requires 225 Watts IF; 89 fields, 10 mJ/cm²).
- 0.35 NA will require higher source power to maintain high wafer throughputs
 - 0.25 NA systems have an effective total EUV transmission of 8.1% at the wafer level
 - 0.35 NA systems have an effective total EUV transmission of 3.7 % at the wafer level
- EUV exposure tool for 0.35 NA and capable source (100 wph) assumes a \$85M system vs. 0.25 NA \$65M assumption.



EUV Source CoO Analysis Running Cost Impacts

Percentage of Overall Exposure Level CoO From Source CoO

		Source Condensor Optics Costs (\$M)					
		0.4	0.8	1.2	1.6	2	2.4
Optics Lifetime (B pulses)	2	28.7%	41.5%	50.3%	56.9%	61.9%	65.9%
	6	16.9%	23.7%	29.4%	34.4%	38.7%	42.4%
	10	13.9%	18.4%	22.5%	26.2%	29.6%	32.6%
	20	11.5%	13.9%	16.3%	18.5%	20.6%	22.6%
	40	10.2%	11.5%	12.7%	13.9%	15.1%	16.3%
	60	9.7%	10.6%	11.5%	12.3%	13.1%	13.9%
	80	9.5%	10.2%	10.8%	11.5%	12.1%	12.7%

Collector costs and lifetimes are major issues when below 20 B pulses

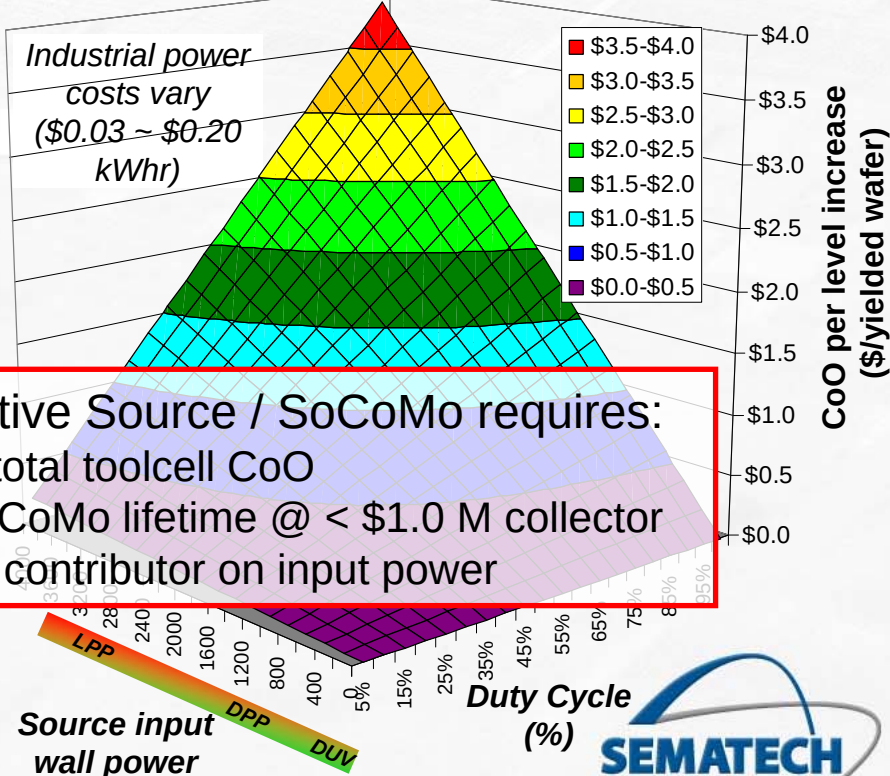
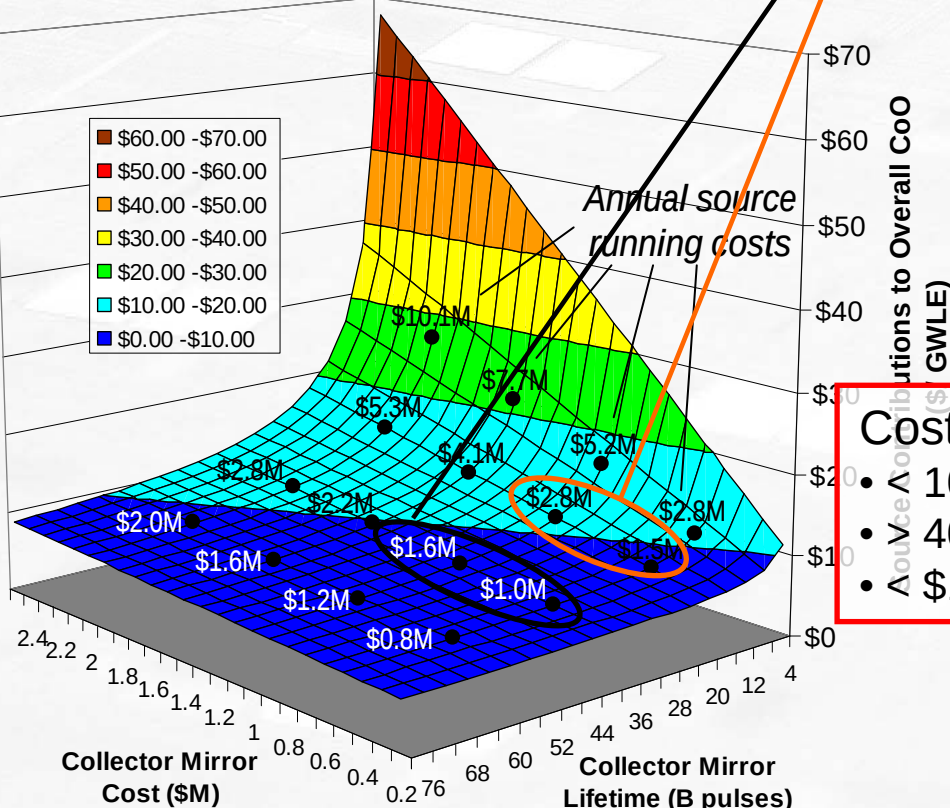
- Most dominant overall impact to EUV exposure cell CoO below 20 B
- Annual running costs \$1.5M - \$5M/yr at or below 20 B pulse and is a \$6/wafer adder alone
- 40 B pulse lifetime drives a \$3/wafer adder alone

Wall plug electrical power can have significant CoO impacts (Megawatt hours ?)

EUV source electrical power effects to CoO

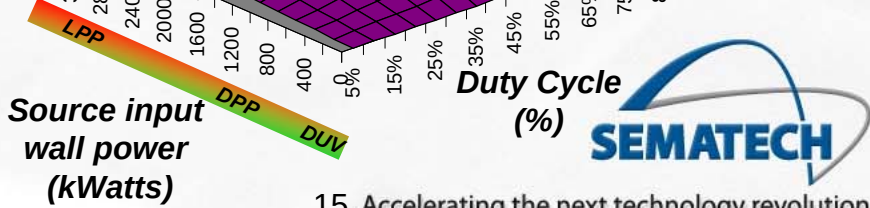
~\$1 CoO adder per 1 Megawatt x hour (\$0.05 kWhr)

EUV source CoO contributions to overall CoO



Cost effective Source / SoCoMo requires:

- < 10% of total toolcell CoO
- > 40 B SoCoMo lifetime @ < \$1.0 M collector
- < \$1 CoO contributor on input power

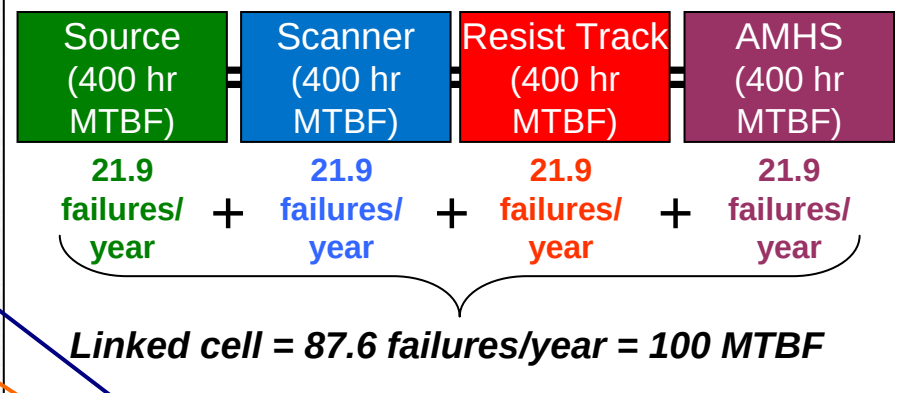


EUV Source vs. Exposure Tool Cell Reliability CoO Impacts

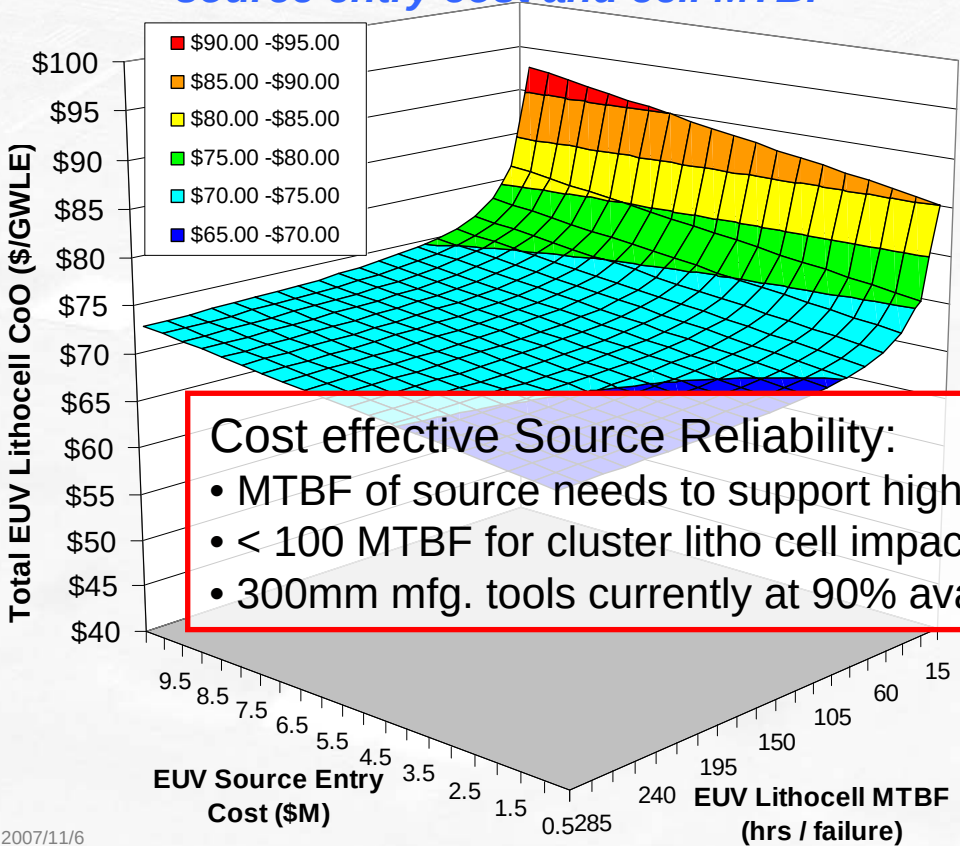
Source MTBF reliability will impact the exposure tool cell CoO and availability

- Linked cell MTBF is inverse sum of all subsystems (track, exp., source, etc.)
- Significant CoO impact when system MTBF below 100 hrs (> 400 hrs MTBF for each sub)
- \$5M high reliability source accounts for \$8.50 CoO per level; (\$10M source = \$11.20 CoO per level)

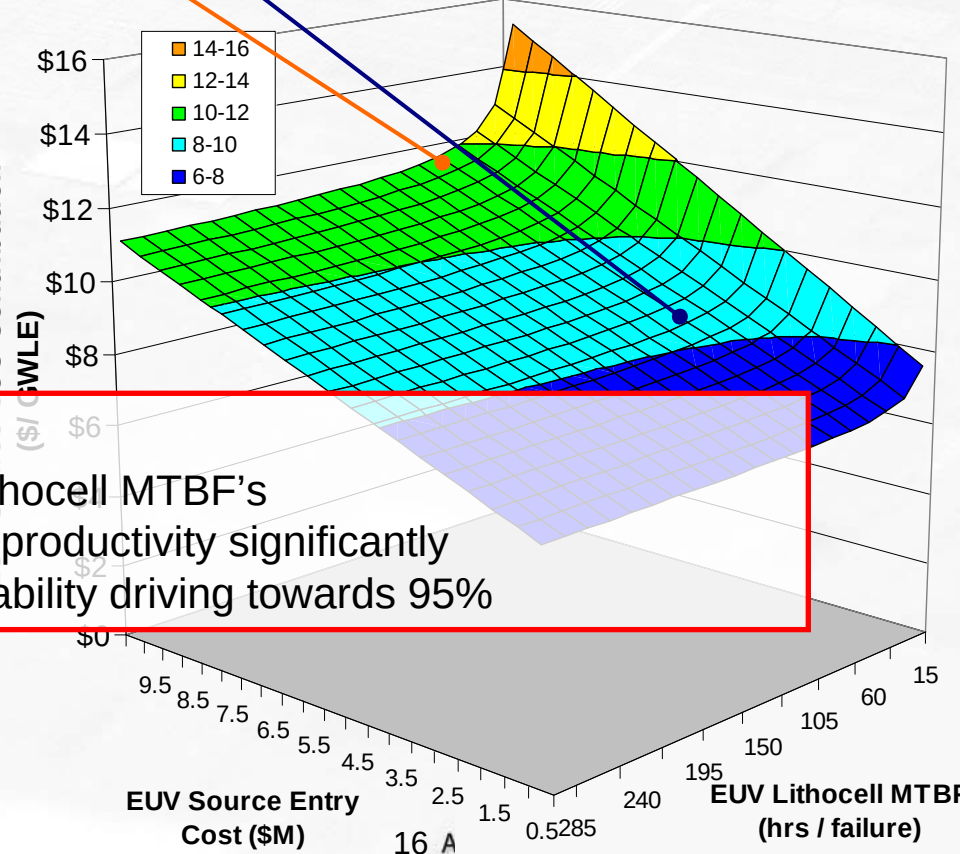
Linked exposure cell reliability acts as series



Total EUV exposure cell CoO as function of source entry cost and cell MTBF



EUV source CoO contributions to overall CoO



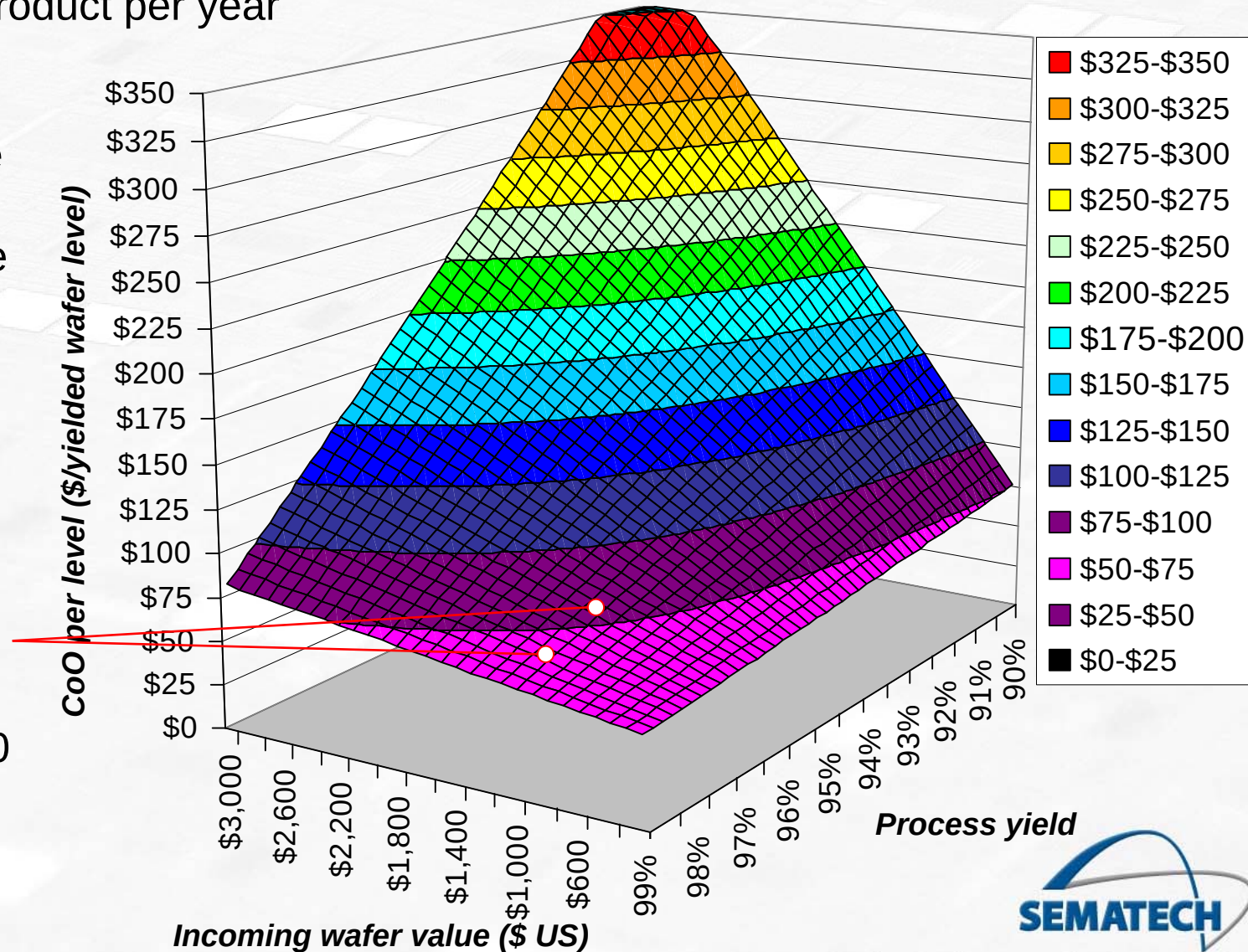
Process Yields and Wafer Value Impacts

Wafer yield impacts can be the largest impact to CoO

- Added wafer values are attained as wafer is processed through manufacturing flow
- A 0.1% yield decrease can cause \$1.00 change in wafer-level CoO and up to \$4 M lost product per year

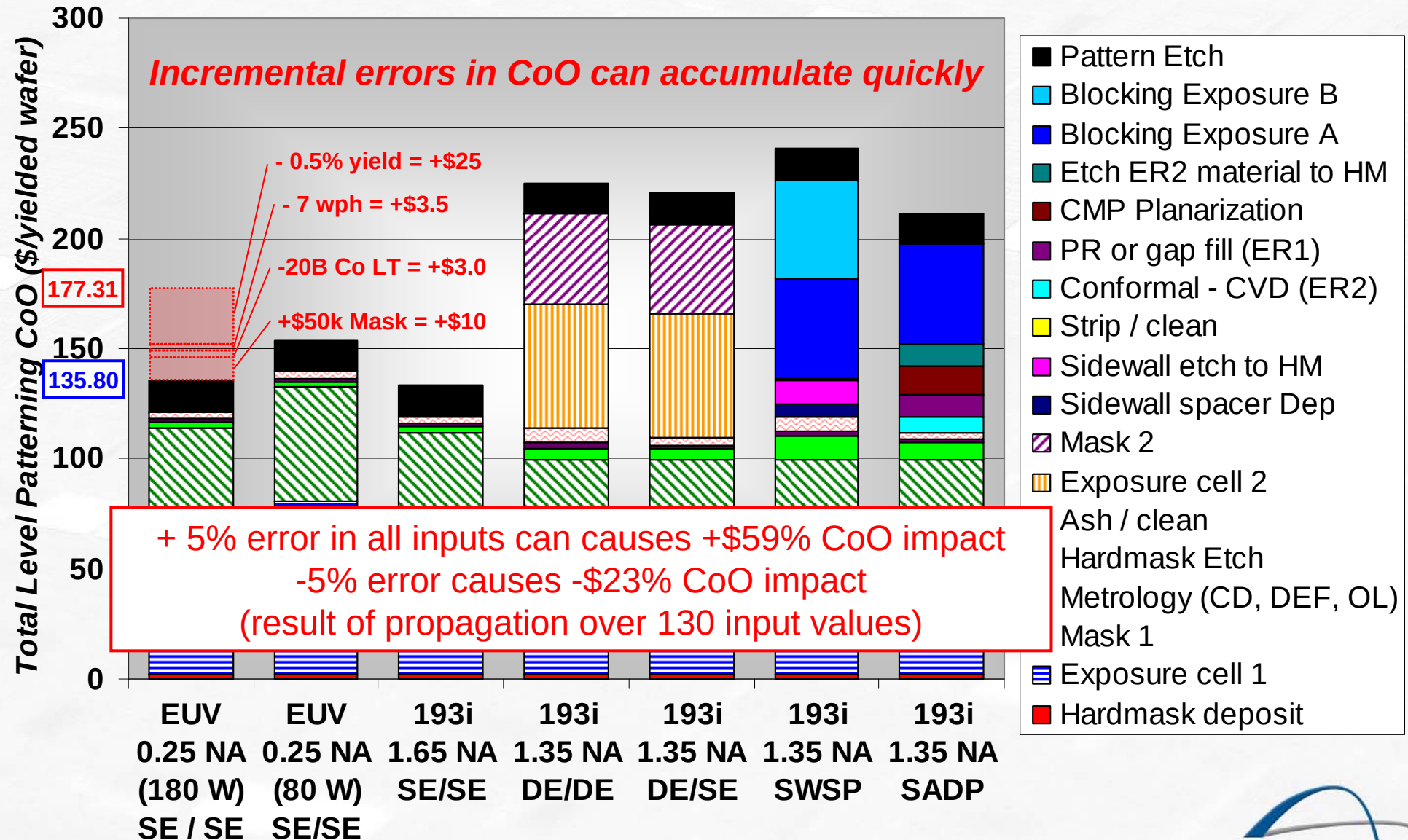
- Dramatic yield impacts reinforce the need for defect-free reticle handling.

- 1.0% yield impact on one level can cause a \$10.00 CoO increase and ~\$40M lost product annually (assuming \$1000 wafer value and 99% vs. 98% yield)



Lithography Patterning Solutions for Logic CoO Anal..

Total CoO Comparison for 32nm HP Logic Metal 1 Level for Various Patterning Strategies (all at 99.0% level yield)



Assumptions include 5,000 wafers per mask, 38nm 1:1 DLS resist image

Summary

- EUV CoO levels are going to be higher than the previous technologies based on the preferred SE / SE case.
 - EUV CoO increase follows a \$20/wfr increase per technology platform
 - EUV toolcell CoO for 32nm HP estimated \$115 (using 5000 wafer per mask)
- The EUV CoO levels for SE/SE appears competitive including “pre” and “post” litho steps given all major EUV technology requirements are met
 - EUV not significantly more than 193i 1.65 N.A. SE / SE at 32nm HP
 - Significantly less expensive than 1.35 N.A. or 1.65 N.A. DP by 35%-40%
- Very important that 0.25 NA EUV systems meet required development goals to maintain cost-effective advantage DE/DE.
 - Numerous minor compounded effects can quickly increase EUV CoO levels
 - EUV mask performance and cost are driven by both EUV blank cost as well as shot count and write time requirements (cost effective high blank yields)
 - Adequate system TPT while maintaining printing yield requires at least 10 mJ/cm² resist and 180 - 200 Watt IF source
 - Source and SoCoMo performance and running costs require CoO contribution of 15% or less (< \$10M source, > 40 B pulse SoCoMo LT, < \$1M SoCoMo)
 - Essentially no yield impact due to EUV mask printing and handling



Thank You....

Acknowledgements:

Scott Hector – Freescale

Victor Pol – Freescale

Will Conley - Freescale

Mark Mason – TI

Shane Palmer – TI → PAL

Scott MacKay – Photronics → PAL

Robert Wright – ISMI

Doug Guenther – ATDF

James Beach – ATDF

Lloyd Litt – AMD/SEMATECH

Greg Hughes – SEMATECH

Shyam Palaiyanur – SEMATECH
(Nano-Scholar)

Jeff Byers – SEMATECH

Vivek Bakshi – SEMATECH

Michael Lercel – IBM

Stefan Wurm – Qimonda / SEMATECH

Pat Gabella – SEMATECH

John Peterson – PAL

The SEMATECH CoO historical contributors:

G. Escher

G. Shelden

E. Muzio

W. Trybula

S. MacKay

Birol Kuyel

Keith Standiford

John Canning

Martin McCallum

and many others

