EUV Mask Pilot Line at Intel Corporation

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Outline

- Introduction: EUV Challenge
- Pilot Line Concept
- Project Execution
- Mask Fabrication
- Summary

EUV-Specific Challenges Require New Capabilities

- Defects
  - How to find them — Substrate, Blank and Pattern Inspection
  - How to fix them — Electron-beam Mask Repair
  - How to eliminate them — Defect Review and Analysis
- 50nm mask flatness — Flatness Metrology
- Actinic metrology — EUV AIM
- *Must avoid multilayer damage*

Pilot Line Concept

- Objectives:
  - Masks for EUV lithography development
    - 0.3 NA EUV Micro Exposure Tool (MET) now
    - 0.25 NA full-field beta tool in 2006
  - EUV mask process development.
    - All process steps, incl. integrated back end.
    - Defect reduction
  - Enable the supplier infrastructure.
    - Tools for today and for production.
    - Reticle Handling
- Strategy:
  - Use standard tool set as much as possible
  - Develop EUV-specific tools and materials and their infrastructure where needed.

EUV Mask Development Schedule

Start with Roadmap Goals

90nm	65nm	45nm	32nm

32nm Si Dev.

Mask Pilot Line

EUVL Demon-stration

Process Development
Mask Fabrication

Infrastructure Development *Two Tool Strategy*

Beta Tools

Production Tools

How do we do it?

Specifi-cations

Beta Tool Purchases

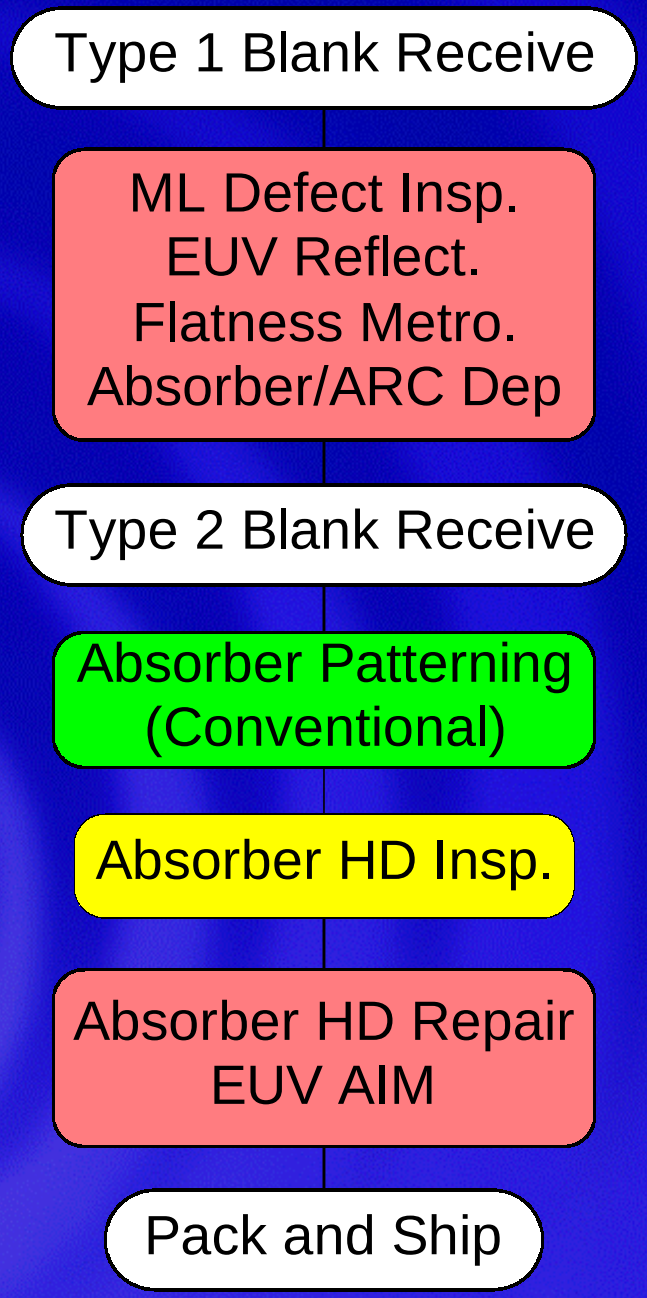
Development Agreements

Consortia Partnering for PT NRE

Production Tool Purchases

Pilot Line Flow

- Includes part of blank fabrication and back end
- Accomodates Type 1 and Type 2 blanks
  - Type 1 = w/o absorber
  - Type 2 = with absorber
- Conventional patterning
- Industry-standard HD inspection tool
- New HD repair and AIM



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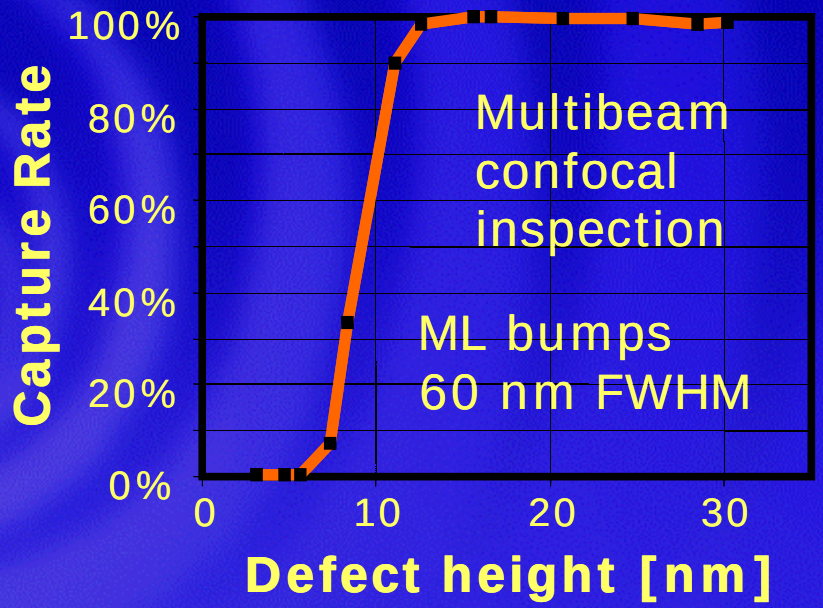
Pilot Line Implements EUV Defect Inspection Strategy

- Multilayer defects: find and develop an appropriate inspection tool
  - Confocal inspection (2002 BACUS)
- Pattern Defects: Make industry-standard pattern inspection tools work for EUV masks.
  - High contrast under reflected light.
  - Reflected light database rendering

Mask Blank Inspection

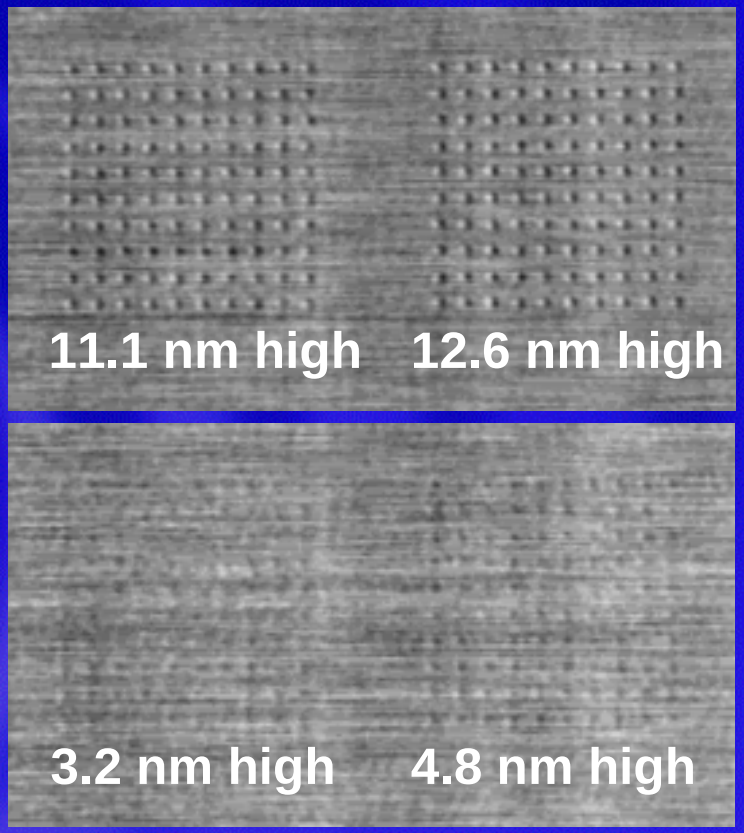
- 488nm multibeam confocal inspection
- Determines blank and substrate quality
- Applications:
  - Substrate defect inspection (at supplier)
  - Multilayer defect inspection
  - Absorber inspection
- Capabilty
  - 60nm (PSL equiv.) sensitivity
  - Some improvement possible



Blank Inspection Tool Development

- Very small defects are visible in review images
  - Inspection is false defect limited
  - Opportunity for improvement.
- Rigorous simulations predict production tool sensitivity
  - Predicts dependence on λ, size, film index and defect index
- Tool being deployed in industry
  - Industry-wide benefit
- Production tool development underway
  - Shorter wavelength
  - ISMT funding

Review images of ML bump defect arrays 60nm FWHM



60nm PSL ~ 11 nm high

Pattern Inspection

- Mask DUV reflectivity optimized for pattern inspection
  - Absorber ARC tuned to 257nm
  - High contrast similar to CoG transmitted light images
- Use "industry standard" DUV pattern inspection tool
  - Use pre-existing infrastructure
  - Sensitivity as good as CoG
  - Reflected light database rendering under development.
- Development aided by NIST ATP Project on NGL Mask Inspection

Reflected Light DUV Review Images

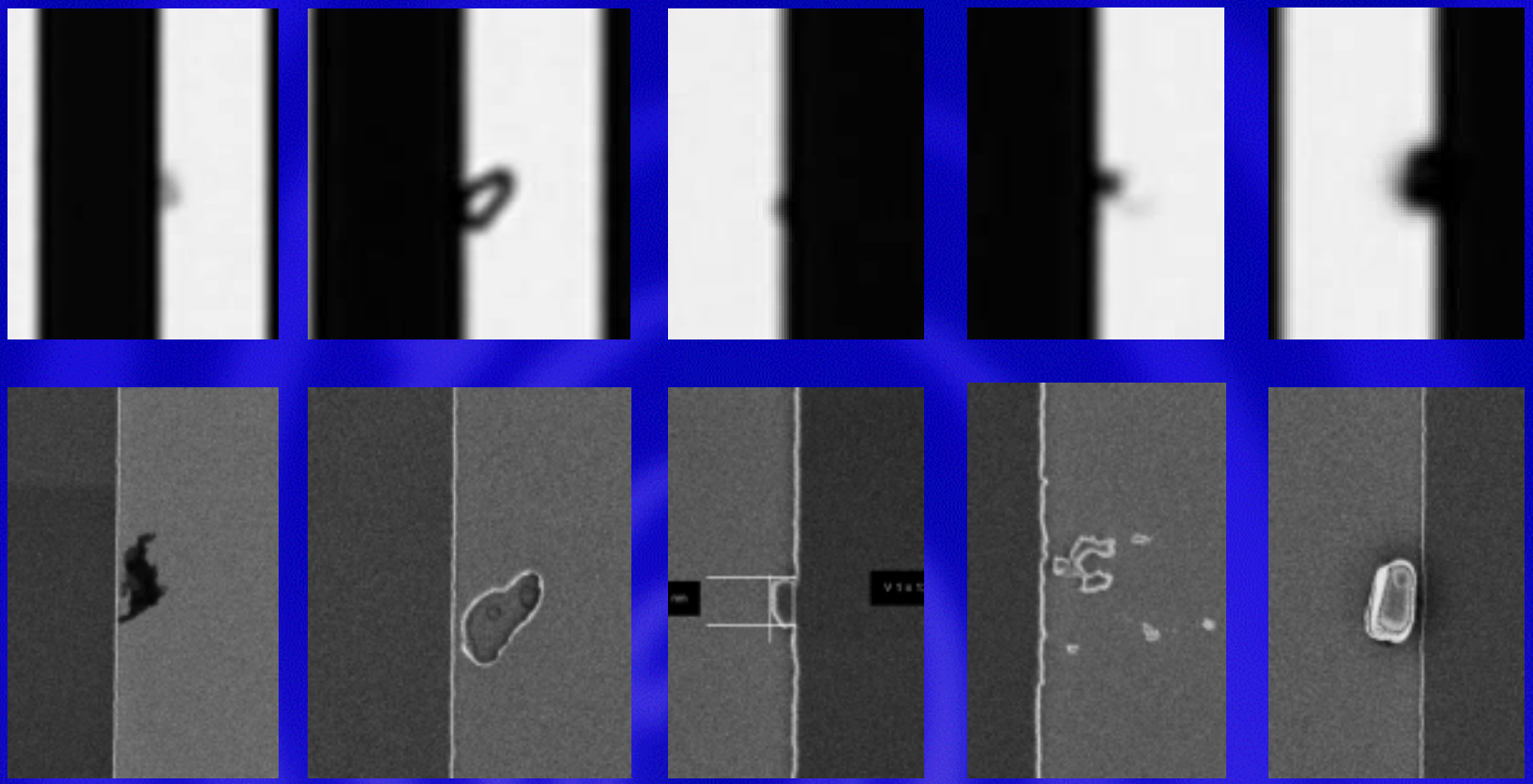
140 nm 120 nm 80 nm

Defect Size (inscribed circle)

Defects Typed by Linked DUV and SEM

DUV

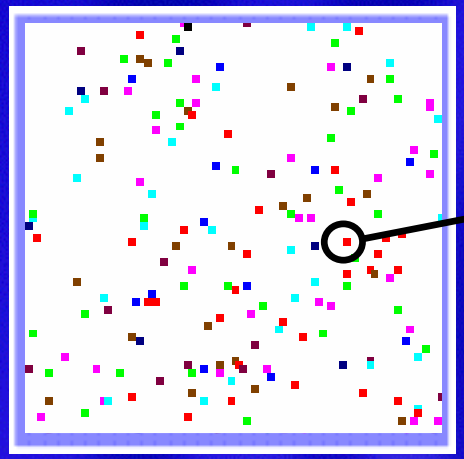
SEM



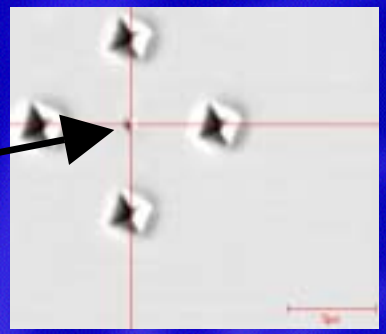
- **High-speed inspection and linked SEM provides quick feedback on defectivity**

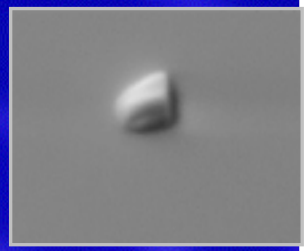
Flow for Blank Defect Analysis

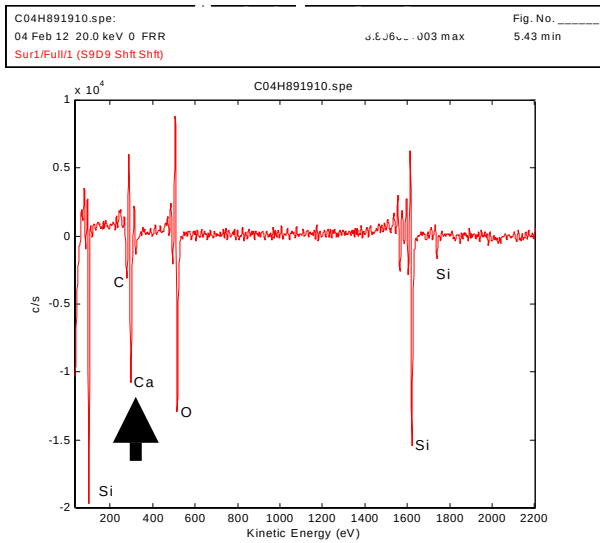
Blank Inspection → Fiducial Marking → SEM / align → FE Auger Elemental



60nm res.







- Additional data suggest defect origin
- Please see poster "Analysis of defects on EUV mask blanks and substrates" for additional details.

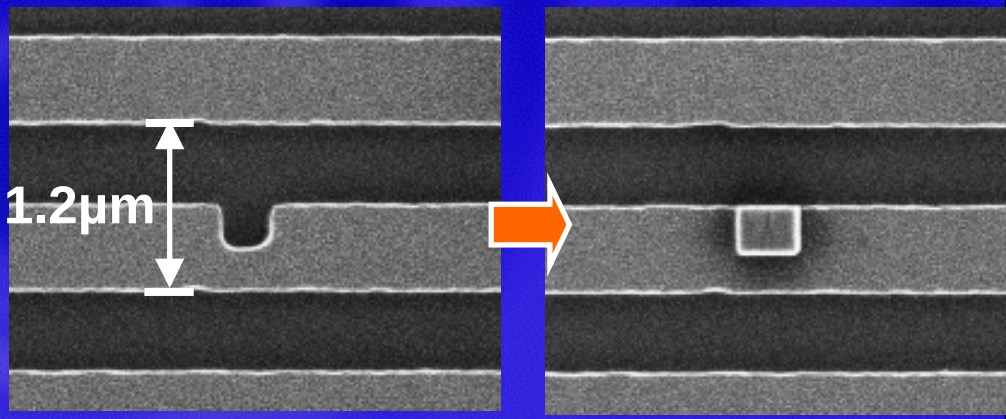
Absorber/ARC Sputter

- Module needed to follow blank inspection
- PVD cluster tool with 4 process modules
  - TaN
  - Ta-based ARC
  - Metal (chrome)
  - SiO_2
- Adapted from Si PVD tool
- Low film stress (200 MPa) demonstrated
- Loads mask from SMIF

Electron-Beam Mask Repair

- World's first e-beam mask repair tool, from NaWoTec
- Application: clear and opaque pattern defect repair
  - TaN etch, Metal dep
  - Conventional mask repair with surface charge compensation
- Capabilility
  - SEM resolution
  - Excellent edge placement precision
  - True damage-free mask repair
  - High etch selectivity
  - No EUV buffer layer required if Ru capping layer also used

Tool installed at Intel



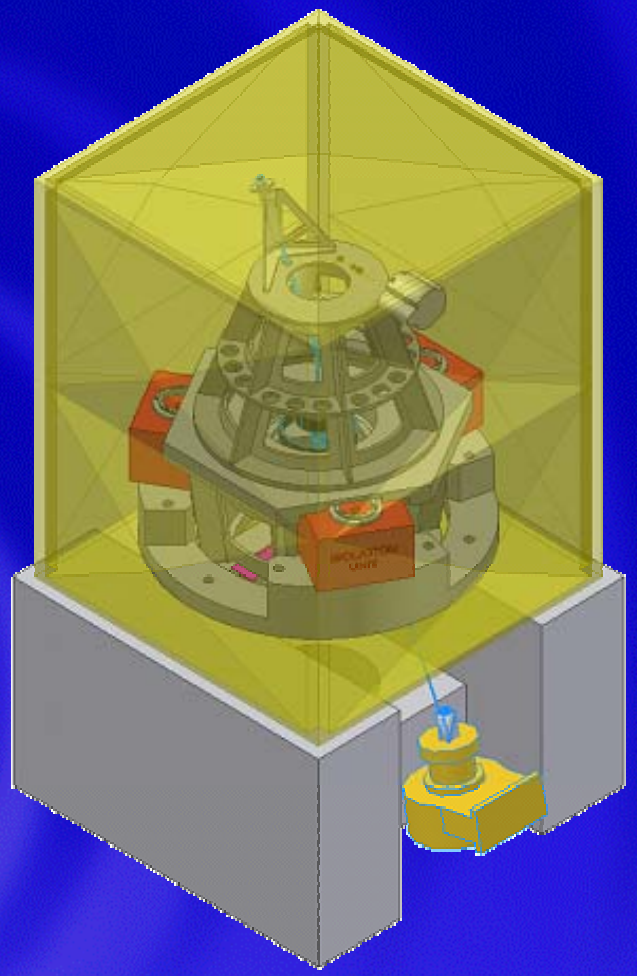
SEM of clear defect repair

Flatness Metrology

- Visible light shearing interferometer
- Applications: Blank and mask flatness
- Extensive vibration and acoustic isolation.
- Spec'd capability: 5 nm peak-valley flatness precision
- 2004 Delivery

EUV Aerial Image Metrology

- EUV version of standard tool
  - Emulates 0.25 NA exposure tool
  - Repair qualification use
  - Multilayer defect actinic metrology
- Capability:
  - EUV reticle imaging optics
  - Köhler illumination
  - Variable partial coherence
  - Robot reticle handling - loading from SMIF pod & pre-alignment
  - Automated focus finding & thru focus image capture
- 2006 Delivery
  - Use MET print tests in 2005



Exitech Tool Concept

EUV AIM Development

- Extra care required to set development direction.
- ISMT enlisted a team of experts to clarify design issues:
  - John Taylor and Anton Barty of LLNL
    - Evaluated several design concepts
    - Defined key criteria for each design option.
  - Resource for bidders
  - Resource for ISMT technical decision makers
- Tool selection and development funding by ISMT.

LLNL Design Study
J. Taylor, A. Barty

Status as of Today

- Pilot Line is a Work in Progress
  - Process modules added as they become available
  - Tools installed as they are delivered
  - Production tools to replace beta tools when they are ready.
- Today
  - 7 EUV-specific tools defined and funded
  - 3 EUV-specific tools delivered
  - EUV masks made for internal use.

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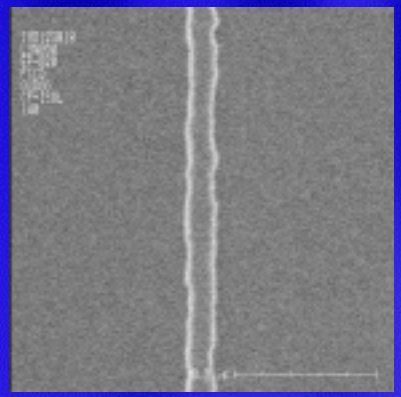
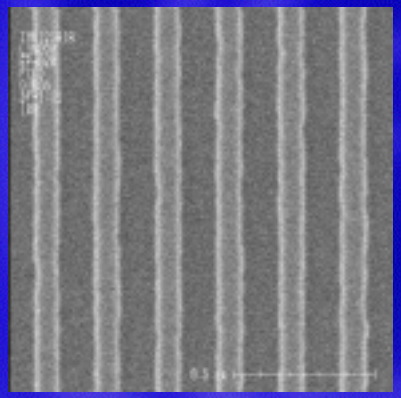
Recent Mask Results

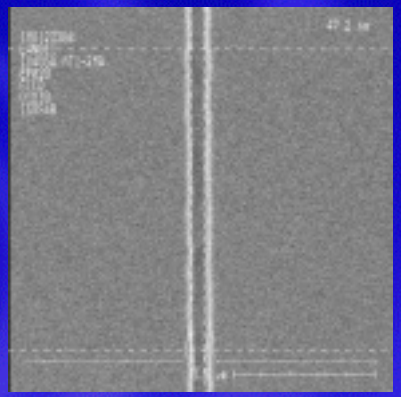
- Process resolution targeted for 32nm node feature sizes.
  - Supports 0.3NA EUV micro exposure tool.
  - TaBN absorber on Ru capping layer
  - Patterning done with production e-beam writer



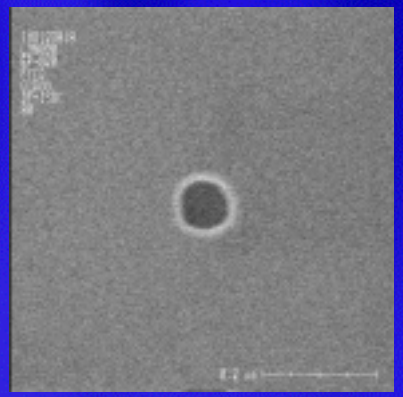
106nm
coded 140



121 nm space
95 nm line



47 nm space
coded 48



78nm
coded 80

Summary

- Intel's EUV mask pilot line is up and running.
  - Vehicle for process, material and infrastructure development.
  - Defect reduction tools and methods in place
  - Process has been simplified
  - Now supplying EUV masks for lithography development.
- 7 EUV-specific tools defined and funded
  - 3 tools installed at Intel so far
  - Thanks to ISMT for support (see 2004 PMJ)
    - 3 tools, blanks and materials