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Advances in EUV Lithography Development for Sub-50nm DRAM Nodes

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Never stop thinking.

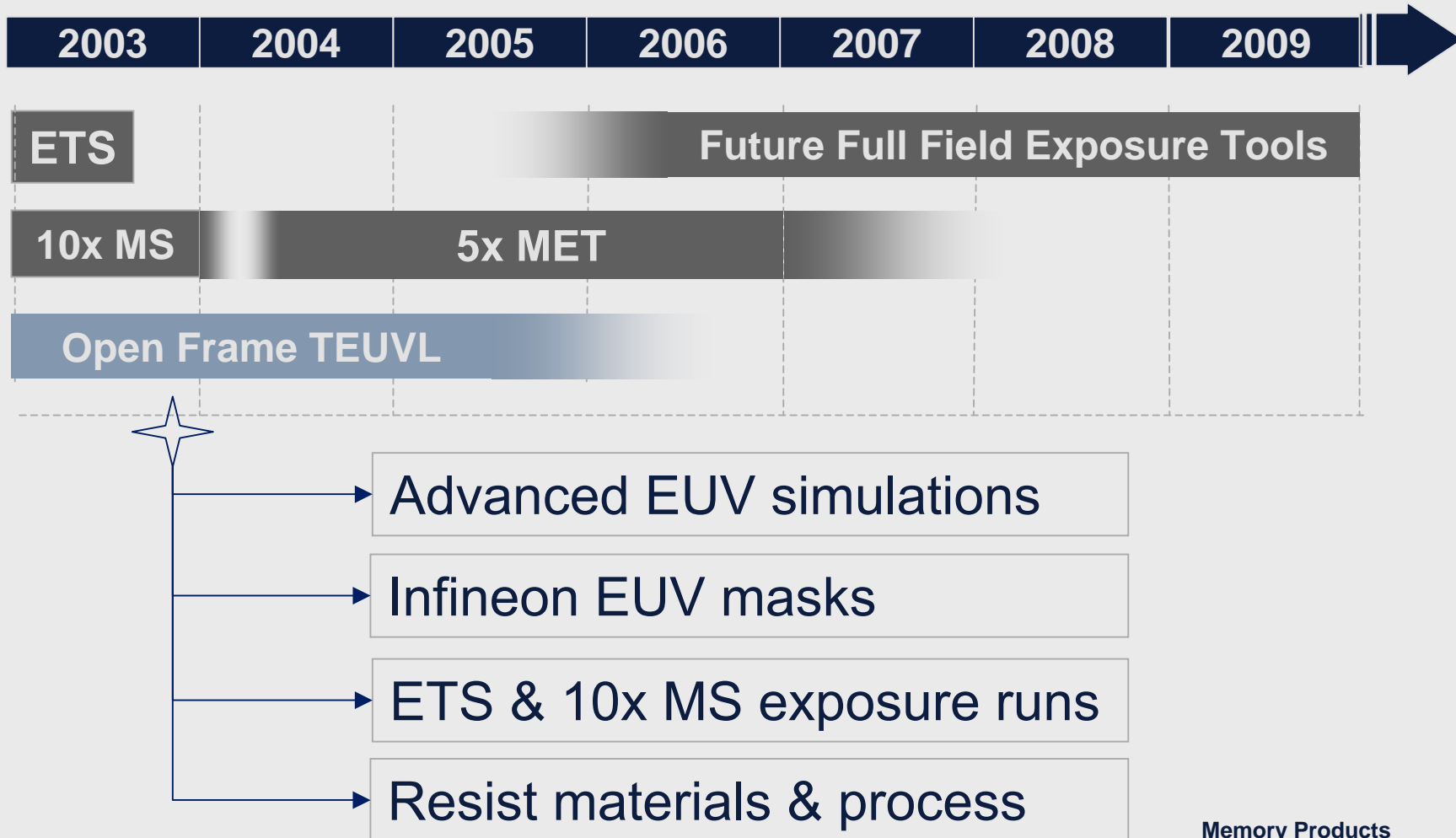
Contents

- Introduction
- Simulation tools
- Lithography process characterization / optimization
- Infineon absorber masks
- Line edge roughness (LER)
- Resist profiles
- Conclusion

Why EUV for sub-50nm DRAM Manufacturing?

- Only world-wide accepted NGL-candidate
- Assuming reasonable throughput (>100 wph) cost of ownership allows further DRAM device shrinkage

EUVL Development for Sub-50nm DRAM Nodes



Contents

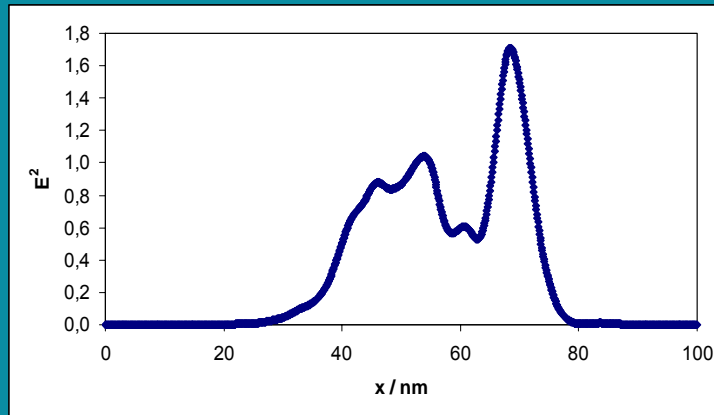
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Simulator Tool Comparison – Near Field

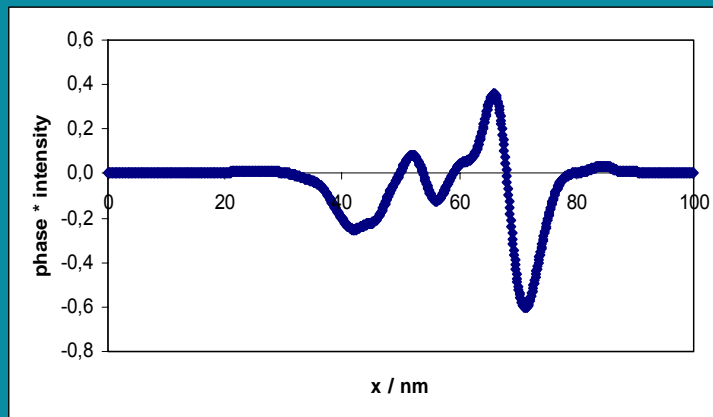
Topographical mask: dense lines/spaces, 50 nm

Delight3D

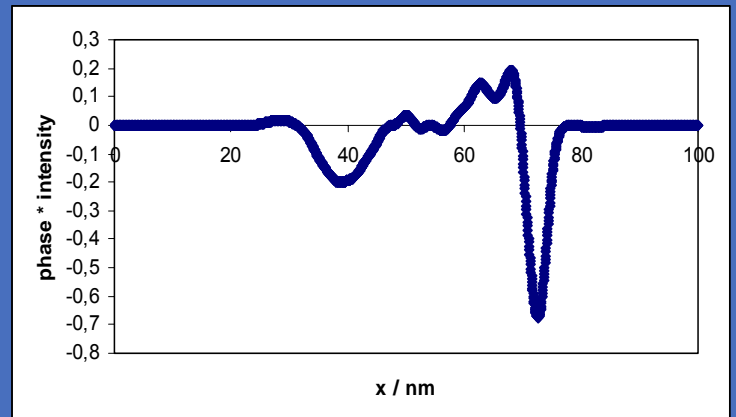
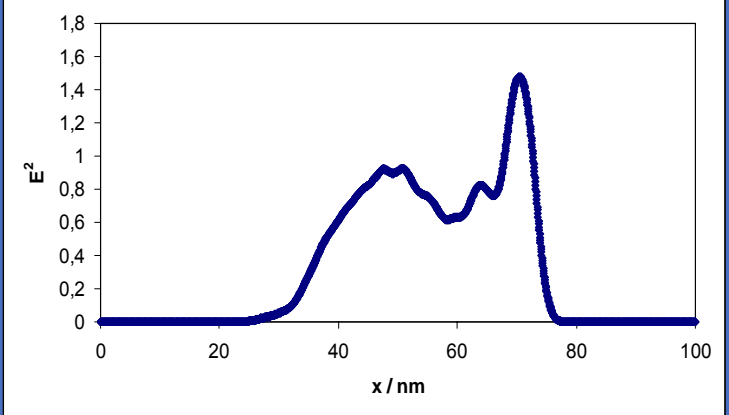
intensity



phase



Solid-EUV



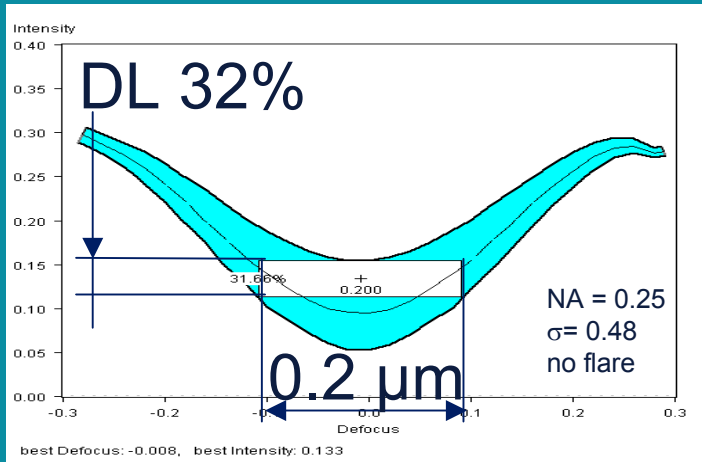
Simulator Tool Comparison – Aerial Image Consistency

Topographical mask: dense lines/spaces

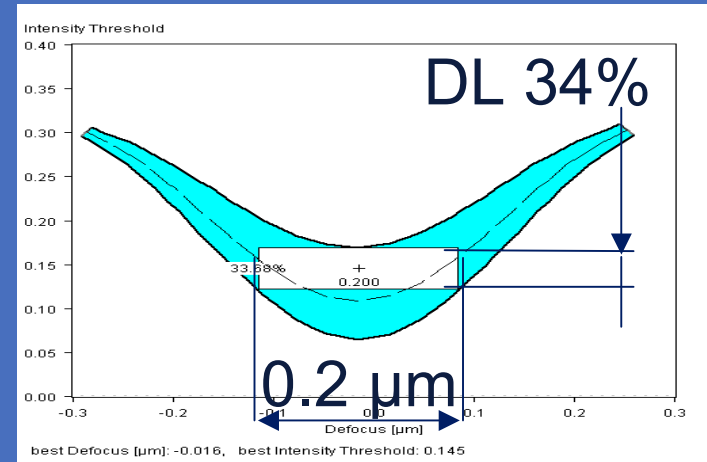
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process window
dense lines 50 nm

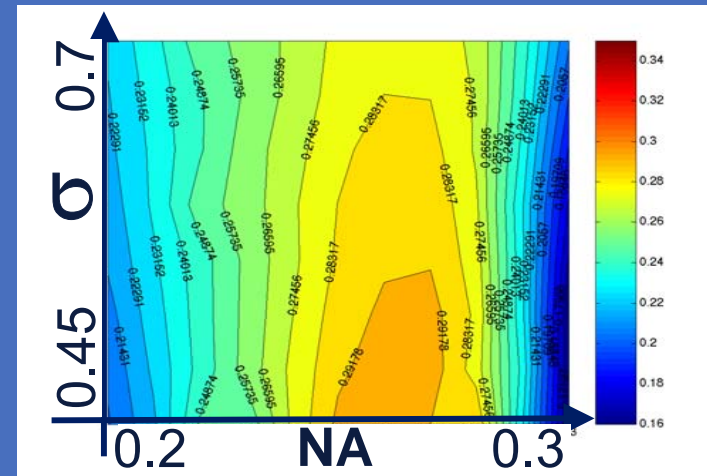
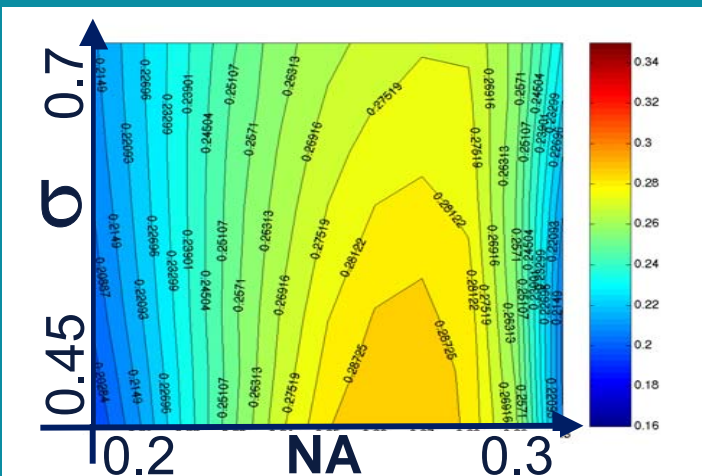
Delight3D



Solid-EUV

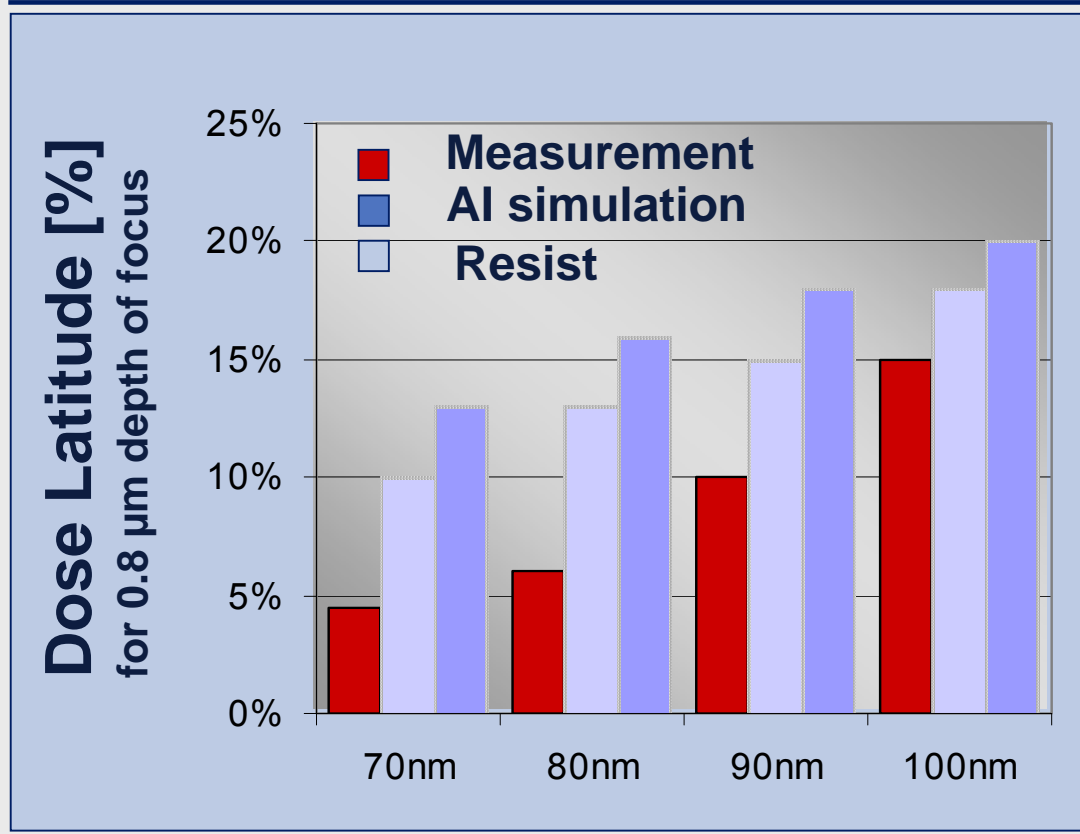


NA-sigma scan
dense lines 32 nm



Comparison: Simulation / ETS Results

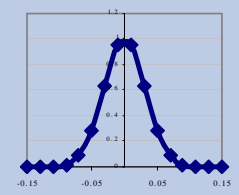
(NA = 0.1 / $\lambda = 13.4$ / dense lines, 50% pattern density)



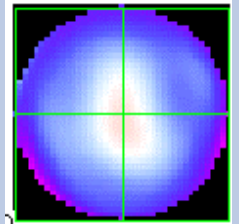
Litho process consumes 25 – 50 % of the process window

Room for improved process control !

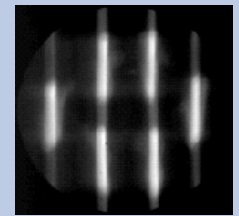
Flare PSF



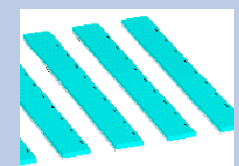
Aberrations from measurement



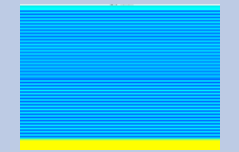
Real illuminator



IFX ETS1 Cr-absorber mask



Ideal blank



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Process Characterization

Utilizing Open Frame Exposure Tool TEUVL

Shibley EUV-2D

Resist sensitivity dependence on process parameters

	EUV	248nm
Resist Thickness	0.5 % per nm	0.5 % per nm
PEB Temperature	1.0 % per °C	1.0 % per °C
PAB Temperature	0.5 % per °C	0.5 % per °C
Development Time	0.2 % per 10s	0.2 % per 10s

- No difference 248nm / EUV
- (Same result for resist contrast)
- Ongoing: CD variation versus process parameters
- **Sufficient process stability!**

Process Parameter Optimization

Utilizing Open Frame Exposure Tool TEUVL

Shibley EUV-2D

Optimized parameters for best contrast and sensitivity

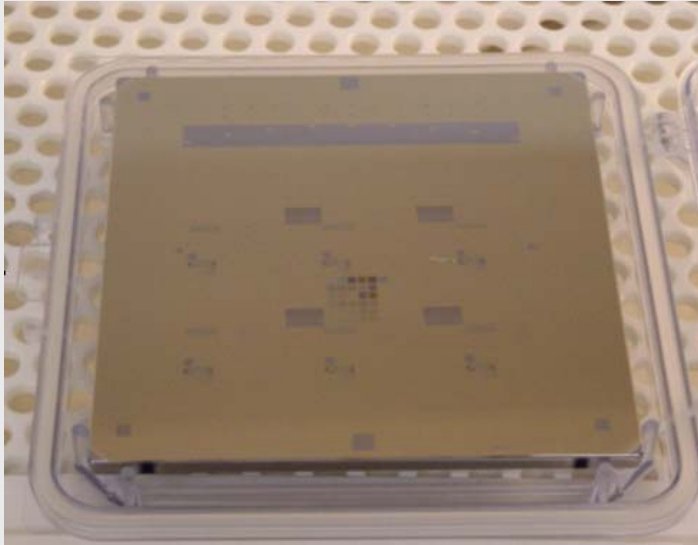
	EUV		248nm
Resist Thickness	100	≠	120
PEB Temperature	135		130
PAB Temperature	120		130
Development Time	60		45

- **Best working point differs from 248nm to EUV**

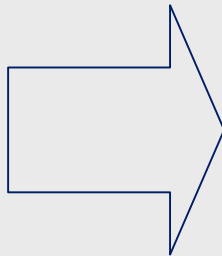
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2 Masks for ETS Exposures



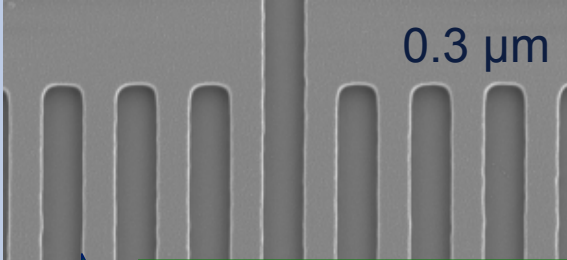
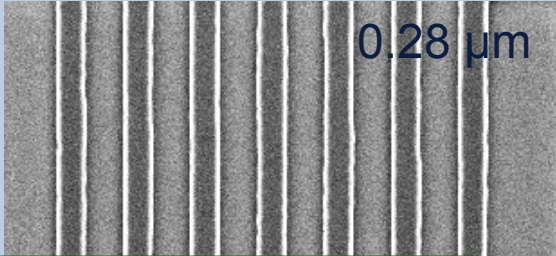


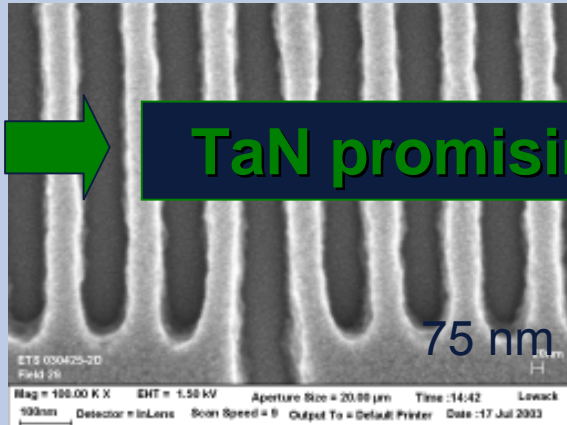
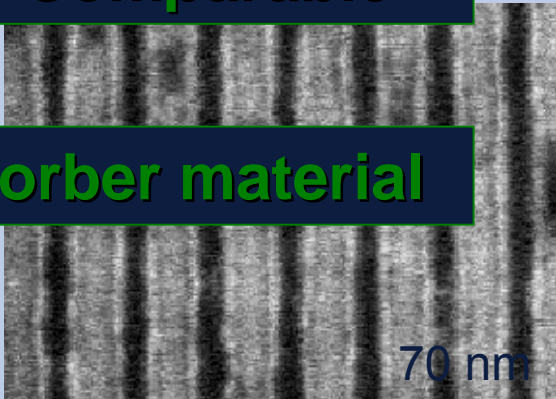

- Cr absorber
 - Standard absorber material
- TaN absorber
 - Better CD uniformity
 - Small etch bias



Cr and TaN mask manufactured by Infineon and IMS-Chips

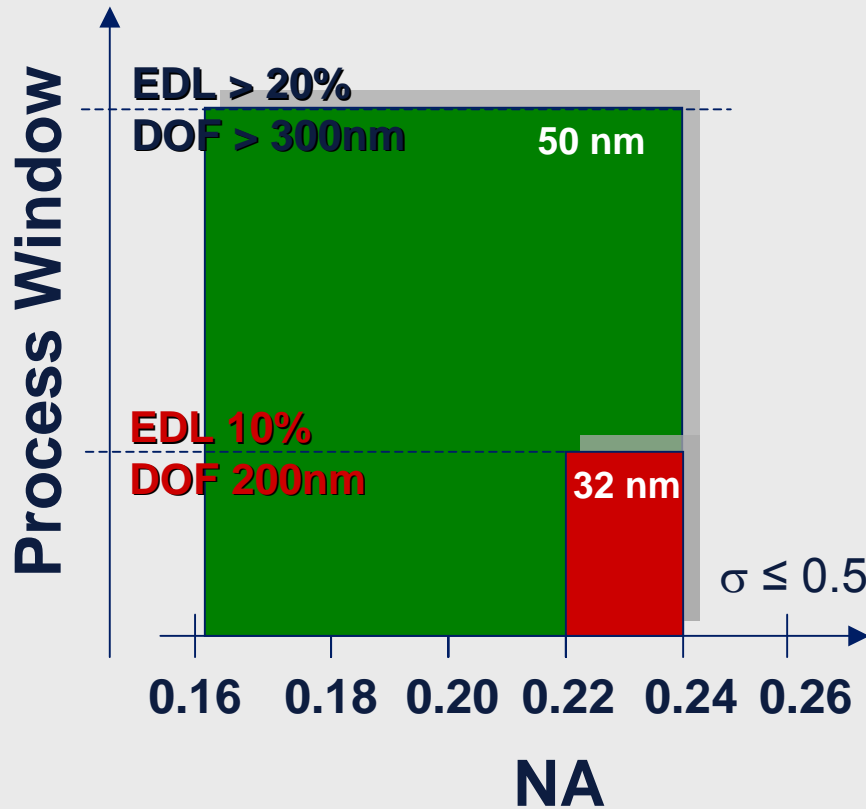
ETS Exposures: Cr & TaN Absorber Masks

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	Cr 75nm* dense lines 	TaN 70nm* dense lines 	
mask		75 / 70 nm half pitch	
		Process Windows Comparable	
ETS exposure			
		TaN promising absorber material	

* at wafer level

Limits of Cr/TaN Absorber Masks



Aerial image simulation:

- NA- σ -scan
- Typical DRAM configuration:
dense and isolated lines
- 10 nm CD tolerance
- 8% flare
- bias optimized
- 1nm mask error

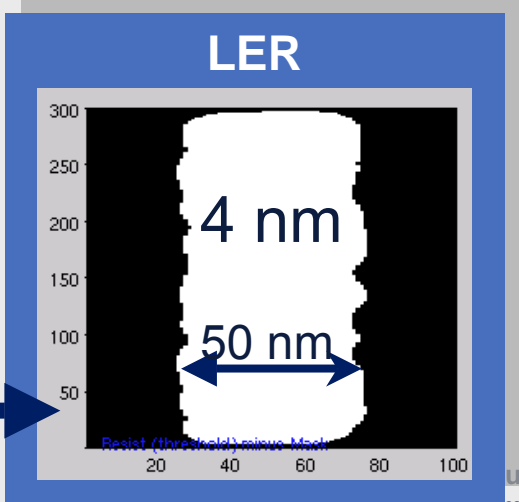
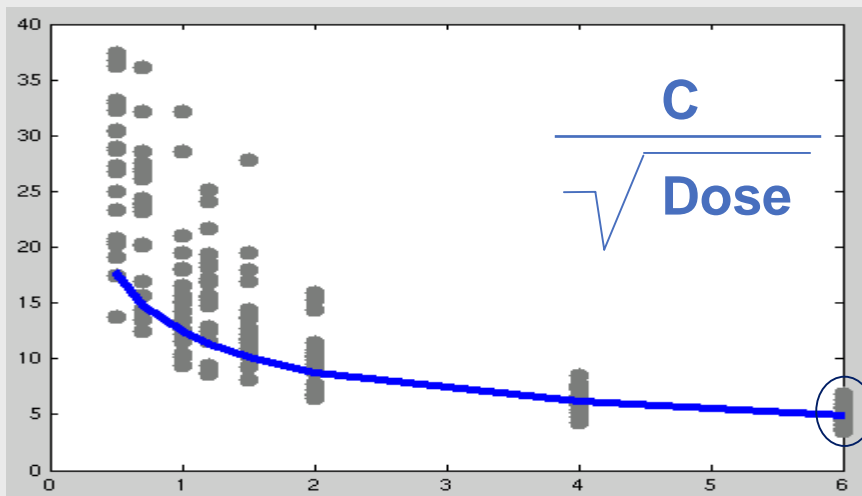
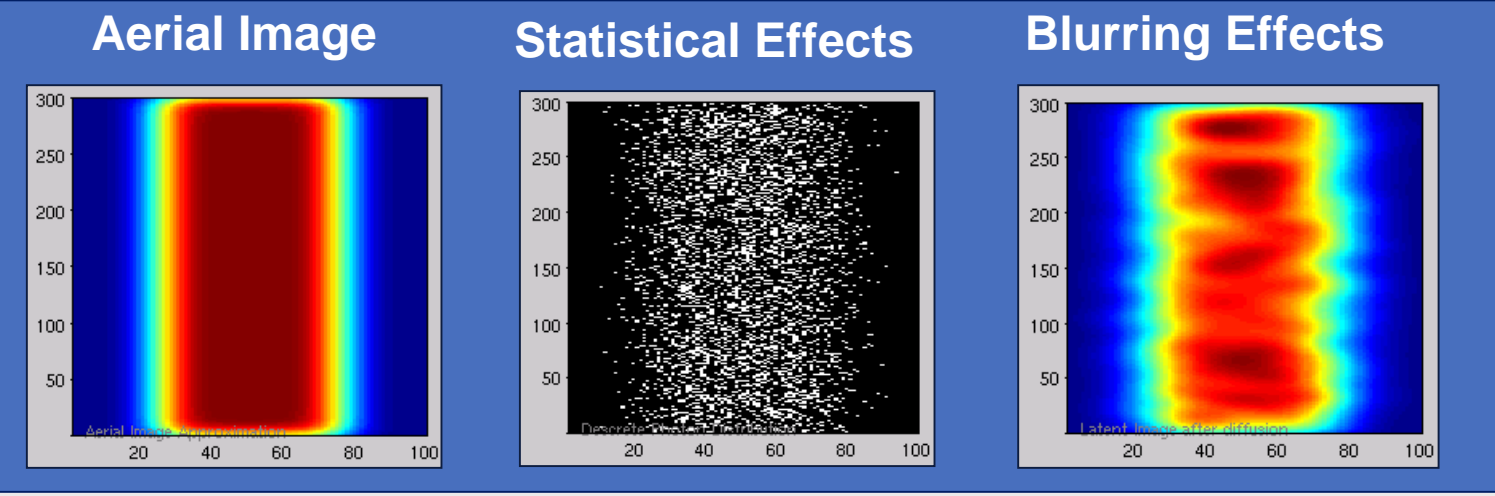
- Low sigma / NA adjustable: **0.16 – 0.25**
- New mask concepts needed for sub-30nm technology nodes

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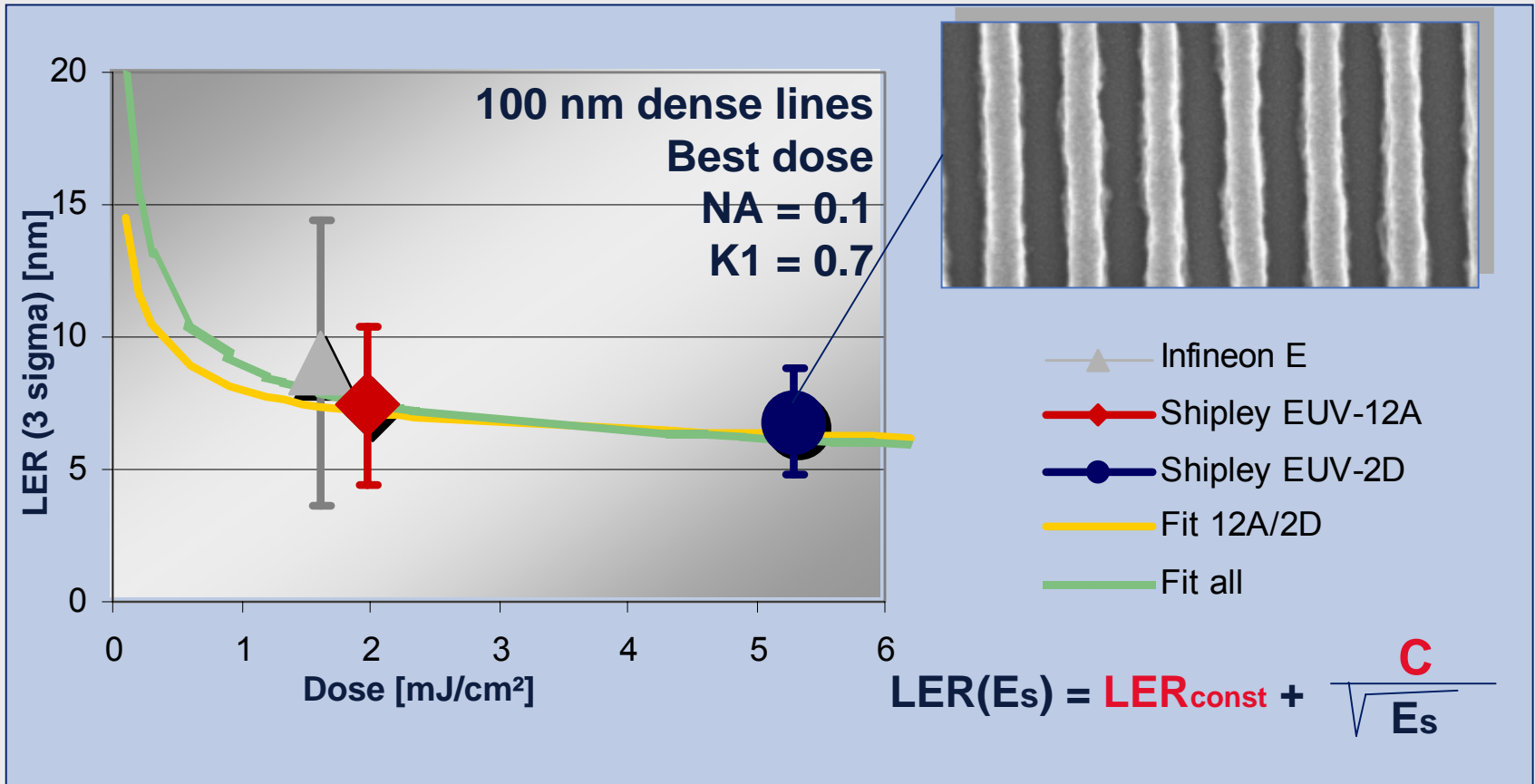
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Line Edge Roughness - Simulation

Weak source / high sensitive resists required & High photon energy



'Photon Statistics' Impacts Printing Results



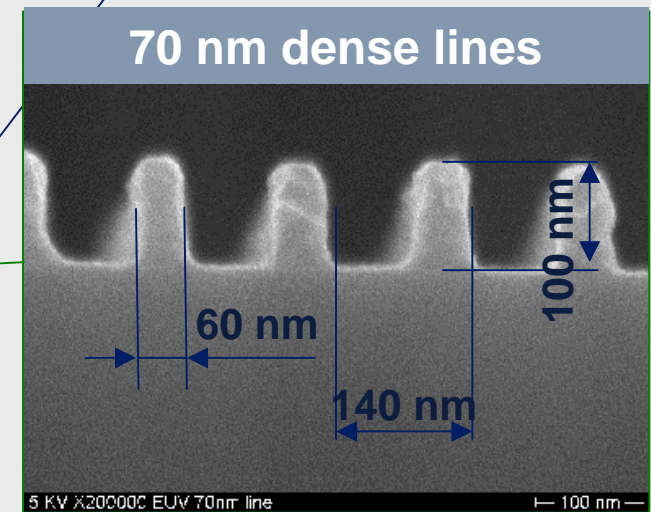
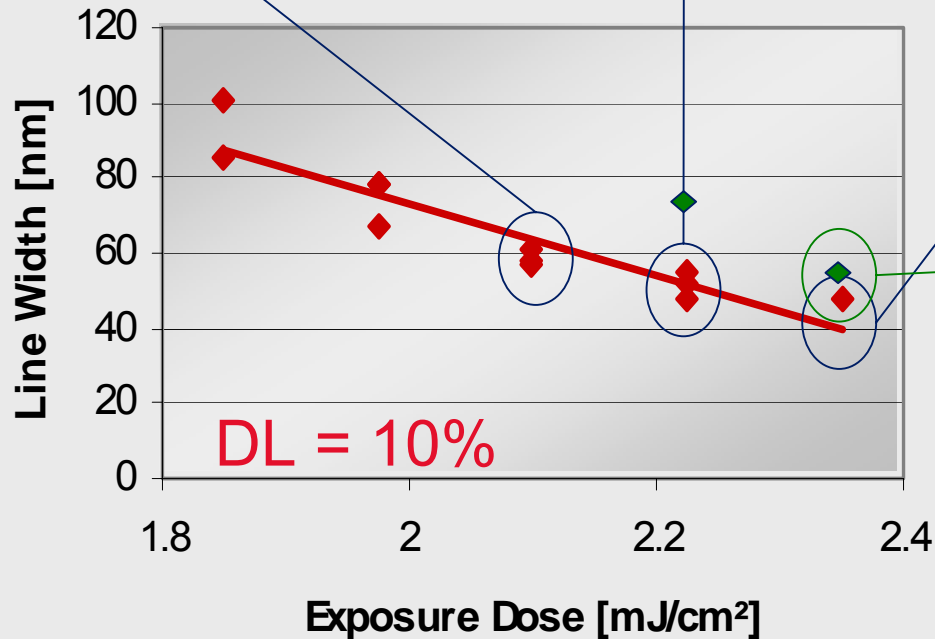
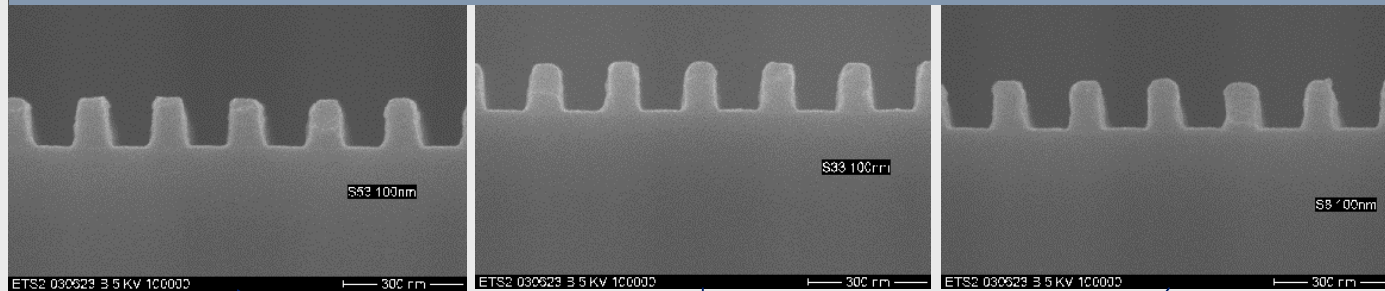
- Dose independent (constant) LER >3 – 5 nm
- Dose dependent LER relevant at EUV doses

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Profiles / Shipley EUV-12A on Silicon Substrate

100 nm dense lines [- 40 / 4 nm mask bias]



Suitable profiles for pattern transfer !

Conclusion

- Major results:
 - Suitable resist profiles for pattern transfer obtained with high sensitive Shipley EUV-12A resist
 - Resist response to process parameters comparable to 248nm lithography
 - “Shot Noise” effects are not dramatic but contribute to LER above $2\text{mJ}/\text{cm}^2$
 - TaN promising absorber material down to 30nm node
 - Alternative mask concepts needed for sub-30nm nodes

- We are confident that EUVL process can meet the specifications of sub-50nm DRAM technology nodes